LP3939 Power Amplifier Driver for Dual Band CDMA Handsets

Check for Samples: LP3939

FEATURES

- **Power-switch for dual band CDMA power amplifier**

KEY SPECIFICATIONS

- **0.002 µA Quiescent Current (typ)**
- **LLP16 Package**

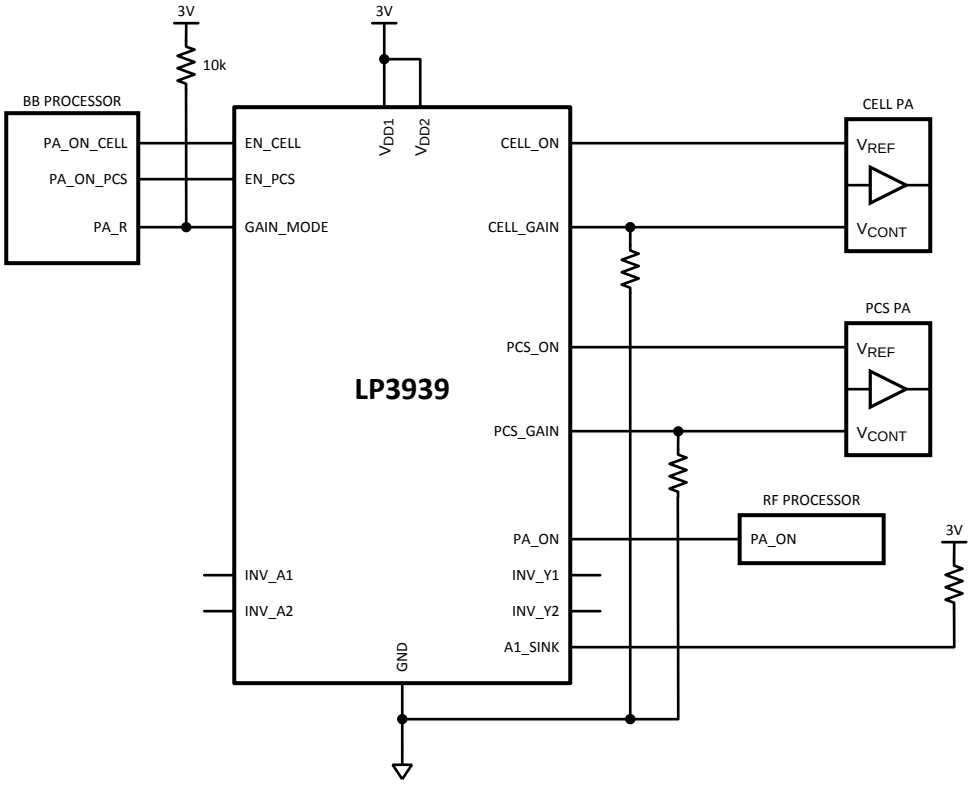
APPLICATIONS

- **Dual-band CDMA phones with MSM3xxx or MSM5xxx platform**

DESCRIPTION

Designed specifically for Qualcomm's MSM3xxx and MSM5xxx series, the LP3939 is an integrated device that provides interface to the baseband processor to power-switch two independent power amplifiers in dual band applications. By integrating the discrete components necessary to achieve the same functions, the LP3939 drastically reduces board space and component cost.

LP3939 Application Circuit



NOTE: This application circuit shows the connection interface to a typical Skyworks PA. Connections to other PA vendors may vary slightly.

Connection Diagram

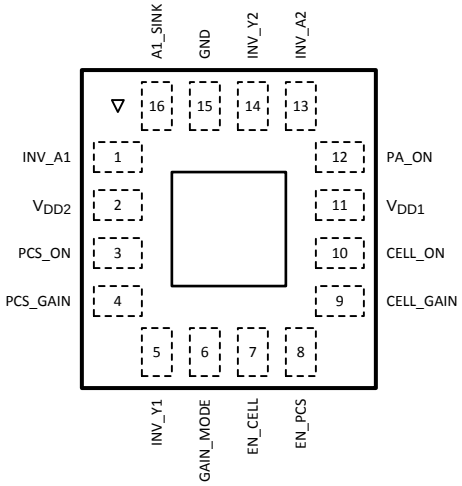


Figure 1. Top View

Table 1. Pin Descriptions

Pin	Name	Functional Description
1	INV_A1	Input
2	V_{DD2}	Supply. V_{DD1} and V_{DD2} must be tied together externally.
3	PCS_ON	Output, open drain
4	PCS_GAIN	Output, open drain
5	INV_Y1	Output
6	GAIN_MODE	Input
7	EN_CELL	Input
8	EN_PCS	Input
9	CELL_GAIN	Output, open drain
10	CELL_ON	Output, open drain
11	V_{DD1}	Supply. V_{DD1} and V_{DD2} must be tied together externally.
12	PA_ON	Output
13	INV_A2	Input
14	INV_Y2	Output, open drain
15	GND	GND
16	A1_SINK	Output, open drain

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

V_{DD1}, V_{DD2}	−0.3V to +6.0V
EN_CELL, EN_PCS, GAIN_MODE, INV_A1, INV_A2, PA_ON, INV_Y1, CELL_ON, CELL_GAIN, PCS_ON, PCS_GAIN, INV_Y2 and A1_SINK	−0.3V to (V_{DD} + 0.3V)
GND to GND SLUG	±0.3V
Junction Temperature	150°C
Maximum Power Dissipation (3)	2.0W
Storage Temperature	−65°C to +150°C
ESD (4):	
Human Body Model	2 kV
Machine Model	200V

(1) All voltages are with respect to the potential at the GND pin.
(2) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(3) The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula: $PD = \frac{T_J - T_A}{\theta_{JA}}$ where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient temperature. The 2.0W rating appearing under Absolute Maximum Ratings results from substituting the Absolute Maximum junction temperature, 150°C for T_J, 70°C for T_A and 39.8°C/W for θ_{JA}. More power can be dissipated safely at ambient temperatures below 70°C. Less power can be dissipated safely at ambient temperatures above 70°C. The Absolute Maximum power dissipation can be increased by 25 mW for each degree below 70°C, and it must be derated by 25 mW for each degree above 70°C.
(4) The human body model is 100 pF discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Operating Ratings (1) (2)

V_{DD1}, V_{DD2}	1.8V to 5.5V
Junction Temperature	−40°C to +125°C
Operating Temperature	−40°C to +85°C
Thermal Resistance θ_{JA} (LLP16)	39.8°C/W
Maximum Power Dissipation (3)	1.38W

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) Like the Absolute Maximum power dissipation, the maximum power dissipation depends on the ambient temperature. The 1.38W rating appearing under Absolute Maximum Ratings results from substituting the Maximum junction temperature, 125°C for T_J, 70°C for T_A and 39.8°C/W for θ_{JA}. More power can be dissipated safely at ambient temperatures below 70°C. Less power can be dissipated safely at ambient temperatures above 70°C. The Absolute Maximum power dissipation can be increased by 25 mW for each degree below 70°C, and it must be derated by 25 mW for each degree above 70°C.

DC Electrical Characteristics

Unless otherwise noted, $V_{DD1} = V_{DD2} = 3V$. Typical values and limits appearing in normal type apply for $T_J = 25°C$. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40°C to +85°C. (1)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
I_{IN}	Input Current	All Input Pins	0.05		**5**	µA
I_Q	Quiescent Current	All inputs tied to V_{DD} or ground. No load at the outputs.	0.002		**5**	µA
$I_{LEAKAGE}$	Output Leakage Current	CELL_ON, PCS_ON CELL_GAIN, PCS_GAIN			**10**	µA
		A1_SINK			**5**	
R_{DS-ON}	MOSFET's ON Resistance	P-Ch, $V_{DD} = 3V$ CELL_ON, PCS_ON CELL_GAIN, PCS_GAIN	275		**500**	mΩ
		P-Ch, $V_{DD} = 2V$ CELL_ON, PCS_ON CELL_GAIN, PCS_GAIN	430		**650**	
V_{IH}	Logic High Input	$1.8V \le V_{DD} < 2.5V$ EN_CELL, EN_PCS, INV_A1, GAIN_MODE, INV_A2		**1.4**		V
		$2.5V \le V_{DD} \le 3.5V$ EN_CELL, EN_PCS, INV_A1, GAIN_MODE, INV_A2		**2.0**		
V_{IL}	Logic Low Input	$1.8V \le V_{DD} \le 3.5V$ EN_CELL, EN_PCS, INV_A1, GAIN_MODE, INV_A2			**0.4**	V
V_{OH}	Logic High Output	PA_ON, INV_Y1, $I_{SOURCE} = 1$ mA	2.93	**2.8**		V
		INV_Y2, $I_{SOURCE} = 1$ mA	2.74	**2.5**		
V_{OL}	Logic Low Output	PA_ON, INV_Y1, $I_{SINK} = 1$ mA	80		**200**	mV
		INV_Y2, A1_SINK $I_{SINK} = 1$ mA	16		**55**	

(1) All limits are guaranteed by testing or statistical analysis.

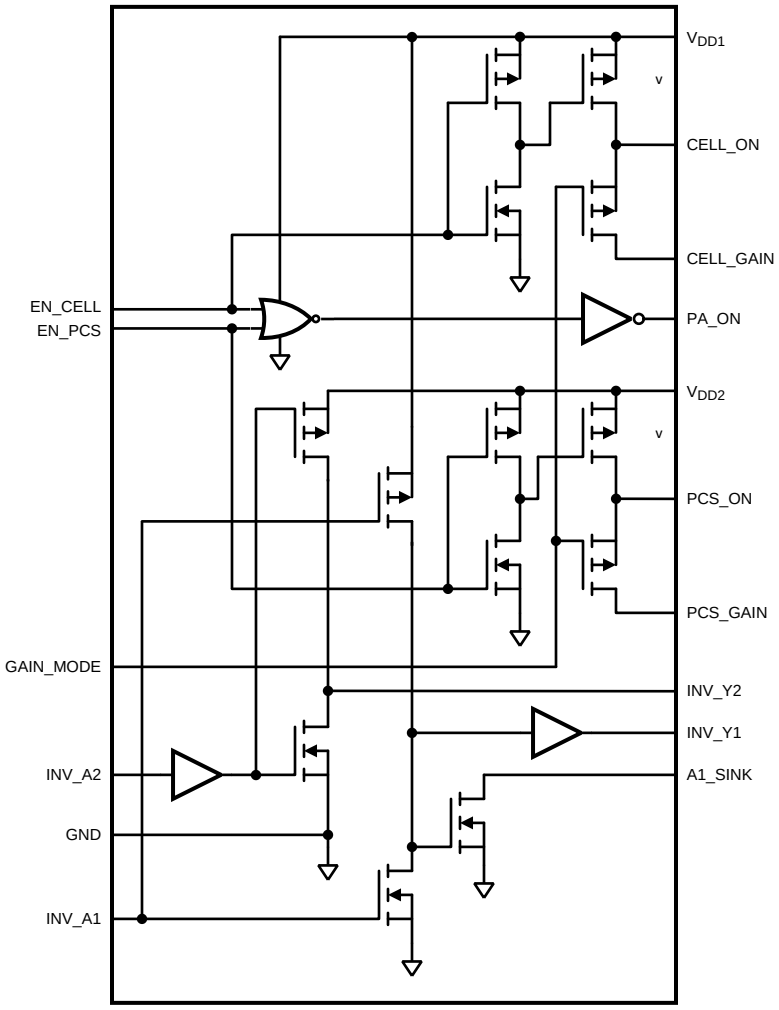
AC Electrical Characteristics

Unless otherwise noted, $V_{DD1} = V_{DD2} = 3V$, $C_{LOAD} = 50$ pF. Typical values and limits appearing in normal type apply for $T_J = 25°C$. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40°C to +85°C. (1)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
t_{PLH}	Propagations Delay Low to High	EN_CELL to PA_ON or EN_PCS to PA_ON	10		**80**	ns
		EN_CELL to CELL_ON or EN_PCS to PCS_ON $R_{PD} = 100\Omega$	7		**56**	ns
		GAIN_MODE to CELL_GAIN or GAIN_MODE to PCS_GAIN $R_{PD} = 100\Omega$	7		**56**	ns
		INV_A1 to INV_Y1	10		**80**	ns
		INV_A2 to INV_Y2	25		**200**	ns
t_{PHL}	Propagations Delay High to Low	EN_CELL to PA_ON or EN_PCS to PA_ON	10		**80**	ns
		EN_CELL to CELL_ON or EN_PCS to PCS_ON $R_{PD} = 100\Omega$	25		**200**	ns
		GAIN_MODE to CELL_GAIN or GAIN_MODE to PCS_GAIN $R_{PD} = 100\Omega$	20		**160**	ns
		INV_A1 to INV_Y1	10		**80**	ns
		INV_A1 to A1_SINK $R_{PU} = 10$ kΩ	5		**40**	ns
		INV_A2 to INV_Y2	5		**40**	ns
t_{RISE}	Rise Time	PA_ON	15		**120**	ns
		INV_Y2	50		**400**	
		INV_Y1	20		**160**	
T_{FALL}	Fall Time	PA_ON	15		**120**	ns
		INV_Y2	10		**80**	
		INV_Y1	20		**160**	

(1) All AC parameters are guaranteed by design, not production tested.

LP3939 Block Diagram



Truth Tables

Table 2. PA Enables

INPUTS		OUTPUTS(1)		
EN_CELL	EN_PCS	CELL_ON	PCS_ON	PA_ON
0	0	0	0	0
1	0	1	0	1
0	1	0	1	1
1	1	Not Valid		

(1) **Note:** Measured with a 10 kΩ pull down resistor on CELL_ON and PCS_ON.

Table 3. PA Gain Mode

INPUTS			OUTPUTS(1)	
GAIN_MODE	EN_CELL	EN_PCS	CELL_GAIN	PCS_GAIN
0	0	0	0	0
0	1	0	1	0
1	1	0	0	0
0	0	1	0	1
1	0	1	0	0
X	1	1	Not Valid	

(1) **Note:** Measured with a 10 kΩ pull down resistor on CELL_GAIN and PCS_GAIN.

Table 4. Current Sink Control

INPUTS	OUTPUTS(1)	
INV_A1	INV_Y1	A1_SINK
0	1	0
1	0	1
INV_A2	INV_Y2	
0	1	
1	0	

(1) **Note:** Measured with a 10 kΩ pull up resistor on A1_SINK.

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