

## LP5996 Dual Linear Regulator with 300mA and 150mA Outputs

Check for Samples: [LP5996](#)

### FEATURES

- 2 LDO Outputs with Independent Enable
- 1.5% Accuracy at Room Temperature, 3% over Temperature
- Thermal Shutdown Protection
- Stable with Ceramic Capacitors

### APPLICATIONS

- Cellular Handsets
- PDA's
- Wireless Network Adaptors

### DESCRIPTION

The LP5996 is a dual low dropout regulator. The first regulator can source 150mA, while the second is capable of sourcing 300mA.

The LP5996 provides 1.5% accuracy requiring an ultra low quiescent current of 35 $\mu$ A. Separate enable pins allow each output of the LP5996 to be shut down, drawing virtually zero current.

The LP5996 is designed to be stable with small footprint ceramic capacitors down to 1 $\mu$ F.

The LP5996 is available in fixed output voltages and comes in a 10 pin, 3mm x 3mm package. .

**Table 1. Key Specifications**

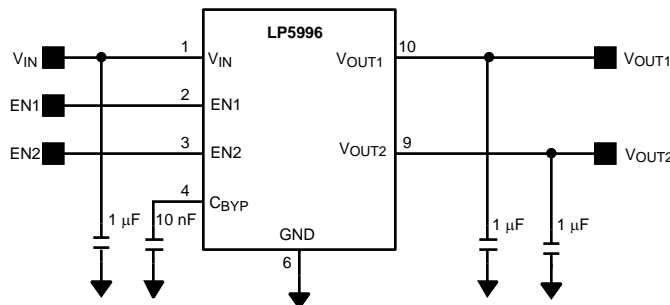
	VALUE	UNIT
Input Voltage Range	2.0V to 6.0	V
Low Dropout Voltage	210	mV at 300mA
Ultra-Low $I_Q$ (enabled)	35	$\mu$ A
Virtually Zero $I_Q$ (disabled)	<10	nA

### Package

All available in Lead Free option.

10 pin SON 3mm x 3mm

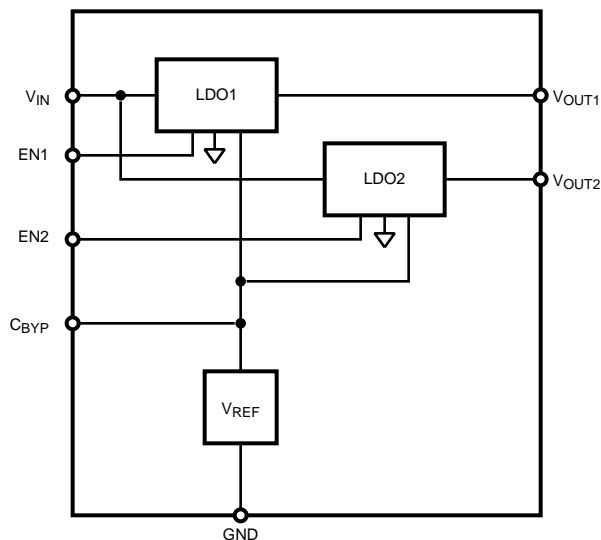
### Typical Application Circuit



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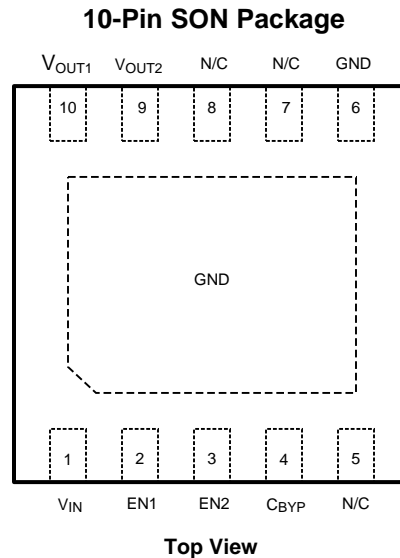
## Functional Block Diagram



### Pin Descriptions

Name	Pin No	Function
V <sub>IN</sub>	1	Voltage Supply Input. Connect a 1μF capacitor between this pin and GND.
EN1	2	Enable Input to Regulator 1. Active high input. High = On. Low = OFF.
EN2	3	Enable Input to Regulator 2. Active high input. High = On. Low = OFF.
C <sub>BYP</sub>	4	Internal Voltage Reference Bypass. Connect a 10nF capacitor from this pin to GND to reduce noise and improve line transient and PSRR. This pin may be left open.
N/C	5	No Connection. Do not connect to any other pin.
GND	6	Common Ground pin. Connect externally to exposed pad.
N/C	7	No Connection. Do not connect to any other pin.
N/C	8	No Connection. Do not connect to any other pin.
V <sub>OUT2</sub>	9	Output of Regulator 2. 300mA maximum current output. Connect a 1μF capacitor between this pin to GND.
V <sub>OUT1</sub>	10	Output of Regulator 1. 150mA maximum current output. Connect a 1μF capacitor between this pin to GND.
GND	Pad	Common Ground. Connect to Pin 6.

## Connection Diagram



**Figure 1. See Package Number DSC0010A**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings <sup>(1) (2)(3)</sup>

Input Voltage	-0.3V to 6.5V
V <sub>OUT1</sub> , V <sub>OUT2</sub> , EN1, and EN2 Voltage to GND	-0.3V to (V <sub>IN</sub> + 0.3V) with 6.5V (max)
Junction Temperature (T <sub>J-MAX</sub> )	150°C
Lead/Pad Temp. <sup>(4)</sup>	235°C
Storage Temperature	-65°C to 150°C
Continuous Power Dissipation Internally Limited <sup>(5)</sup>	
ESD Rating <sup>(6)</sup>	
Human Body Model	2.0kV
Machine Model	200V

- (1) All Voltages are with respect to the potential at the GND pin.
- (2) Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
- (3) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**
- (4) For detailed soldering specifications and information, please refer to National Semiconductor Application Note AN-1187, Leadless Leadframe Package.
- (5) Internal thermal shutdown circuitry protects the device from permanent damage.
- (6) The human body model is 100pF discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

### Operating Ratings <sup>(1) (2)</sup>

Input Voltage	2.0V to 6.0V
EN1, EN2 Voltage	0 to (V <sub>IN</sub> + 0.3V) to 6.0V (max)

- (1) Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
- (2) All Voltages are with respect to the potential at the GND pin.

**Operating Ratings** <sup>(1)</sup> <sup>(2)</sup> (continued)

Junction Temperature	-40°C to 125°C
Ambient Temperature Range, T <sub>A</sub> <sup>(3)</sup>	-40°C to 85°C

- (3) The maximum ambient temperature (T<sub>A(max)</sub>) is dependant on the maximum operating junction temperature (T<sub>J(max-op)</sub> = 125°C), the maximum power dissipation of the device in the application (P<sub>D(max)</sub>), and the junction to ambient thermal resistance of the part/package in the application (θ<sub>JA</sub>), as given by the following equation: T<sub>A(max)</sub> = T<sub>J(max-op)</sub> - (θ<sub>JA</sub> × P<sub>D(max)</sub>).

**Thermal Properties** <sup>(1)</sup>

Junction To Ambient Thermal Resistance <sup>(2)</sup>	
θ <sub>JA</sub> SON-10 Package	55°C/W

- (1) Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
- (2) Junction to ambient thermal resistance is dependant on the application and board layout. In applications where high maximum power dissipation is possible, special care must be paid to thermal dissipation issues in board design.

**Electrical Characteristics** <sup>(1)</sup> <sup>(2)</sup>

Unless otherwise noted, V<sub>EN</sub> = 950mV, V<sub>IN</sub> = V<sub>OUT</sub> + 1.0V, or 2.0V, whichever is higher, where V<sub>OUT</sub> is the higher of V<sub>OUT1</sub> and V<sub>OUT2</sub>. C<sub>IN</sub> = 1 μF, I<sub>OUT</sub> = 1 mA, C<sub>OUT1</sub> = C<sub>OUT2</sub> = 1.0μF.

Typical values and limits appearing in normal type apply for T<sub>A</sub> = 25°C. Limits appearing in **boldface** type apply over the full junction temperature range for operation, -40 to +125°C.

Parameter		Test Conditions		Typ	Limit		Units
					Min	Max	
V <sub>IN</sub>	Input Voltage	(3)			2	6	V
ΔV <sub>OUT</sub>	Output Voltage Tolerance	I <sub>OUT</sub> = 1mA	1.5V < V <sub>OUT</sub> ≤ 3.3V		-2.5 <b>-3.75</b>	+2.5 <b>+3.75</b>	%
			V <sub>OUT</sub> ≤ 1.5V		-2.75 <b>-4</b>	+2.75 <b>+4</b>	
	Line Regulation Error	V <sub>IN</sub> = (V <sub>OUT(NOM)</sub> + 1.0V) to 6.0V		0.03		<b>0.3</b>	%/V
	Load Regulation Error	I <sub>OUT</sub> = 1mA to 150mA (LDO 1)		85		<b>155</b>	μV/mA
		I <sub>OUT</sub> = 1mA to 300mA (LDO 2)		26		<b>85</b>	
V <sub>DO</sub>	Dropout Voltage <sup>(4)</sup>	I <sub>OUT</sub> = 1mA to 150mA (LDO 1)		110		<b>220</b>	mV
		I <sub>OUT</sub> = 1mA to 300mA (LDO 2)		210		<b>550</b>	
I <sub>Q</sub>	Quiescent Current	LDO 1 ON, LDO 2 ON I <sub>OUT1</sub> = I <sub>OUT2</sub> = 0mA		35		<b>100</b>	μA
		LDO 1 ON, LDO 2 OFF I <sub>OUT1</sub> = 150mA		45		<b>110</b>	
		LDO 1 OFF, LDO 2 ON I <sub>OUT2</sub> = 300mA		45		<b>110</b>	
		LDO 1 ON, LDO 2 ON I <sub>OUT1</sub> = 150mA, I <sub>OUT2</sub> = 300mA		70		<b>170</b>	
		V <sub>EN1</sub> = V <sub>EN2</sub> = 0.4V		0.5		<b>10</b>	nA
I <sub>SC</sub>	Short Circuit Current Limit	LDO 1		420		<b>750</b>	mA
		LDO 2		550		<b>840</b>	
I <sub>OUT</sub>	Maximum Output Current	LDO 1			<b>150</b>		mA
		LDO 2			<b>300</b>		

(1) All Voltages are with respect to the potential at the GND pin.

(2) Min Max limits are guaranteed by design, test or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

(3) V<sub>IN(MIN)</sub> = V<sub>OUT(NOM)</sub> + 0.5V, or 2.0V, whichever is higher.

(4) Dropout voltage is voltage difference between input and output at which the output voltage drops to 100mV below its nominal value. This parameter only for output voltages above 2.0V

## Electrical Characteristics<sup>(1) (2)</sup> (continued)

Unless otherwise noted,  $V_{EN} = 950\text{mV}$ ,  $V_{IN} = V_{OUT} + 1.0\text{V}$ , or  $2.0\text{V}$ , whichever is higher, where  $V_{OUT}$  is the higher of  $V_{OUT1}$  and  $V_{OUT2}$ .  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $C_{OUT1} = C_{OUT2} = 1.0\text{ }\mu\text{F}$ .

Typical values and limits appearing in normal type apply for  $T_A = 25^\circ\text{C}$ . Limits appearing in **boldface** type apply over the full junction temperature range for operation,  $-40$  to  $+125^\circ\text{C}$ .

Parameter		Test Conditions		Typ	Limit		Units
					Min	Max	
PSRR	Power Supply Rejection Ratio <sup>(5)</sup>	f = 1kHz, I <sub>OUT</sub> = 1mA to 150mA C <sub>BYP</sub> = 10nF	LDO1	58			dB
			LDO2	70			
		f = 20kHz, I <sub>OUT</sub> = 1mA to 150mA C <sub>BYP</sub> = 10nF	LDO1	45			
			LDO2	60			
e <sub>n</sub>	Output noise Voltage <sup>(5)</sup>	BW = 10Hz to 100kHz C <sub>BYP</sub> = 10nF	V <sub>OUT</sub> = 0.8V	36			μV <sub>RMS</sub>
			V <sub>OUT</sub> = 3.3V	75			
T <sub>SHUTDOWN</sub>	Thermal Shutdown	Temperature		160			°C
		Hysteresis		20			
Enable Control Characteristics							
I <sub>EN</sub>	Input Current at V <sub>EN1</sub> or V <sub>EN2</sub>	V <sub>EN</sub> = 0.0V		0.005		0.1	μA
		V <sub>EN</sub> = 6V		2		5	
V <sub>IL</sub>	Low Input Threshold					0.4	V
V <sub>IH</sub>	High Input Threshold				0.95		V
Timing Characteristics							
T <sub>ON</sub>	Turn On Time <sup>(5)</sup>	To 95% Level C <sub>BYP</sub> = 10nF		300			μs
Transient Response	Line Transient Response  δV <sub>OUT</sub>   <sup>(5)</sup>	T <sub>rise</sub> = T <sub>fall</sub> = 10μs δV <sub>IN</sub> = 1VC <sub>BYP</sub> = 10nF		20			mV (pk - pk)
	Load Transient Response  δV <sub>OUT</sub>   <sup>(5)</sup>	T <sub>rise</sub> = T <sub>fall</sub> = 1μs	LDO 1 I <sub>OUT</sub> = 1mA to 150mA	175			
			LDO 2 I <sub>OUT</sub> = 1mA to 300mA	150			

(5) This electrical specification is guaranteed by design.

## Output Capacitor, Recommended Specifications

Parameter		Test Conditions	Nom	Limit		Units
				Min	Max	
$C_{OUT}$	Output Capacitance	Capacitance <sup>(1)</sup>	1.0	<b>0.7</b>		$\mu\text{F}$
		ESR		5	500	$\text{m}\Omega$

(1) The Capacitor tolerance should be 30% or better over temperature. The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor is X7R. However, depending on the application, X5R, Y5V and Z5U can also be used. (See capacitor section in Applications Hints).

## Typical Performance Characteristics.

Unless otherwise specified,  $C_{IN} = 1.0\mu\text{F}$  Ceramic,  $C_{OUT1} = C_{OUT2} = 1.0\mu\text{F}$  Ceramic,  $C_{BYP} = 10\text{nF}$ ,  $V_{IN} = V_{OUT2(NOM)} + 1.0\text{V}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{OUT1(NOM)} = 3.3\text{V}$ ,  $V_{OUT2(NOM)} = 3.3\text{V}$ , Enable pins are tied to  $V_{IN}$ .

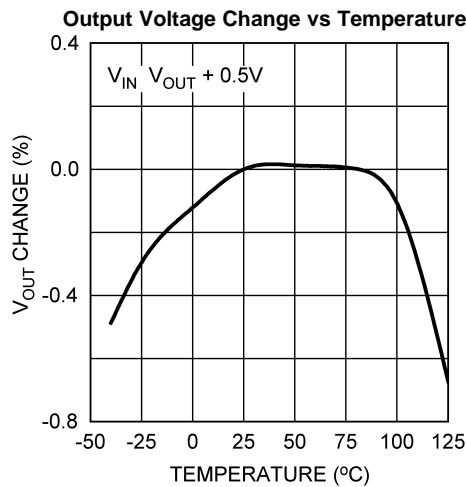


Figure 2.

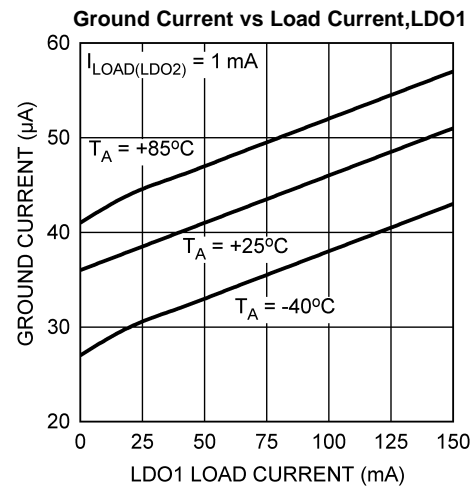


Figure 3.

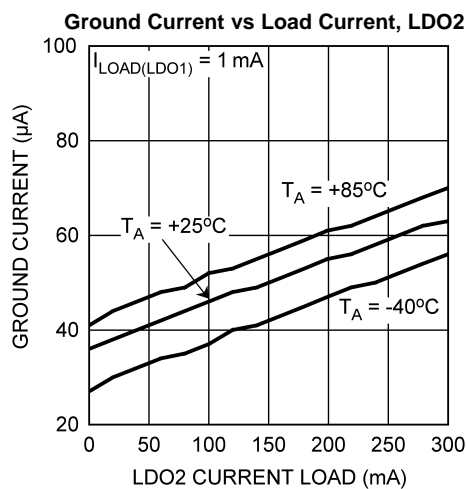


Figure 4.

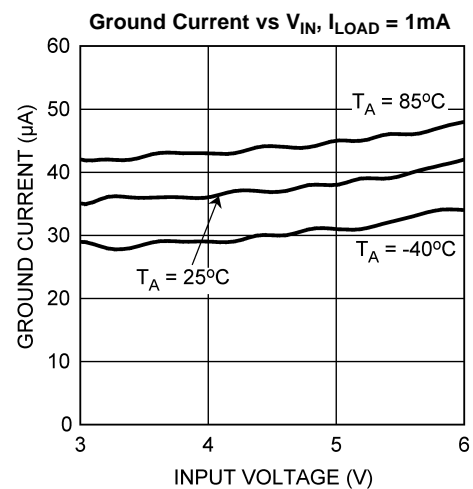


Figure 5.

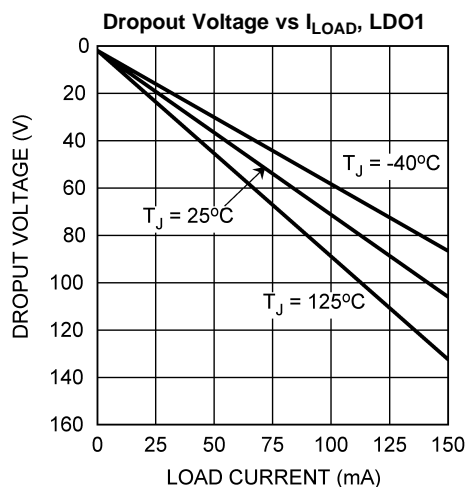


Figure 6.

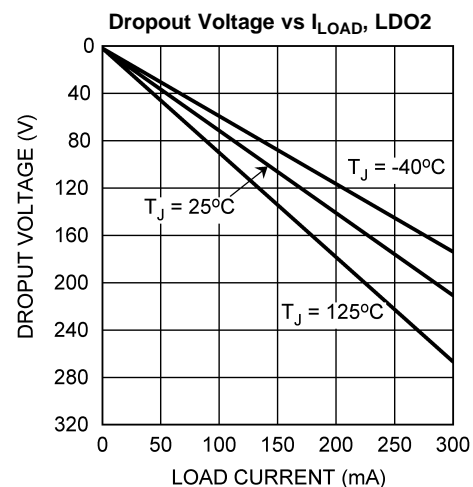


Figure 7.

## Typical Performance Characteristics. (continued)

Unless otherwise specified,  $C_{IN} = 1.0\mu\text{F}$  Ceramic,  $C_{OUT1} = C_{OUT2} = 1.0\mu\text{F}$  Ceramic,  $C_{BYP} = 10\text{nF}$ ,  $V_{IN} = V_{OUT2(NOM)} + 1.0\text{V}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{OUT1(NOM)} = 3.3\text{V}$ ,  $V_{OUT2(NOM)} = 3.3\text{V}$ , Enable pins are tied to  $V_{IN}$ .

Line Transient,  $C_{BYP} = 10\text{nF}$

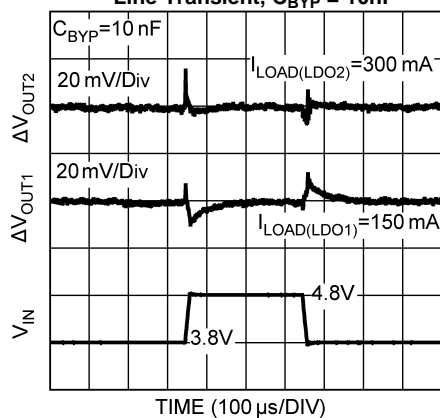


Figure 8.

Line Transient,  $C_{BYP} = 0$

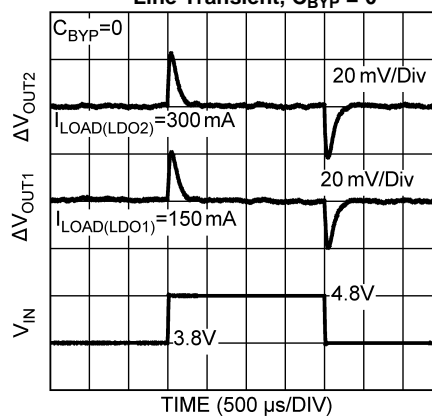


Figure 9.

Load Transient, LDO1

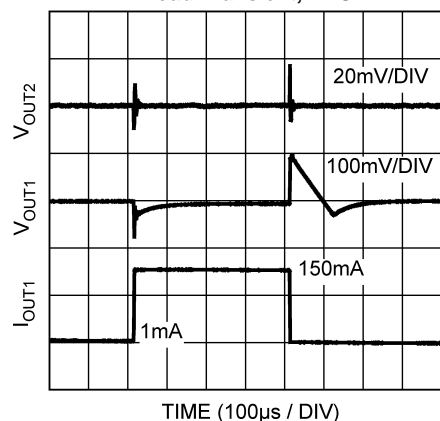


Figure 10.

Load Transient, LDO2

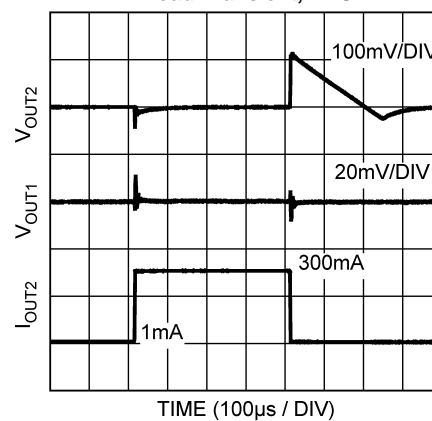


Figure 11.

Noise Density, LDO1

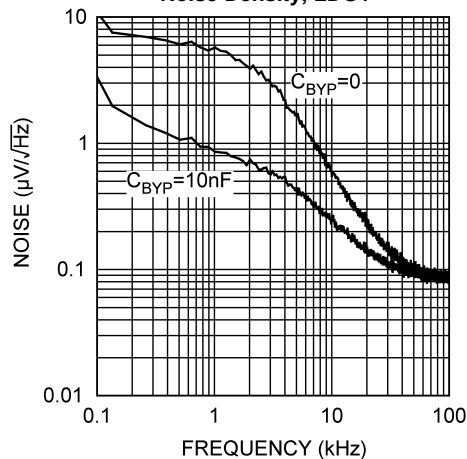


Figure 12.

Noise Density, LDO2

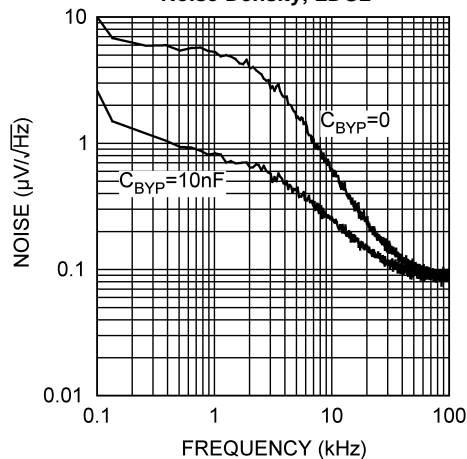
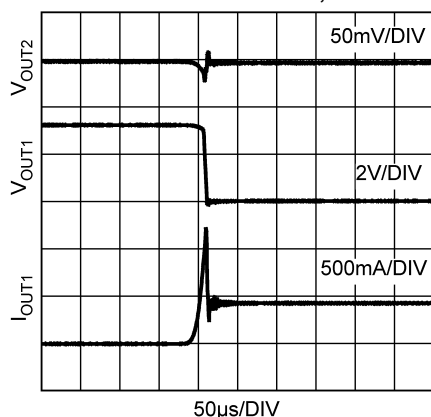


Figure 13.

### Typical Performance Characteristics. (continued)

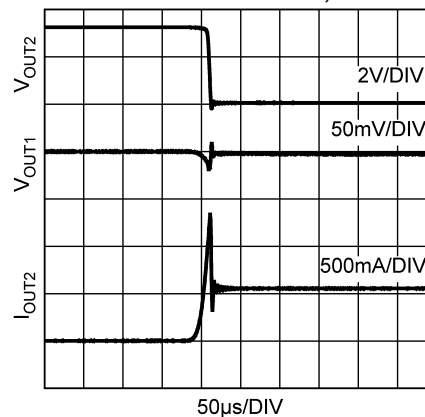
Unless otherwise specified,  $C_{IN} = 1.0\mu\text{F}$  Ceramic,  $C_{OUT1} = C_{OUT2} = 1.0\mu\text{F}$  Ceramic,  $C_{BYP} = 10\text{nF}$ ,  $V_{IN} = V_{OUT2(NOM)} + 1.0\text{V}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{OUT1(NOM)} = 3.3\text{V}$ ,  $V_{OUT2(NOM)} = 3.3\text{V}$ , Enable pins are tied to  $V_{IN}$ .

**Short Circuit Current, LDO1**



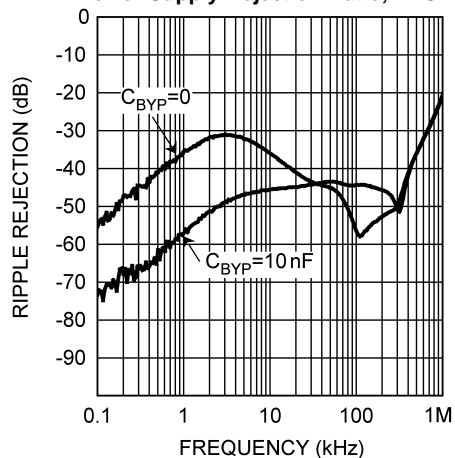
**Figure 14.**

**Short Circuit Current, LDO2**



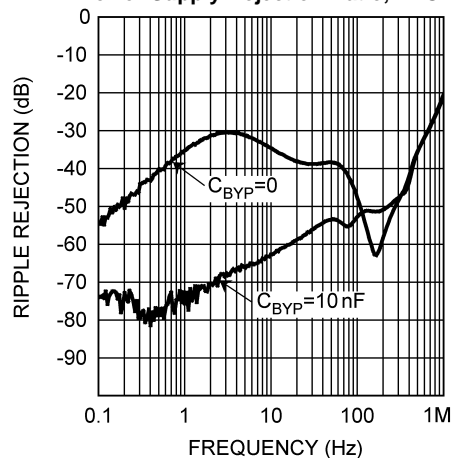
**Figure 15.**

**Power Supply Rejection Ratio, LDO1**



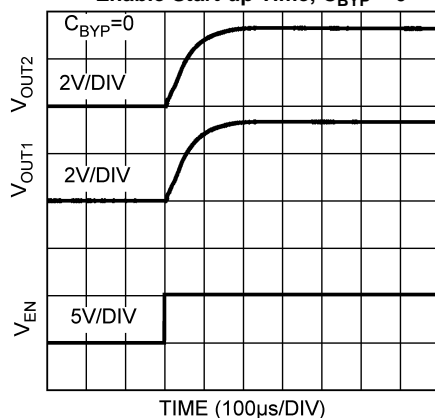
**Figure 16.**

**Power Supply Rejection Ratio, LDO2**



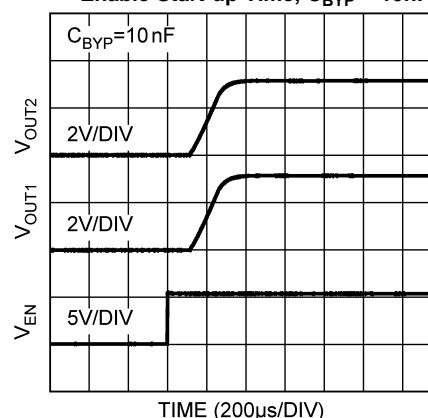
**Figure 17.**

**Enable Start-up Time,  $C_{BYP} = 0$**



**Figure 18.**

**Enable Start-up Time,  $C_{BYP} = 10\text{nF}$**



**Figure 19.**



## APPLICATION HINTS

### OPERATION DESCRIPTION

The LP5996 is a low quiescent current, power management IC, designed specifically for portable applications requiring minimum board space and smallest components. The LP5996 contains two independently selectable LDOs. The first is capable of sourcing 150mA at outputs between 0.8V and 3.3V. The second can source 300mA at an output voltage of 0.8V to 3.3V.

### INPUT CAPACITOR

An input capacitor is required for stability. It is recommended that a 1.0 $\mu$ F capacitor be connected between the LP5996 input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

**Important:** Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain approximately 1.0 $\mu$ F over the entire operating temperature range.

### OUTPUT CAPACITOR

The LP5996 is designed specifically to work with very small ceramic output capacitors. A 1.0 $\mu$ F ceramic capacitor (temperature types Z5U, Y5V or X7R) with ESR between 5m $\Omega$  to 500m $\Omega$ , is suitable in the LP5996 application circuit.

For this device the output capacitor should be connected between the  $V_{OUT}$  pin and ground.

It is also possible to use tantalum or film capacitors at the device output,  $C_{OUT}$  (or  $V_{OUT}$ ), but these are not as attractive for reasons of size and cost (see the section Capacitor Characteristics).

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5m $\Omega$  to 500m $\Omega$  for stability.

### NO-LOAD STABILITY

The LP5996 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

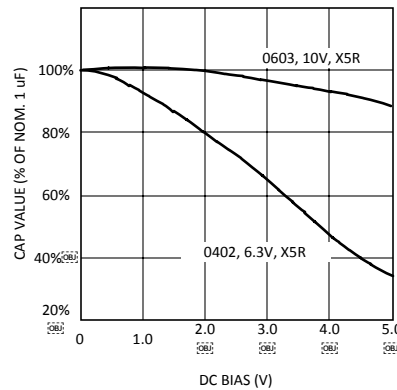
### CAPACITOR CHARACTERISTICS

The LP5996 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47 $\mu$ F to 4.7 $\mu$ F, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1.0 $\mu$ F ceramic capacitor is in the range of 20m $\Omega$  to 40m $\Omega$ , which easily meets the ESR requirement for stability for the LP5996.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, [Figure 20](#) shows a typical graph comparing different capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, increasing the DC Bias condition can result

in the capacitance value falling below the minimum value given in the recommended capacitor specifications table ( $0.7\mu\text{F}$  in this case). Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.



**Figure 20. Graph Showing a Typical Variation in Capacitance vs DC Bias**

The capacitance value of ceramic capacitors varies with temperature. The capacitor type X7R, which operates over a temperature range of  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , will only vary the capacitance to within  $\pm 15\%$ . The capacitor type X5R has a similar tolerance over a reduced temperature range of  $-55^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . Many large value ceramic capacitors, larger than  $1\mu\text{F}$  are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from  $25^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below  $25^{\circ}\text{C}$ .

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the  $0.47\mu\text{F}$  to  $4.7\mu\text{F}$  range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from  $25^{\circ}\text{C}$  down to  $-40^{\circ}\text{C}$ , so some guard band must be allowed.

## ENABLE CONTROL

The LP5996 features active high enable pins for each regulator, EN1 and EN2, which turns the corresponding LDO off when pulled low. The device outputs are enabled when the enable pins are set to high. When not enabled the regulator output is off and the device typically consumes 2nA.

If the application does not require the Enable switching feature, one or both enable pins should be tied to  $V_{\text{IN}}$  to keep the regulator output permanently on.

To ensure proper operation, the signal source used to drive the enable inputs must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under  $V_{\text{IL}}$  and  $V_{\text{IH}}$ .

## BYPASS CAPACITOR

The internal voltage reference circuit of the LP5996 is connected to the  $C_{\text{BYP}}$  pin via a high value internal resistor. An external capacitor, connected to this pin, forms a low-pass filter which reduces the noise level on both outputs of the device. There is also some improvement in PSSR and line transient performance. Internal circuitry ensures rapid charging of the  $C_{\text{BYP}}$  capacitor during start-up. A 10nF, high quality ceramic capacitor with either NPO or COG dielectric is recommended due to their low leakage characteristics and low noise performance.

## SAFE AREA OF OPERATION

Due consideration should be given to operating conditions to avoid excessive thermal dissipation of the LP5996 or triggering its thermal shutdown circuit. When both outputs are enabled, the total power dissipation will be  $P_{D(LDO1)} + P_{D(LDO2)}$  where  $PD = (V_{IN} - V_{OUT}) \times I_{OUT}$  for each LDO

In general, device options which have a large difference in output voltage will dissipate more power with both outputs enabled, due to the input voltage required for the higher output voltage LDO. In such cases, especially at elevated ambient temperature, it may not be possible to operate both outputs at maximum current at the same time.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LP5996SD-0833	ACTIVE	WSON	DSC	10	1000	TBD	Call TI	Call TI	-40 to 85	L176B	<a href="#">Samples</a>
LP5996SD-0833/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L176B	<a href="#">Samples</a>
LP5996SD-1018/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L224B	<a href="#">Samples</a>
LP5996SD-1525	ACTIVE	WSON	DSC	10	1000	TBD	Call TI	Call TI	-40 to 85	L177B	<a href="#">Samples</a>
LP5996SD-1525/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L177B	<a href="#">Samples</a>
LP5996SD-1833/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L225B	<a href="#">Samples</a>
LP5996SD-2533/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L226B	<a href="#">Samples</a>
LP5996SD-2828	ACTIVE	WSON	DSC	10	1000	TBD	Call TI	Call TI	-40 to 85	L180B	<a href="#">Samples</a>
LP5996SD-2828/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L180B	<a href="#">Samples</a>
LP5996SD-3030	ACTIVE	WSON	DSC	10	1000	TBD	Call TI	Call TI	-40 to 85	L181B	<a href="#">Samples</a>
LP5996SD-3030/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L181B	<a href="#">Samples</a>
LP5996SD-3033	ACTIVE	WSON	DSC	10	1000	TBD	Call TI	Call TI	-40 to 85	L179B	<a href="#">Samples</a>
LP5996SD-3033/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L179B	<a href="#">Samples</a>
LP5996SD-3308	ACTIVE	WSON	DSC	10	1000	TBD	Call TI	Call TI	-40 to 85	L205B	<a href="#">Samples</a>
LP5996SD-3308/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L205B	<a href="#">Samples</a>
LP5996SD-3333	ACTIVE	WSON	DSC	10	1000	TBD	Call TI	Call TI	-40 to 85	L182B	<a href="#">Samples</a>
LP5996SD-3333/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L182B	<a href="#">Samples</a>
LP5996SDX-0833	ACTIVE	WSON	DSC	10	4500	TBD	Call TI	Call TI	-40 to 85	L176B	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LP5996SDX-0833/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L176B	<a href="#">Samples</a>
LP5996SDX-1018/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L224B	<a href="#">Samples</a>
LP5996SDX-1525	ACTIVE	WSON	DSC	10	4500	TBD	Call TI	Call TI	-40 to 85	L177B	<a href="#">Samples</a>
LP5996SDX-1525/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L177B	<a href="#">Samples</a>
LP5996SDX-1833/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L225B	<a href="#">Samples</a>
LP5996SDX-2533/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L226B	<a href="#">Samples</a>
LP5996SDX-2828	ACTIVE	WSON	DSC	10	4500	TBD	Call TI	Call TI	-40 to 85	L180B	<a href="#">Samples</a>
LP5996SDX-2828/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L180B	<a href="#">Samples</a>
LP5996SDX-3030	ACTIVE	WSON	DSC	10	4500	TBD	Call TI	Call TI	-40 to 85	L181B	<a href="#">Samples</a>
LP5996SDX-3030/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L181B	<a href="#">Samples</a>
LP5996SDX-3033	ACTIVE	WSON	DSC	10	4500	TBD	Call TI	Call TI	-40 to 85	L179B	<a href="#">Samples</a>
LP5996SDX-3033/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L179B	<a href="#">Samples</a>
LP5996SDX-3308	ACTIVE	WSON	DSC	10	4500	TBD	Call TI	Call TI	-40 to 85	L205B	<a href="#">Samples</a>
LP5996SDX-3308/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L205B	<a href="#">Samples</a>
LP5996SDX-3333	ACTIVE	WSON	DSC	10	4500	TBD	Call TI	Call TI	-40 to 85	L182B	<a href="#">Samples</a>
LP5996SDX-3333/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L182B	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Only one of markings shown within the brackets will appear on the physical device.

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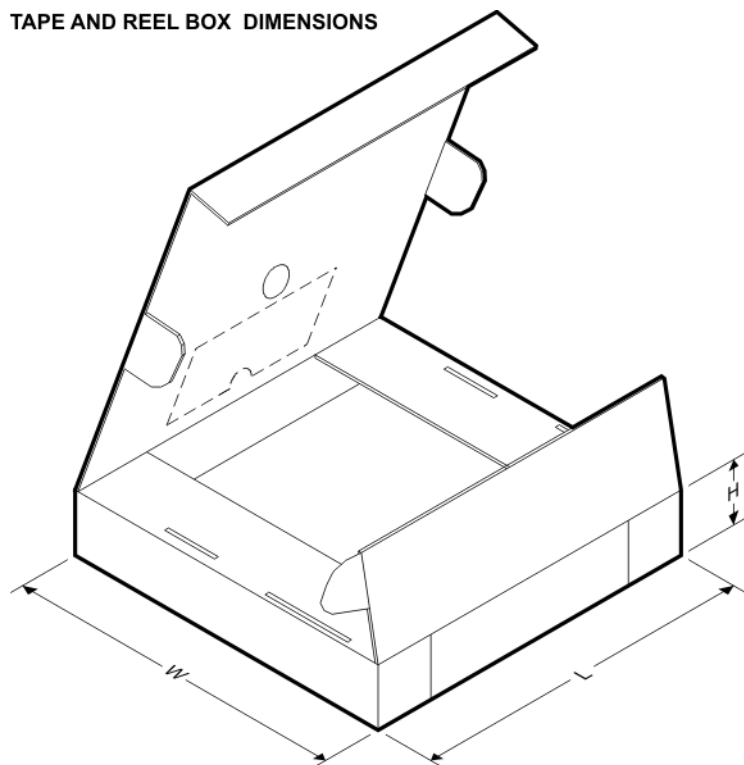
**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5996SD-0833	SON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SD-0833/NOPB	SON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SD-1018/NOPB	SON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SD-1525	SON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SD-1525/NOPB	SON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SD-1833/NOPB	SON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SD-2533/NOPB	SON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SD-2828	SON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SD-2828/NOPB	SON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SD-3030	SON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SD-3030/NOPB	SON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SD-3033	SON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SD-3033/NOPB	SON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SD-3308	SON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SD-3308/NOPB	SON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SD-3333	SON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SD-3333/NOPB	SON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SDX-0833	SON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5996SDX-0833/NOPB	SON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SDX-1018/NOPB	SON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SDX-1525	SON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SDX-1525/NOPB	SON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SDX-1833/NOPB	SON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SDX-2533/NOPB	SON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SDX-2828	SON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SDX-2828/NOPB	SON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SDX-3030	SON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SDX-3030/NOPB	SON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SDX-3033	SON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SDX-3033/NOPB	SON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SDX-3308	SON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SDX-3308/NOPB	SON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SDX-3333	SON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP5996SDX-3333/NOPB	SON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



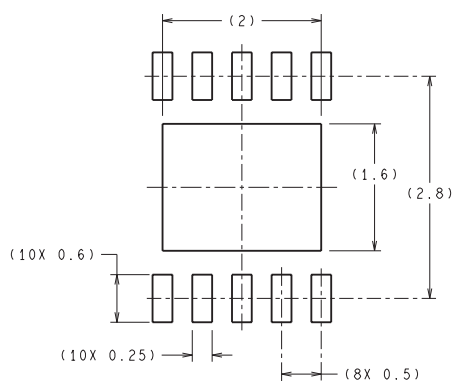
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5996SD-0833	SON	DSC	10	1000	203.0	190.0	41.0

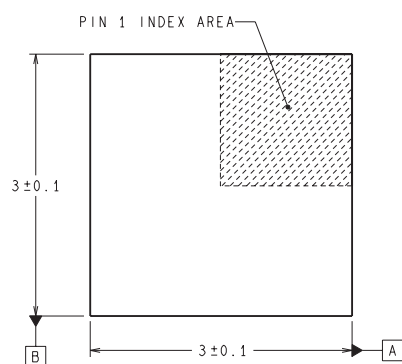


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5996SD-0833/NOPB	SON	DSC	10	1000	203.0	190.0	41.0
LP5996SD-1018/NOPB	SON	DSC	10	1000	203.0	190.0	41.0
LP5996SD-1525	SON	DSC	10	1000	203.0	190.0	41.0
LP5996SD-1525/NOPB	SON	DSC	10	1000	203.0	190.0	41.0
LP5996SD-1833/NOPB	SON	DSC	10	1000	203.0	190.0	41.0
LP5996SD-2533/NOPB	SON	DSC	10	1000	203.0	190.0	41.0
LP5996SD-2828	SON	DSC	10	1000	203.0	190.0	41.0
LP5996SD-2828/NOPB	SON	DSC	10	1000	203.0	190.0	41.0
LP5996SD-3030	SON	DSC	10	1000	203.0	190.0	41.0
LP5996SD-3030/NOPB	SON	DSC	10	1000	203.0	190.0	41.0
LP5996SD-3033	SON	DSC	10	1000	203.0	190.0	41.0
LP5996SD-3033/NOPB	SON	DSC	10	1000	203.0	190.0	41.0
LP5996SD-3308	SON	DSC	10	1000	203.0	190.0	41.0
LP5996SD-3308/NOPB	SON	DSC	10	1000	203.0	190.0	41.0
LP5996SD-3333	SON	DSC	10	1000	203.0	190.0	41.0
LP5996SD-3333/NOPB	SON	DSC	10	1000	203.0	190.0	41.0
LP5996SDX-0833	SON	DSC	10	4500	349.0	337.0	45.0
LP5996SDX-0833/NOPB	SON	DSC	10	4500	349.0	337.0	45.0
LP5996SDX-1018/NOPB	SON	DSC	10	4500	349.0	337.0	45.0
LP5996SDX-1525	SON	DSC	10	4500	349.0	337.0	45.0
LP5996SDX-1525/NOPB	SON	DSC	10	4500	349.0	337.0	45.0
LP5996SDX-1833/NOPB	SON	DSC	10	4500	349.0	337.0	45.0
LP5996SDX-2533/NOPB	SON	DSC	10	4500	349.0	337.0	45.0
LP5996SDX-2828	SON	DSC	10	4500	349.0	337.0	45.0
LP5996SDX-2828/NOPB	SON	DSC	10	4500	349.0	337.0	45.0
LP5996SDX-3030	SON	DSC	10	4500	349.0	337.0	45.0
LP5996SDX-3030/NOPB	SON	DSC	10	4500	349.0	337.0	45.0
LP5996SDX-3033	SON	DSC	10	4500	349.0	337.0	45.0
LP5996SDX-3033/NOPB	SON	DSC	10	4500	349.0	337.0	45.0
LP5996SDX-3308	SON	DSC	10	4500	349.0	337.0	45.0
LP5996SDX-3308/NOPB	SON	DSC	10	4500	349.0	337.0	45.0
LP5996SDX-3333	SON	DSC	10	4500	349.0	337.0	45.0
LP5996SDX-3333/NOPB	SON	DSC	10	4500	349.0	337.0	45.0

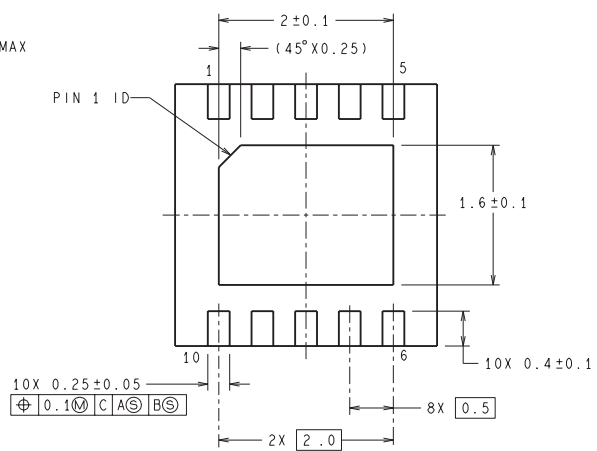
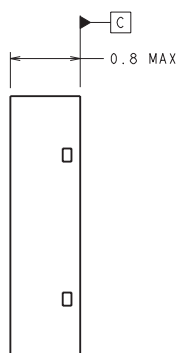
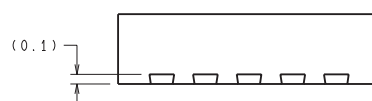
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