

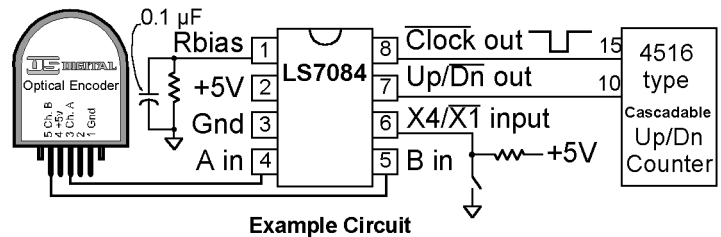
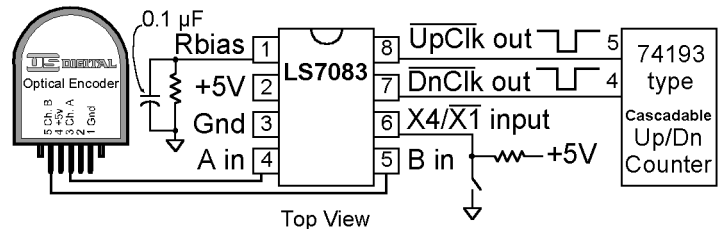
Quadrature Clock Converters

Features:

- X4 or X1 resolution multiplication
- TTL and CMOS compatible
- Low power (micro-amps)
- 8-pin DIP or SOIC package
- No external clocks required
- Drive standard Up/Dn counters
- Monolithic CMOS
- U.S. Digital warrants its products against defects in materials and workmanship for two years. See complete warranty for details.

Description:

These devices allow incremental shaft encoders to drive standard up/down counters. Connect the encoder quadrature outputs to the A & B inputs. The LS7083 outputs can connect directly to the up and down clock inputs of counters such as 74193 or 40193. The LS7084 outputs can connect directly to the Clock and Up/Dn inputs of counters such as 4516 or 74169.



Pin Descriptions

Pin 1 (Rbias input):

Connect a 0.1 μF bypass capacitor and resistor to ground for the internal current mirror which feeds the two internal 2-axis one-shots. The resistor value sets the width of the low-true clock outputs. A typical value is 300kOhm which sets the output pulse width to 1 μs and max A,B frequency to 250kHz. Minimum resistor value is 50kOhm. See the Rbias table (next page) for other values. The chip's current consumption is inversely proportional to this resistance. Typical current is 40 μA @ 100kOhm and 6 μA @ 2MegOhm.

Pins 4 & 5 (A & B inputs):

Connect to the A & B quadrature outputs of the encoder. Both inputs have debounce filters. Minimum pulse width is set at 160ns. There is no maximum limit. Input current is less than 1 μA . The A&B inputs can be swapped to reverse the direction of the external counters.

Pin 6 (X4/X1 input):

A high level applied to this input selects X4 mode, a low level selects the X1 mode. Input current is less than 1 μA . Do not let this input float. In X4 mode, a clock pulse is generated for every transition of the A or B input. Note that there are 4 transitions per cycle of quadrature code. Thus, a 500 cycle/rev encoder will produce 2000 counts/rev in X4 mode. In X1 mode, only one clock is generated per quadrature cycle.

LS7083 pin 7 (Down Clock output):

Normally high, low-true. The low level pulse width is set by pin 1. Down counts are enabled only when B leads A (clockwise rotation). In X4 mode, one pulse is generated for each A/B state change. In X1 mode, one pulse is generated per quadrature cycle.

LS7084 pin 7 (Up/Down Clock output):

This output steers the external counter up or down. High = Up (A leads B), Low = Down (B leads A).

LS7083 pin 8 (Up Clock output):

Normally high, low-true. The low level pulse width is set by pin 1. Up counts are enabled only when A leads B (counter-clockwise rotation). In X4 mode, one pulse is generated for each A/B state change. In X1 mode, one pulse is generated per quadrature cycle.

LS7084 pin 8 (Clock output):

Normally high, low-true. The low level pulse width is set by pin 1. In X4 mode, one pulse is generated for each A/B state change regardless of count direction. In X1 mode, one pulse is generated per quadrature cycle. The external counter should count on the rising (high-going) edge of this output.

Surface Mount Package:

The 8-pin SOIC package has the same pin-out as the DIP version shown above.

Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Operating Temperature	0	70	°C
Storage Temperature	-65	150	°C
Voltage at any input	-.5	VCC+.5	Volts
Supply Voltage (Vcc)		10.5	Volts

Rbias Resistor Value vs Timing

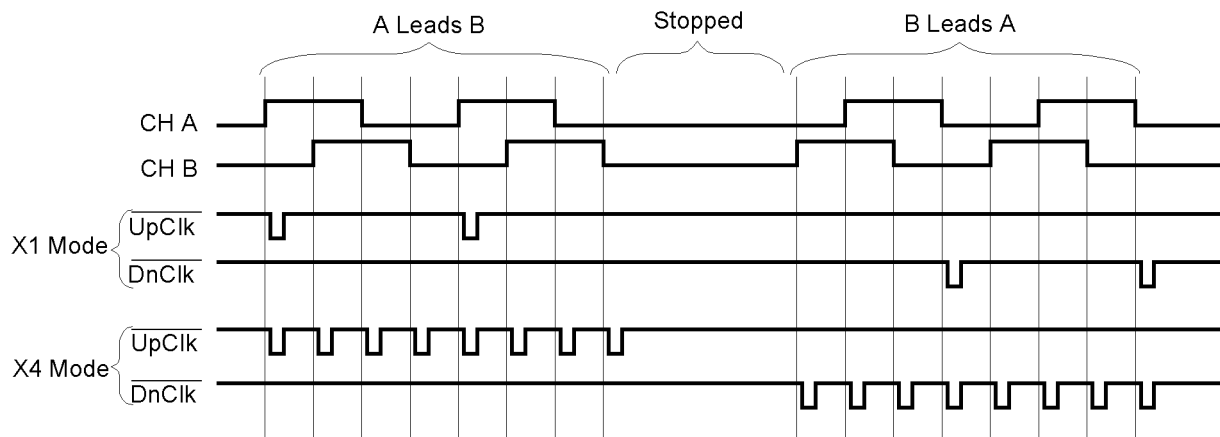
Resistor	Pulse Width	Max A,B Freq
100kOhm	400ns	625kHz
300kOhm	1µs	250kHz
500kOhm	1.4µs	180kHz
2MegOhm	5µs	50kHz
10MegOhm	25µs	10kHz

DC Electrical Characteristics for 5v Operation

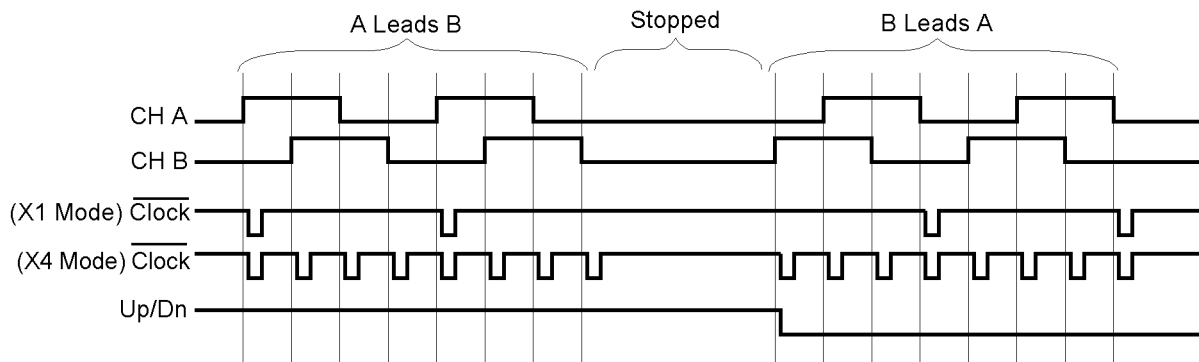
Parameter	Min.	Max.	Units	Notes
Supply Voltage	4.75	10.5	Volts	
Supply Current	-	8	µA	A,B = 0Hz Rbias=300k
X4/X1 Logic Low		1.4	Volts	
X4/X1 Logic High	3.7		Volts	
A,B Logic Low		0.6	Volts	
A,B Logic High	3.3		Volts	
Low Output Current	1.75		mA	Vout = 0.4V
High Output Current	1.0		mA	Vout = 4.75V

Use standard CMOS levels when operating with higher supply voltages up to 10.5 Volts.

LS7083 Timing Diagram



LS7084 Timing Diagram



Timing Diagram Notes:

The maximum time delay from the A or B input to the leading edge of any output is 235ns.

The pulse width of all clock outputs is set by the value of the Rbias resistor as shown in the table above.

Typical rise or fall time of each logic output 10 to 20 ns.

- Purchase orders may be scheduled out over a 12 month period to receive a higher quantity discounted price.
- Typically orders are shipped same day or next day.

DIP Package (600mil)
LS7083 & LS7084

Price:
\$3.05 / 1
\$2.45 / 25
\$1.95 / 100
\$1.65 / 500
\$1.40 / 1K
\$1.20 / 5K
\$1.02 / 10K

SOIC Package
LS7083-S & LS7084-S

Price:
\$3.60 / 1
\$2.90 / 25
\$2.30 / 100
\$1.95 / 500
\$1.65 / 1K
\$1.35 / 5K
\$1.13 / 10K

All information subject to change without notice.

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