LTC4300-1

Hot Swappable 2-Wire Bus Buffer

March 2001

FEATURES

- **Bidirectional Buffer for SDA and SCL Lines**
- **Prevents SDA and SCL Corruption During Live Board Insertion and Removal from Backplane**
- Ability to Isolate Input SDA and SCL Lines from Output
- Compatible with I²C™, I²C Fast Mode and SMBus Standards
- Small MSOP 8-Pin Package
- dV/dt Rise Time Accelerators on all SDA and SCL Lines
- Low I_{CC} Chip Disable: <1µA
- READY Open Drain Output
- 1V Precharge on all SDA and SCL Lines

APPLICATIONS

- Hot Board Insertion
- Servers
- Capacitance Buffer/Bus Extender
- Desktop Computer

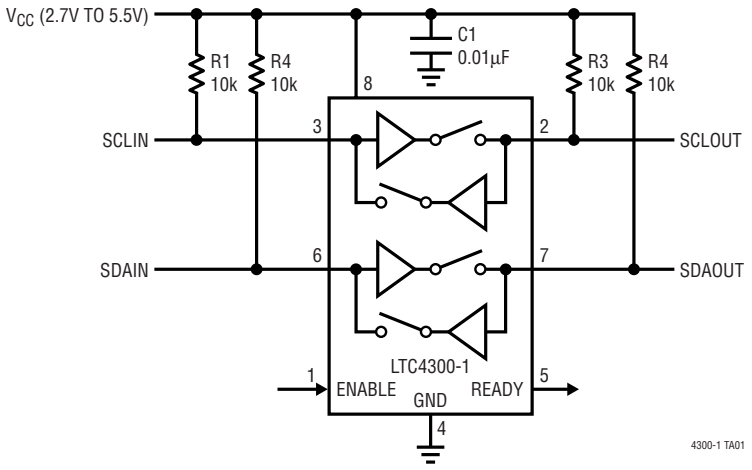
DESCRIPTION

The LTC®4300-1 hot swappable 2-wire bus buffer allows I/O card insertion into a live backplane without corruption of the data and clock busses. Control circuitry prevents the backplane from being connected to the card until a stop bit or bus idle occurs on the backplane without bus contention on the card. When the connection is made, the LTC4300-1 provides bidirectional buffering, keeping the backplane and card capacitances isolated.

Rise time accelerator circuitry allows the use of weaker DC pull-up currents while still meeting rise time requirements. During insertion, the SDA and SCL lines are precharged to 1V to minimize the current required to charge the parasitic capacitance of the chip. The LTC4300-1 incorporates a digital ENABLE input pin, which forces the part into a low current mode when asserted low, and an open drain READY output pin, which indicates that the backplane and card sides are connected together.

The LTC4300-1 is available in a small 8-pin MSOP package.

TYPICAL APPLICATION

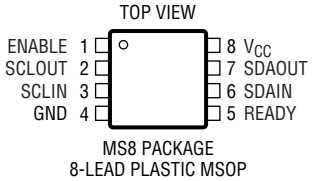


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} to GND ..... –0.5 to 7V
SDAIN, SCLIN, SDAOUT, SCLOUT
READY, ENABLE ..... –0.5 to 7V
Operating Temperature Range
LTC4300-1C ..... 0°C to 70°C
LTC4300-1I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 200°C/W

ORDER PART NUMBER
LTC4300-1CMS8 LTC4300-1IMS8
MS8 PART MARKING
LTUB LTUC

Consult factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range. V_{CC} = 2.7V to 5.5V, $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{CC}	Positive Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.5V, $V_{SDAIN} = V_{SCLIN}$ = 0V	●		2.8	6	mA
I_{SD}	Supply Current in Shutdown Mode	V_{ENABLE} = 0V			0.1		µA
Start-Up Circuitry							
V_{PRE}	Precharge Voltage	SDA, SCL Floating	●	0.8	1.0	1.2	V
t_{IDLE}	Bus Idle Time		●	50	75		µs
V_{OL}	READY Output Low Voltage	I_{PULLUP} = 3mA	●			0.4	V
Rise Time Accelerators							
$I_{PULLUPAC}$	Transient Boosted Pull-Up Current	Positive Transition on SDA,SCL, V_{CC} = 2.7V Slew Rate = 1.25V/µs, Note 2		1	2		mA
Input-Output Connection							
V_{OS}	Input-Output Offset Voltage	10k to V_{CC} on SDA, SCL, V_{CC} = 3.3V, Note 3	●	0	75	150	mV
$F_{SCL, SDA}$	Operating Frequency	Guaranteed by Design, Not Subject to Test		0		400	kHz
C_{IN}	Digital Input Capacitance	Guaranteed by Design, Not Subject to Test				10	pF
V_{OL}	Output Low Voltage, Input = 0V	SDA, SCL Pins, I_{SINK} = 3mA, V_{CC} = 2.7V	●	0		0.4	V
I_{LEAK}	Input Leakage Current	SDA, SCL Pins = V_{CC} = 5.5V				±5	µA

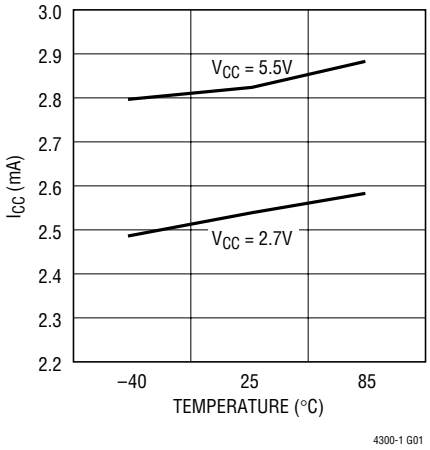
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired

Note 2: $I_{PULLUPAC}$ varies with temperature and V_{CC} voltage, as shown in the Typical Performance Characteristics section.

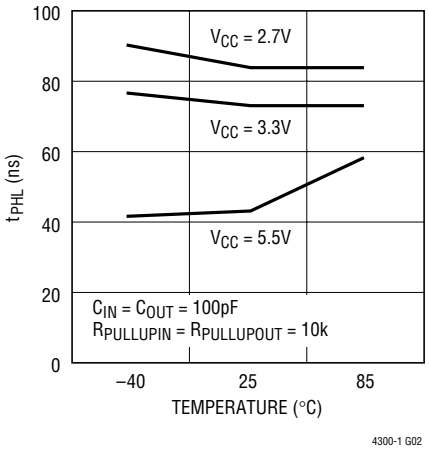
Note 3: The connection circuitry always regulates its output to a higher voltage than its input. The magnitude of this offset voltage as a function of the pullup resistor and V_{CC} voltage is shown in the Typical Performance Characteristics section.

TYPICAL PERFORMANCE CHARACTERISTICS

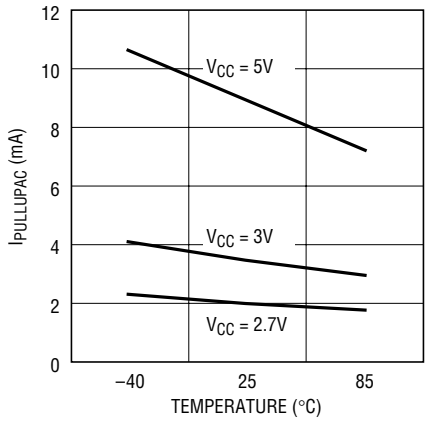
I_{CC} vs Temperature



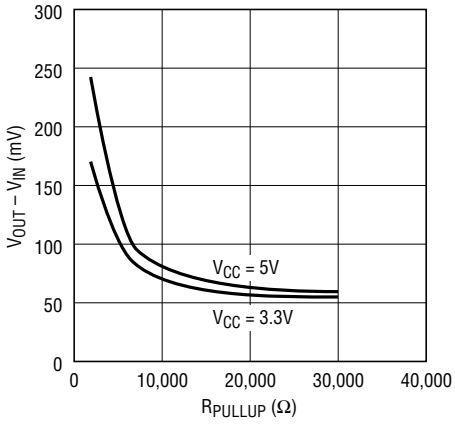
Input – Output t_{PHL} vs Temperature



$I_{PULLUPAC}$ vs Temperature



Connection Circuitry $V_{OUT} – V_{IN}$



PIN FUNCTIONS

ENABLE (Pin 1): Chip Enable Pin. Grounding this pin puts the part in a low current (<1μA) mode. It also disables the rise time accelerators, isolates SDAIN from SDAOUT and isolates SCLIN from SCLOUT.

SCLOUT (Pin 2): Serial Clock Output. Connect this pin to the SCL bus on the card.

SCLIN (Pin 3): Serial Clock Input. Connect this pin to the SCL bus on the backplane.

GND (Pin 4): Ground. Connect this pin to a ground plane for best results.

READY (Pin 5): This is an open-drain output which pulls low when SDAIN and SCLIN are disconnected from SDAOUT and SCLOUT, and turns off when the two sides are connected. Connect a 10k resistor from this pin to V_{CC} to provide the pull up.

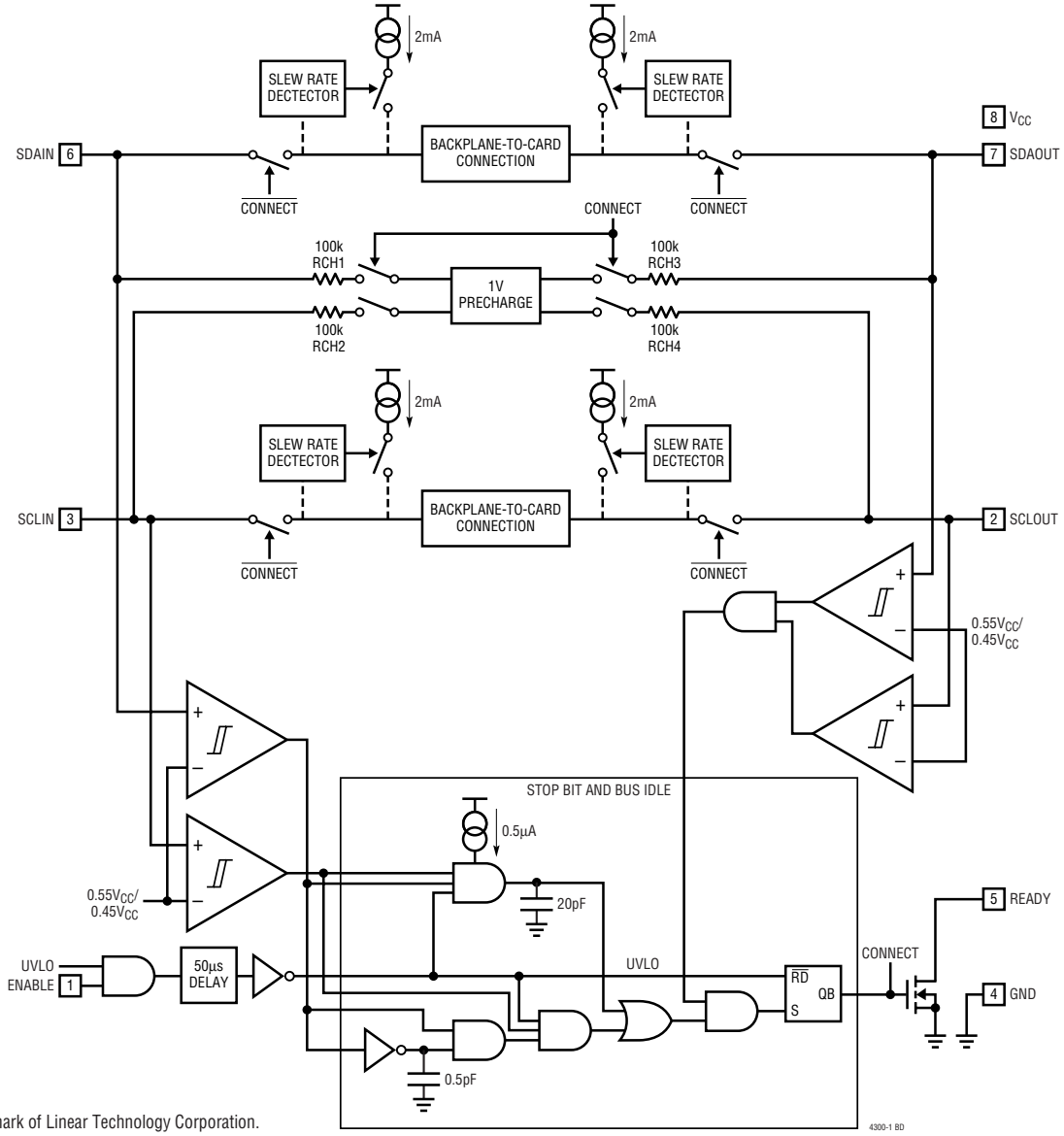
SDAIN (Pin 6): Serial Data Input. Connect this pin to the SDA bus on the backplane.

SDAOUT (Pin 7): Serial Data Output. Connect this pin to the SDA bus on the card.

V_{CC} (Pin 8): Main Input Power Supply. Place a bypass capacitor of at least 0.01μF close to this pin for best results.

BLOCK DIAGRAM

2-Wire Bus Buffer and Hot Swap™ Controller



Hot Swap is a trademark of Linear Technology Corporation.

OPERATION

Input to Output Connection

The LTC4300-1 allows I/O card insertion into a live backplane without corruption of the data and clock lines (SDA and SCL). In its main application, the LTC4300-1 resides on the edge of a peripheral card, with the SCLOUT pin connected to the card's SCL bus and the SDAOUT pin connected to the card's SDA bus. When the card is plugged into a live backplane via a staggered connector, ground makes connection first, followed by V_{CC}. The part starts in an undervoltage lockout (UVLO) state, ignoring any activity on the SDA and SCL pins until V_{CC} rises above 2.5V. This ensures that the part does not try to function until it has enough voltage to do so.

During this time, the 1V precharge circuitry is also active and forces 1V through 100k nominal resistors to the SDA and SCL pins. This concept of initializing the SDA and SCL

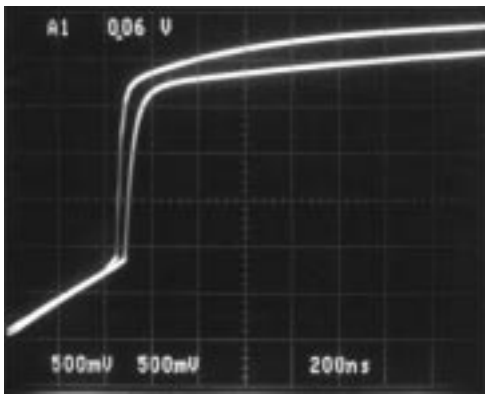
OPERATION

pins before they make contact with a live backplane is described in and required by the CompactPCI™ specification. Because the I/O card is being plugged into a live backplane, the voltage on the backplane SDA and SCL busses may be anywhere between 0V and V_{CC}. Precharging the SCL and SDA pins to 1V minimizes the worst-case voltage differential these pins will see at the moment of connection, therefore minimizing the amount of disturbance caused by the I/O card.

After ground and V_{CC} connect, SDAIN and SCLIN make connection with the backplane SDA and SCL lines. Once the part comes out of UVLO, it looks for either a stop bit or bus idle condition on the backplane side to indicate the completion of a data transaction. When either one occurs, the part also verifies that both the SDAOUT and SCLOUT voltages are high. When all of these conditions are met, the input-to-output connection circuitry is activated, joining the SDA and SCL busses on the I/O card with those on the backplane. The key feature of the connection circuitry is that it provides bidirectional buffering, keeping the backplane and card capacitances isolated.

Because of this isolation, the waveforms on the busses look slightly different from the corresponding waveforms on the card busses. This is true for both the rising and the falling edges. During a rising edge, for example, the rise time on each side is determined by the combined pull-up current of the LTC4300-1 boost current and the bus resistor and the equivalent capacitance on the line. If the pull-up currents are the same, a difference in rise time occurs which is directly proportional to the difference in capacitance between the two sides. This effect is displayed in Figure 1 for V_{CC} = 3.3V and a 10k pull-up resistor on each side (10pF on one side and 100pF on the other).

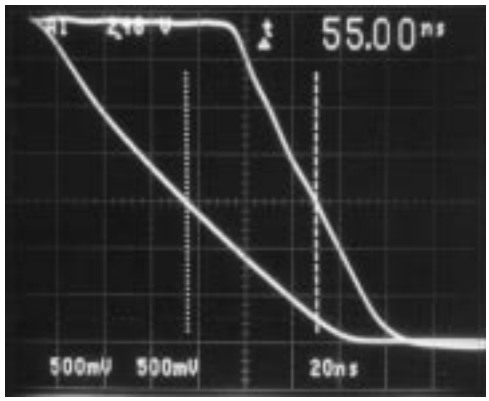
There is a finite propagation delay through the connection circuitry for falling waveforms. Figure 2 shows the falling edge waveforms for the same V_{CC}, pull-up resistors and equivalent capacitance conditions as used in Figure 1. An external NMOS device pulls down the voltage on the side with 100pF capacitance; the LTC4300-1 pulls down the voltage on the opposite side, with a delay of 55ns. This delay is always positive and is a function of supply voltage and temperature, as shown in the Typical Performance Characteristics section. The delay is also a function of the pull-up resistors and the equivalent bus capacitances on both sides of the bus and can become as large as 150ns. Users must account for the difference in propagation time for a rising edge vs a falling edge when determining setup and hold times for their systems.



OUTPUT SIDE 10pF

INPUT SIDE 100pF

Figure 1. Input–Output Connection t_{PLH}



INPUT SIDE 100pF

OUTPUT SIDE 10pF

Figure 2. Input–Output Connection t_{PHL}

CompactPCI is a trademark of the PCI Industrial Computer Manufacturers Group.

OPERATION

Rise Time Accelerators

Once connection has been established, rise time accelerator circuits on all four SDA and SCL pins are activated. These allow the user to choose weaker DC pull-up currents on the bus, reducing power consumption while still meeting system rise time requirements. During positive bus transitions, the LTC4300-1 switches in 2mA of current to quickly slew the SDA and SCL lines once their DC voltages exceed 0.6V. Using a rule of thumb of 20pF of capacitance for every device on the bus (10pF for the device and 10pF for interconnect), choose a pull-up current so that the bus will rise on its own at a rate of at least 1.25V/µs to guarantee activation of the accelerators.

For example, assume an SMBus system with V_{CC} = 3V, a 10k pull-up resistor and equivalent bus capacitance of 200pF. The rise time of an SMBus system is calculated from ($V_{IL(MAX)}$ – 0.15V) to ($V_{IH(MIN)}$ + 0.15V), or 0.65V to 2.25V. It takes an RC circuit 0.62 time constants to traverse this voltage for a 3V supply; in this case, 0.62 • (10k • 200pF) = 1.24µs. Thus, the system exceeds the maximum allowed rise time of 1µs by 24%. However, using the rise time accelerators, which are activated at a DC threshold of below 0.65V, the worst-case rise time is: (2.25V – 0.65V) • 200pF/1mA = 320ns, which meets the 1µs rise time requirement.

READY Digital Output

This pin provides a digital flag which is low when the backplane and I/O card are disconnected and is high when they are connected. The pin is driven by an open drain pull-down capable of sinking 3mA while holding 0.4V on the pin. Connect a resistor of 10k to V_{CC} to provide the pull-up.

ENABLE Low Current Disable

Grounding the ENABLE pin disconnects the backplane side from the card side, disables the rise time accelerators and puts the part in a near-zero current state. When the pin is brought back high, the part waits for data transactions on both the backplane and card sides to be complete (as described in "Input to Output Connection" above) before reconnecting the two sides.

APPLICATIONS INFORMATION

Multiple I/O Cards Plugging into a Backplane

The application shown in Figure 3 highlights the capacitance buffering feature of the LTC4300-1. If the I/O cards were plugged directly into the backplane, all of the backplane and card capacitances would add directly together, making rise and fall time requirements difficult to meet. Placing a LTC4300-1 on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the LTC4300-1 drives the capacitance of everything on the card and the backplane must drive only the capacitance of the LTC4300-1, which is less than 10pF.

Repeater/Bus Extender Application

Users who wish to connect two 2-wire systems separated by a distance can do so by connecting two LTC4300-1s back-to-back, as shown in Figure 4. The I^2C specification allows for 400pF maximum bus capacitance, severely limiting the length of the bus. The SMBus specification places no restriction on bus capacitance, but the limited impedances of devices connected to the bus require systems to remain small if rise and fall time specifications are to be met. The strong pull-up and pull-down impedances of the LTC4300-1 are capable of meeting rise and fall time specifications for several nanofarads of capacitance, thus allowing much more interconnect distance. In this situation, the differential ground voltage between the two systems may limit the allowed distance, because a valid logic low voltage with respect to the ground at one end of the system may violate the allowed V_{OL} specification with respect to the ground at the other end. In addition, the connection circuitry offset voltages of the back-to-back LTC4300-1s add together, directly contributing to the same problem.

APPLICATIONS INFORMATION

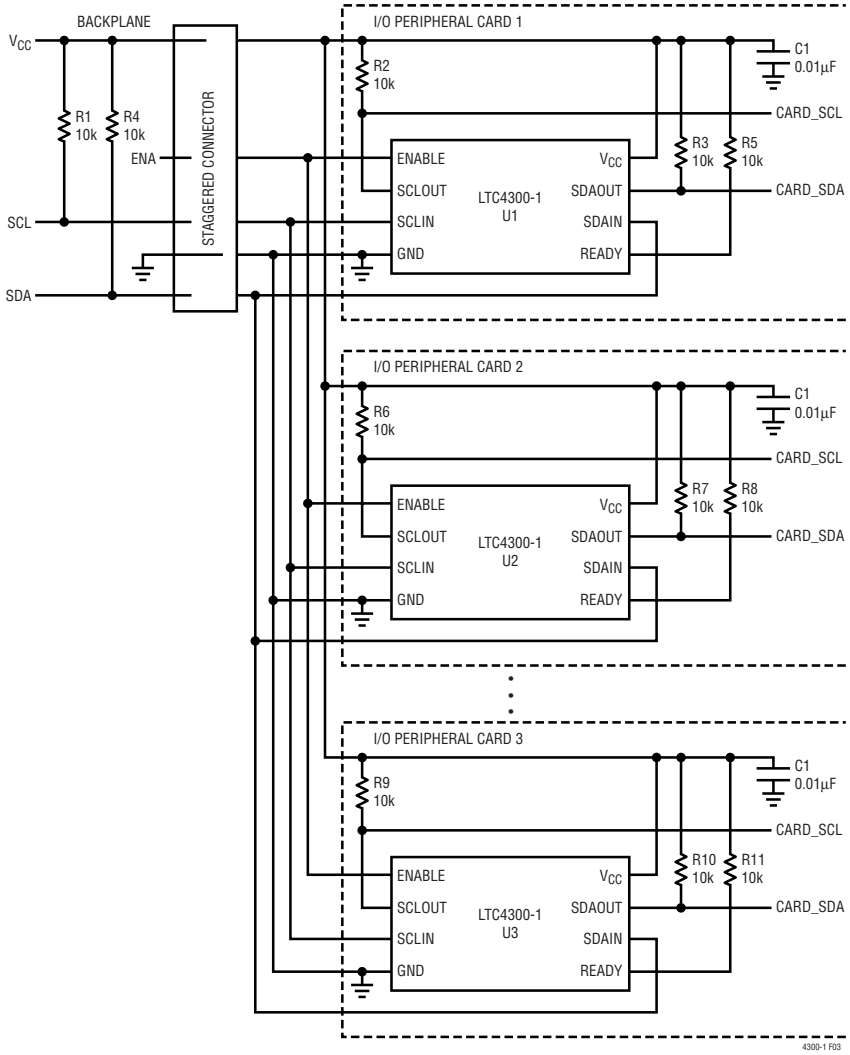


Figure 3. Multiple I/O Cards Plugging into a Backplane

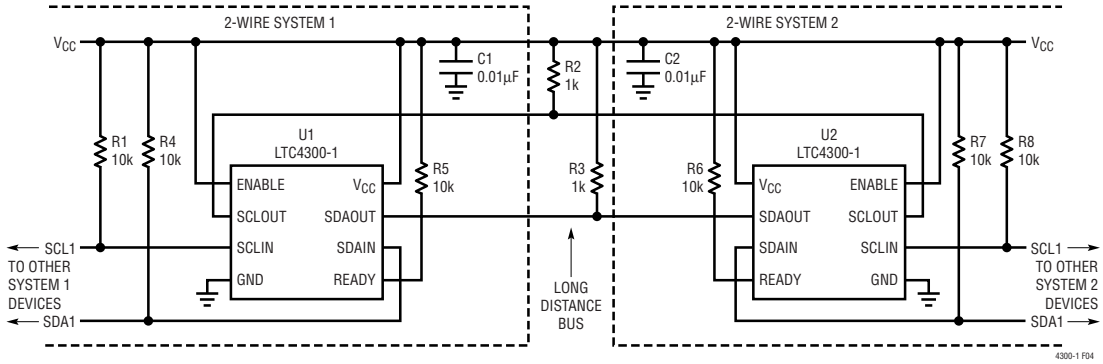
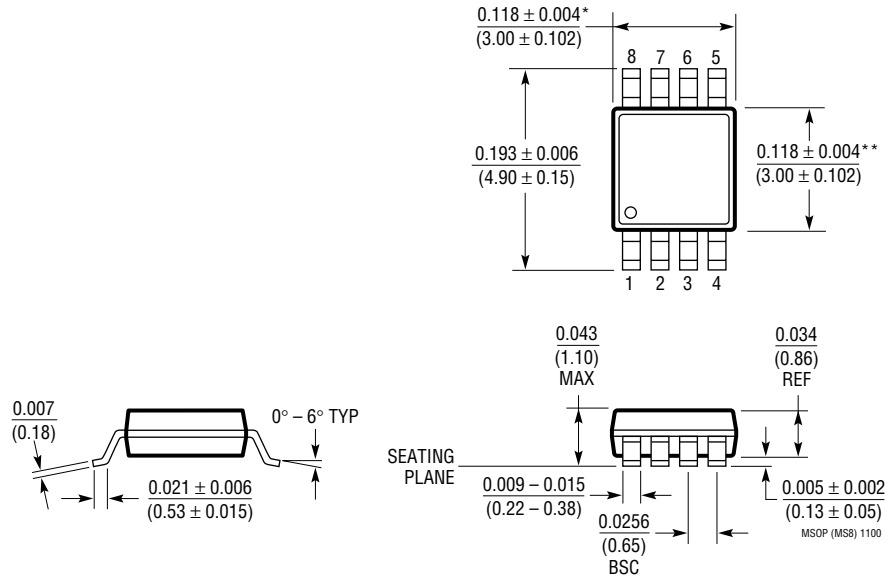


Figure 4. Repeater/Bus Extender Application

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise specified.

MS8 Package
8-Lead Plastic MSOP
(LTC DWG # 05-08-1660)



* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1380/LTC1393	Single-Ended 8-Channel/Differential 4-Channel Analog Mux with SMBus Interface	Low R_{ON}: 35Ω Single-Ended/70Ω Differential, Expandable to 32 Single or 16 Differential Channels
LTC1427-50	Micropower, 10-Bit Current Output DAC with SMBus Interface	Precision 50μA ± 2.5% Tolerance Over Temperature, 4 Selectable SMBus Addresses, DAC Powers up at Zero or Midscale
LTC1623	Dual High Side Switch Controller with SMBus Interface	8 Selectable Addresses/16-Channel Capability
LTC1663	SMBus Interface 10-Bit Rail-to-Rail Micropower DAC	DNL < 0.75LBS Max, 5-Lead SOT-23 Package
LTC1694/LTC1694-1	SMBus Accelerator	Improved SMBus/I^2C Rise Time, Ensures Data Integrity with Multiple SMBus/I^2C Devices
LT1786F	SMBus Controlled CCFL Switching Regulator	1.25A, 200kHz, Floating or Grounded Lamp Configurations
LTC1695	SMBus/I2C Fan Speed Controller in SOT-23	0.75Ω PMOS 180mA Regulator, 6-Bit DAC

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