



# LV3400M

## FM Multiplex Filter

### Overview

The LV3400M is a filter IC designed for FM multiplex broadcast reception and is used in combination with the Sanyo LC72700 demodulation/error correction IC. The adoption of switched capacitor (SCF) technology means that frequency adjustment is not required and that the LV3400M provides stable operation.

### Functions

- 76 kHz band-pass filter (Gaussian filter)
- 54 kHz high-pass filter
- 125 kHz low-pass filter
- Anti-aliasing filter
- Limiter circuit

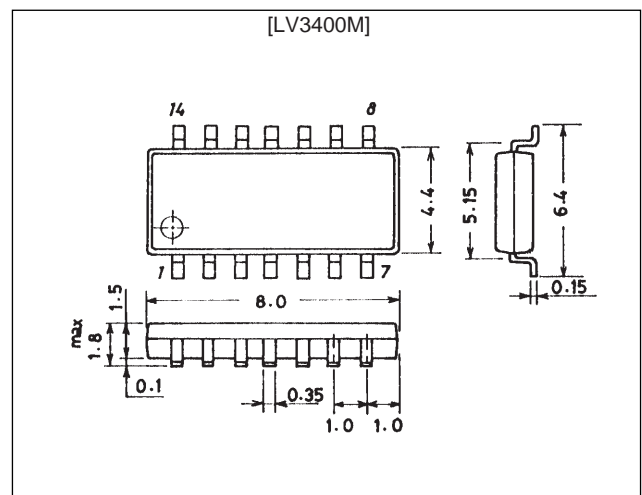
### Features

- Adjustment-free, due to the use of SCF technology.
- Few external components are required.

### Package Dimensions

unit: mm

#### 3111-MFP14S



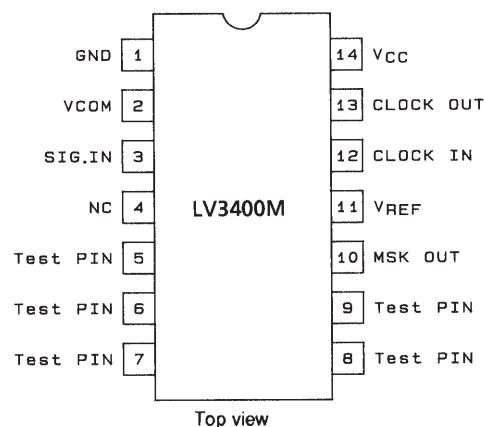
SANYO: MFP14S

### Specifications

#### Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>CC</sub> max		6	V
Maximum input voltage	V <sub>3</sub> , V <sub>7</sub> , V <sub>12</sub>		-0.3 to V <sub>CC</sub> + 0.3	V
Allowable power dissipation	P <sub>d</sub> max		180	mW
Operating temperature	T <sub>opr</sub>		-40 to +85	°C
Storage temperature	T <sub>stg</sub>		-55 to +125	°C

### Pin Assignment



Top view

A05604

## LV3400M

### Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Operating supply voltage range	$V_{CC}$		4.5 to 5.5	V
Input signal voltage range	$V_{IN}$	A composite signal corresponding to a 100% FM modulation level	200 to 300	mVrms
		$f_{IN} = 76\text{ kHz, CW}$	8 to 30	mVrms
Clock frequency	$f_{CK}$		3.60	MHz
Clock input voltage	$V_{CK}$		1.0 to $V_{CC}$	Vp-p

### Operating Characteristics at $T_a = 25^\circ\text{C}$ , $V_{CC} = 5\text{ V}$ , $f_{CK} = 3.6\text{ MHz}$ , $V_{CK} = 1\text{ Vp-p}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain	$I_{CCO}$	The pin 14 current for a no-signal input to $V_{IN}$	3.8	6	8	mA
SCF block common voltage	$V_2$	The pin 2 voltage for a no-signal input to $V_{IN}$	2.1	2.3	2.5	V
Signal input resistance	$R_{in3}$	The pin 3 input resistance		36		k $\Omega$
Clock input resistance	$R_{in12}$	The pin 12 input resistance		100		k $\Omega$
[MSK Output]						
MSK input sensitivity	$V_{3S}$	The input level such that an MSK output with the same frequency is acquired when a 76-kHz CW is applied as $V_{IN}$ .			4	mVrms
MSK output high level	$V_{10H}$	$V_{IN} = 76\text{ kHz, } 4\text{ mVrms, CW}$	4			V
MSK output low level	$V_{10L}$				0.4	V

### Reference Characteristics

Parameter	Symbol	Conditions	Ratings	Unit
AAF cutoff frequency			300	kHz
HPF corner frequency			54	kHz
LPF cutoff frequency			125	kHz
BPF center frequency			76	kHz
BPF -3 dB frequency			19	kHz
Maximum in-band group delay time difference			$\pm 5$	$\mu\text{s}$

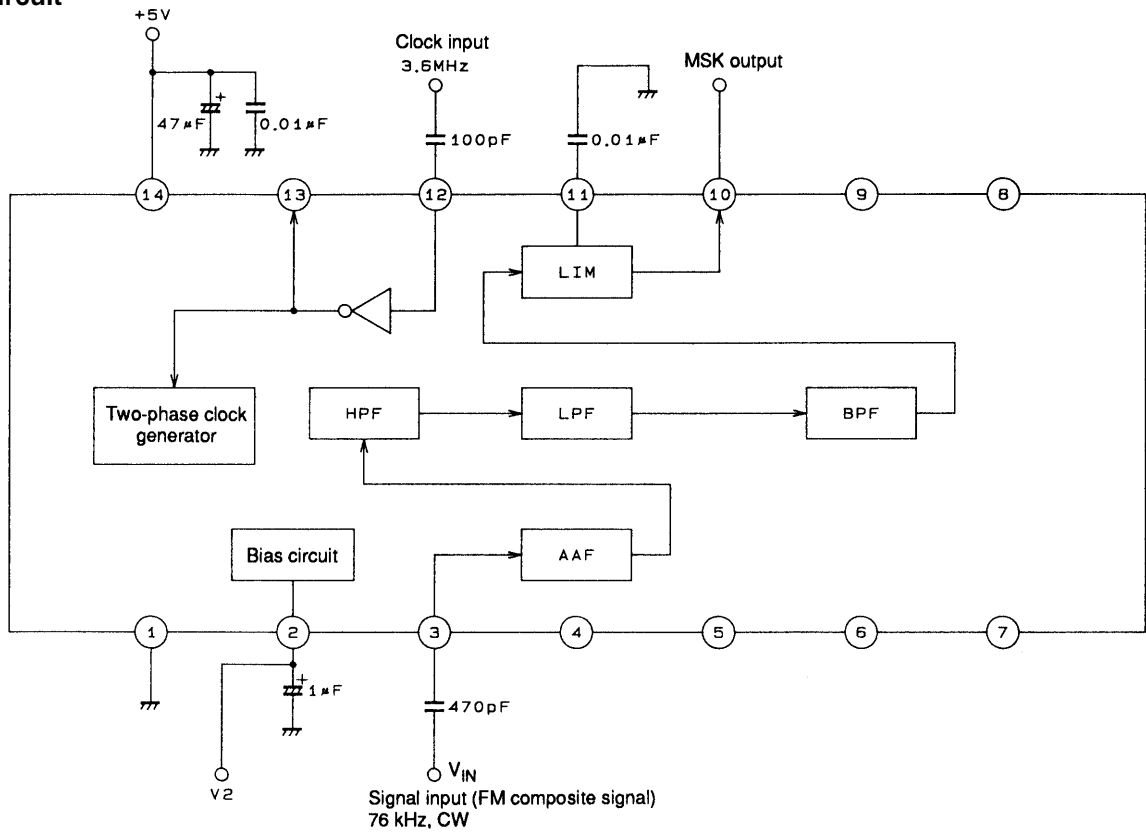
### Pin Functions

PinNo.	Symbol	Description
1	GND	Ground
2	VCOM	SCF block common. A decoupling capacitor must be used.
3	SIG. IN	Signal input. Input an FM modulated signal (composite signal). A modulated signal between 200 and 300 mVrms should be input. The input sensitivity for a pure 76-kHz signal is 4 mVrms or lower.
10	MSK OUT	MSK output (CMOS output)
11	$V_{REF}$	Limiter reference voltage. A low-pass filter is formed by the internal resistance (which is about 10 k $\Omega$ ) and an external capacitor.
12	CLK IN	3.6-MHz clock input. The DC bias at the CMOS inverter input, to which a 100-k $\Omega$ feedback resistor is connected, is about $V_{CC}/2$ . The clock signal is input through a capacitor.
13	CLK OUT	The clock output that was wave-shaped by an inverter. This pin is normally left open.
14	$V_{CC}$	Power supply
4 to 9	NC, Test PIN	This pin must be left open.

### Usage Notes

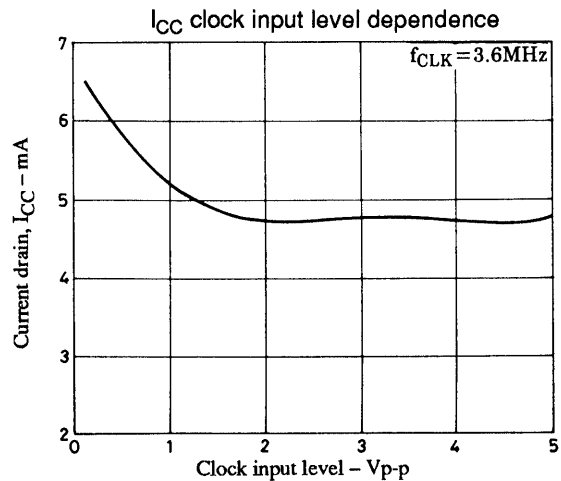
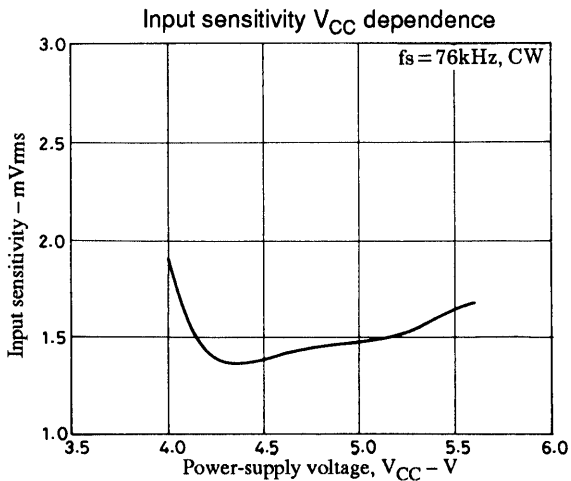
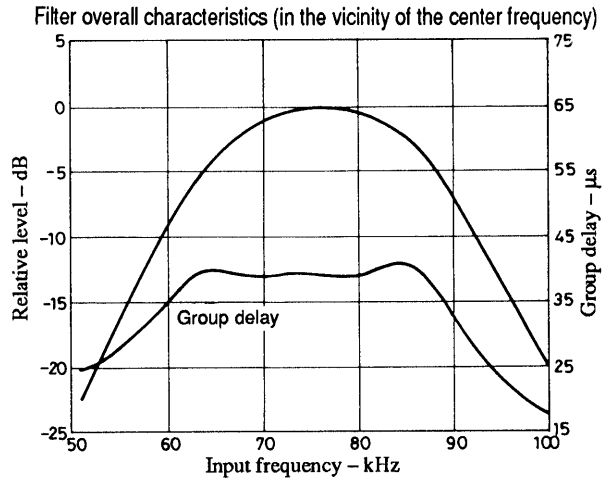
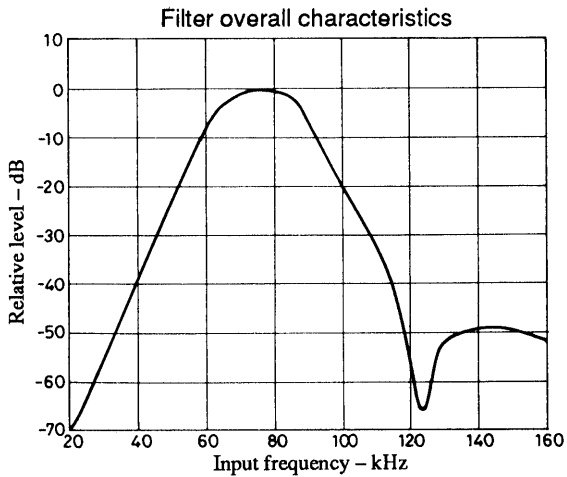
- Pins 4 to 9 and pin 13 are left open in normal use.
- The clock should be taken from the decoder (LC72700) clock output pin and input to pin through a capacitor of about 100 pF. Spurious radiation from the clock line can be reduced by inserting a resistor in the line and thus smoothing the rising and falling edges. This signal is then input to pin 12 through a capacitor.

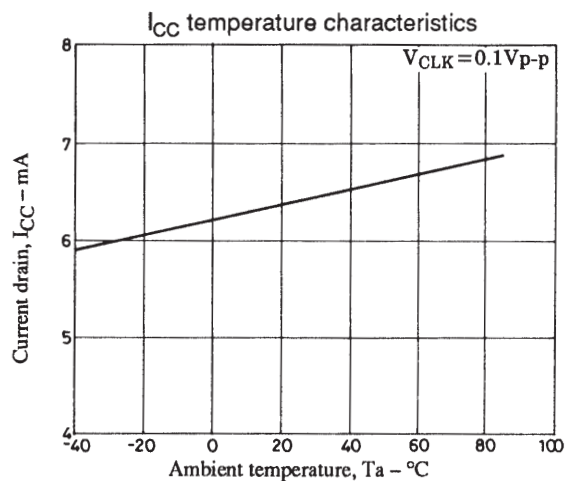
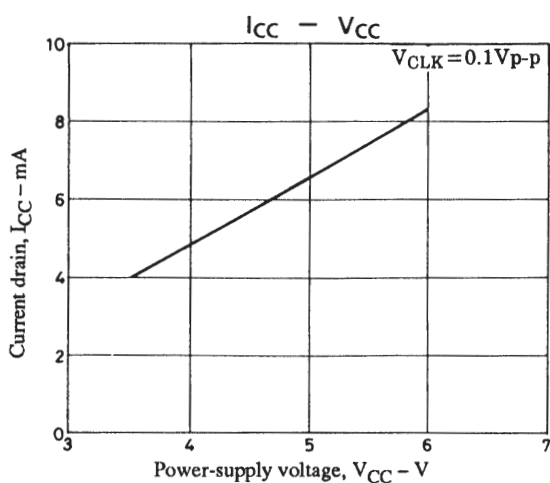
Test Circuit



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Note: Pins 4 to 9 are left open.





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