LXT3104

Quad T1/E1/J1 Long Haul/Short Haul Line Interface Unit

Preliminary Datasheet

The Intel® LXT3104 is a quad 3.3V Long Haul/Short Haul (LH/SH) T1/E1/J1 Line Interface Unit (LIU). This flexible LIU allows the design of T1/E1/J1 LH/SH multi-service cards with a single design and one bill-of-material. The LXT3104 LIU can be configured on a per-port basis through software. Intel's proven design robustness makes the LXT3104 LIU the perfect device for high-density T1/E1/J1 applications. To increase network reliability, Intel's LXT3104 incorporates a DSP-based architecture with features such as Intel® Hitless Protection Switching (Intel® HPS) and Intel® Pulse Template Matching (Intel® PTM). The DSP-based architecture is less sensitive to power supply and temperature variations and allows the LIU to adapt to varying line conditions. Intel® HPS allows the design of 1+1 redundant cards without the use of relays, as well as the ability to switch from one card to another without a loss of frame synchronization. Intel® PTM software allows the transmitter to shape the output pulse to meet various board conditions, without the need to change any external components.

Applications

- Voice over packet gateways
- Integrated Multi-service Access Platforms (IMAPs)
- Integrated Access Devices (IADs)
- Inverse multiplexing for ATM (IMA)
- Wireless base stations
- Routers
- Frame relay access devices
- CSU/DSU equipment

Product Features

- Intel® HPS for 1+1 protection without relays
- Intel® PTM software for pulse output adjustment through software without component or board change
- Interfaces with IXF3208, Octal T1/E1/J1 Framer with Intel® On-Chip Performance Report Messaging (Intel® PRM)
- T1 (100 Ω), E1 (75 and 120 Ω), J1 (110 Ω) termination and LH/SH selectable per port through software without component change
- Receiver sensitivity exceeds 36 dB @ 772 KHz and 43 dB @ 1024 KHz of cable attenuation providing margin for board and cable variations
- 3.3V power supply with 5V tolerant inputs
- On chip Clock Adaptor (CLAD) that allows one master clock for T1/E1/J1 applications (1X, 2X, 4X or 8X T1 or E1 clock)
- 16 bit BPV/Excess Zero counters per port
- B8ZS/HDB3 encoders and decoders, and unipolar/bipolar I/O modes selectable per port
- Digital Jitter Attenuator (DJA) in either receive or transmit path
- Meets or exceeds specifications in ANSI T1.102, T1.403 and T1.408; ITU I.431, CTR12/13, G.703, G.736, G.775 and G.823; ETSI 300-166 and 300-233; and AT&T Pub 62411
- Available in a 17x17mm 256 PBGA (LXT3104BE) or 208 QFP (LXT3104HE) package

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August 2001

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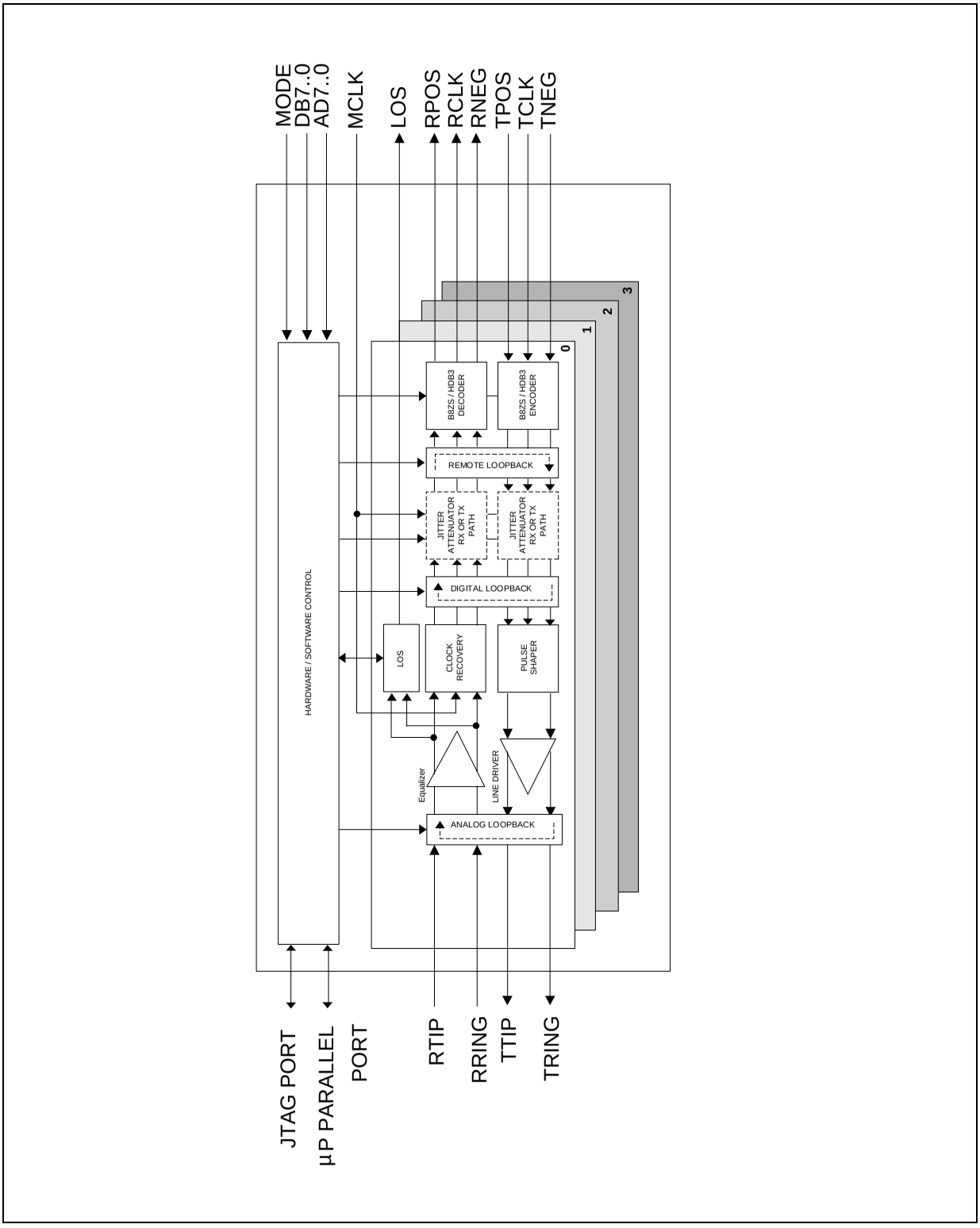
Revision History

Revision	Date	Description
00-1	8/23/01	Initial Issue.

Figure 1. LXT3104 Block Diagram



1.0 Pin Assignments and Signal Descriptions

Figure 2. LXT3104HE 208 Pin QFP Assignment

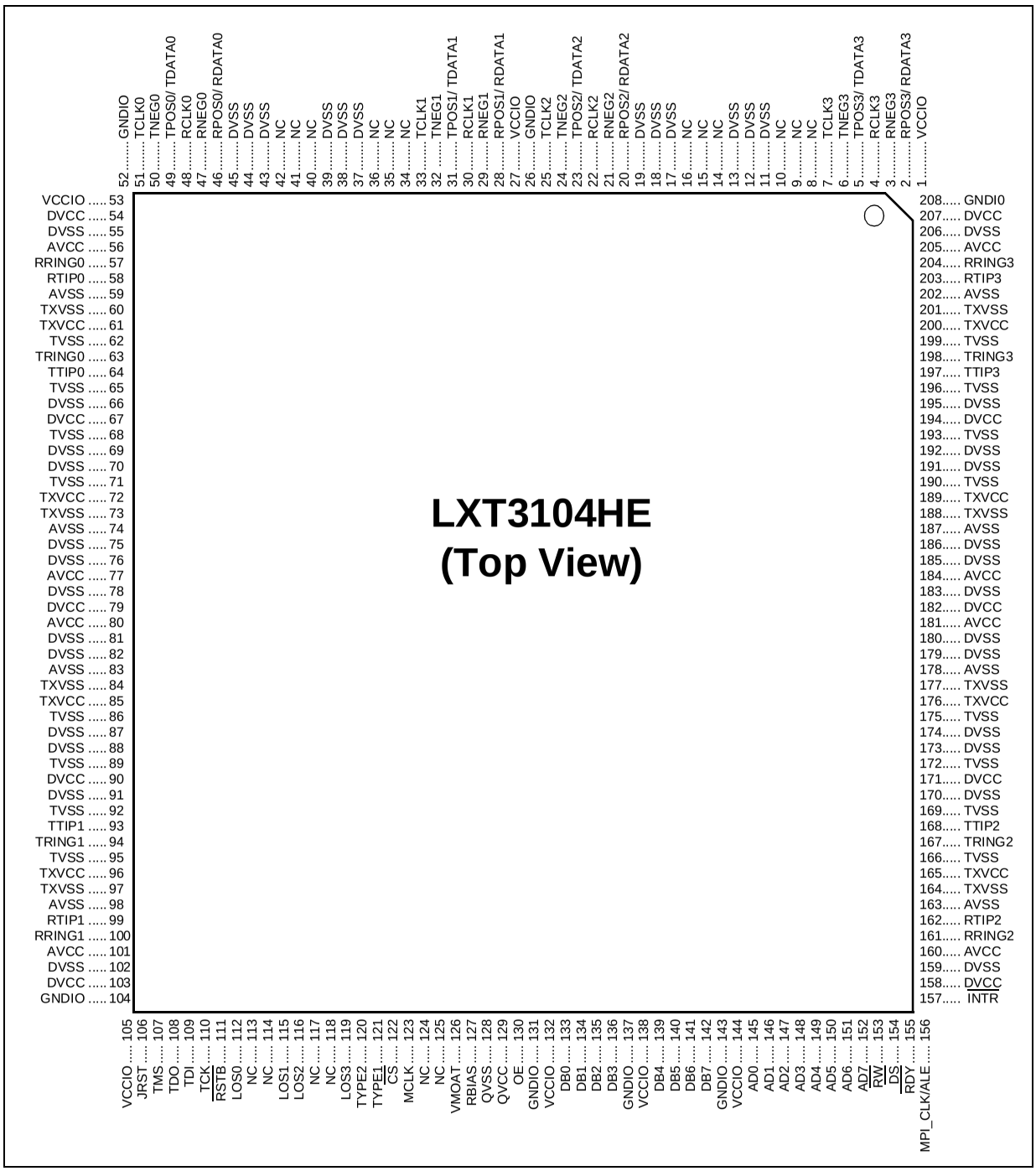
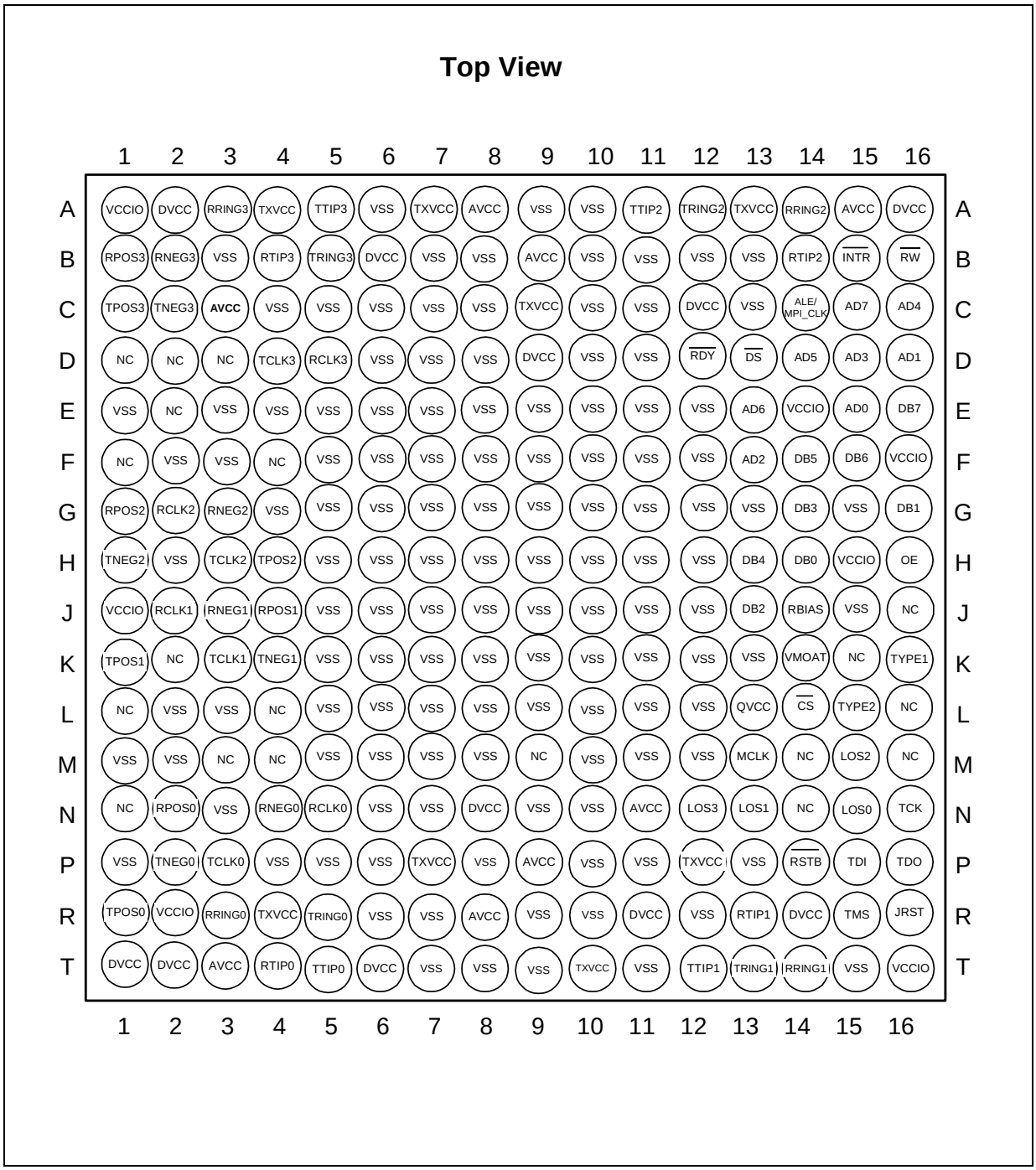


Figure 3. LXT3104BE 256 Plastic Ball Grid Array (PBGA) Assignments



2.0 Signal Descriptions

Table 1. LXT3104HE 208 Pin QFP Description

<table>
<tr><th>QFP</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>1</td><td>VCCIO</td><td>S</td><td>Power (I/O).</td></tr>
<tr><td>2</td><td>RPOS3/
RDATA3</td><td>DO</td><td>Receive Positive Data/Receive Data Output (Ch. 3). In bipolar mode this digital framer interface pin acts as the positive side of the bipolar data output pair, RPOS3 and RNEG3, recovered from the line interface. In unipolar mode, RDATA3 digital framer interface pin acts as a single Non-Return-to-Zero (NRZ) output of the data recovered from the line interface.
Bipolar Mode:
This pin acts as an active high NRZ receive data output. A High signal on RPOS3 corresponds to receipt of a positive pulse on RTIP3/RRING3. This signal along with RNEG3 is valid on the falling edge of RCLK3.
Unipolar Mode:
RDATA3 acts as the receive data output.</td></tr>
<tr><td>3</td><td>RNEG3</td><td>DO</td><td>Receive Negative Data (Ch. 3). In bipolar mode this digital framer interface pin acts as the negative side of the bipolar data output pair, RPOS3 and RNEG3, recovered from the line interface.
Bipolar Mode:
This pin acts as an active high NRZ receive signal output. A High signal on RNEG3 corresponds to receipt of a negative pulse on RTIP/RRING. This signal along with RPOS3 is valid on the falling edge of RCLK3.
Unipolar Mode:
Reserved TBD.</td></tr>
<tr><td>4</td><td>RCLK3</td><td>DO</td><td>Receive Clock Output (Ch. 3). This digital framer interface pin provides the recovered clock from the signal received at RTIP3 and RRING3. Under LOS conditions there is a transition from RCLK3 signal (derived from the recovered data) to MCLK signal at the RCLK3 output.</td></tr>
<tr><td>5</td><td>TPOS3/
TDATA3</td><td>DI</td><td>Transmit Positive Data/Transmit Data Input (Ch. 3). In bipolar mode this digital framer interface pin acts as the positive side of the bipolar data input pair, TPOS3 and TNEG3, which controls the signal transmitted to the line interface. In unipolar mode, TDATA3 digital framer interface pin acts as a single NRZ input data controlling the signal transmitted to the line interface.
Bipolar Mode:
TPOS3 is an active high NRZ input that operates together with TNEG3. TPOS3 starts the transmission of a positive pulse on TTIP3/TRING3 whereas TNEG3 starts the transmission of a negative pulse on TTIP3/TRING3.
<table>
<tr><th>TPOS3</th><th>TNEG3</th><th>Selection</th></tr>
<tr><td>0</td><td>0</td><td>Space</td></tr>
<tr><td>1</td><td>0</td><td>Positive Mark</td></tr>
<tr><td>0</td><td>1</td><td>Negative Mark</td></tr>
<tr><td>1</td><td>1</td><td>Space</td></tr>
</table>
Unipolar Mode:
TDATA3 acts as a single NRZ input controlling the signal transmitted to the line interface.</td></tr>
<tr><td>6</td><td>TNEG3</td><td>DI</td><td>Transmit Negative Data (Ch. 3). In bipolar mode this digital framer interface pin acts as the negative side of the bipolar data input pair, TPOS3 and TNEG3, which controls the signal transmitted to the line interface.
Unipolar Mode:
Tie TNEG3 low in unipolar mode.</td></tr>
</table>

Table 1. LXT3104HE 208 Pin QFP Description (Continued)

<table>
<tr><th>QFP</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>7</td><td>TCLK3</td><td>DI</td><td>Transmit Clock Input (Ch. 3). During normal operation TCLK3 toggles at the line rate, which is 1.544 MHz for T1/J1 operation, and 2.048 MHz for E1 operation. TPOS3 and TNEG3, or TDATA3, are sampled on the falling edge of TCLK3.
<table><tr><th>TCLK</th><th>Operating Mode</th></tr><tr><td>Clocked</td><td>Normal operation</td></tr><tr><td>L</td><td>Driver outputs tristated, but powered on for redundancy.</td></tr><tr><td>H</td><td>Driver outputs tristated and powered down for reduced power draw.</td></tr></table>
Note: The Transmit All Ones (TAOS) generator uses MCLK as a timing reference. In order to assure that the output frequency is within specification limits, MCLK must have the applicable stability.</td></tr>
<tr><td>8</td><td>NC</td><td></td><td>This pin must be left floating.</td></tr>
<tr><td>9</td><td>NC</td><td></td><td>This pin must be left floating.</td></tr>
<tr><td>10</td><td>NC</td><td></td><td>This pin must be left floating.</td></tr>
<tr><td>11</td><td>DVSS</td><td>S</td><td>Digital Ground.</td></tr>
<tr><td>12</td><td>DVSS</td><td>S</td><td>Digital Ground.</td></tr>
<tr><td>13</td><td>DVSS</td><td>S</td><td>Digital Ground.</td></tr>
<tr><td>14</td><td>NC</td><td></td><td>This pin must be left floating.</td></tr>
<tr><td>15</td><td>NC</td><td></td><td>This pin must be left floating.</td></tr>
<tr><td>16</td><td>NC</td><td></td><td>This pin must be left floating.</td></tr>
<tr><td>17</td><td>DVSS</td><td>S</td><td>Digital Ground.</td></tr>
<tr><td>18</td><td>DVSS</td><td>S</td><td>Digital Ground.</td></tr>
<tr><td>19</td><td>DVSS</td><td>S</td><td>Digital Ground.</td></tr>
<tr><td>20</td><td>RPOS2/
RDATA2</td><td>DO</td><td>Receive Positive Data/Receive Data Output (Ch. 2). In bipolar mode this pin acts as the positive side of the bipolar data output pair, RPOS2 and RNEG2, recovered from the line interface. In unipolar mode, RDATA2 acts as a single NRZ output of the data recovered from the line interface.</td></tr>
<tr><td>21</td><td>RNEG2</td><td>DO</td><td>Receive Negative Data (Ch. 2). In bipolar mode this pin acts as the negative side of the bipolar data output pair, RPOS2 and RNEG2, recovered from the line interface.</td></tr>
<tr><td>22</td><td>RCLK2</td><td>DO</td><td>Receive Clock Output (Ch. 2).</td></tr>
<tr><td>23</td><td>TPOS2/
TDATA2</td><td>DI</td><td>Transmit Positive Data/Transmit Data Input (Ch. 2). In bipolar mode this pin acts as the positive side of the bipolar data input pair, TPOS2 and TNEG2, which controls the signal transmitted to the line interface. In unipolar mode, TDATA2 acts as a single NRZ input data controlling the signal transmitted to the line interface.</td></tr>
<tr><td>24</td><td>TNEG2</td><td>DI</td><td>Transmit Negative Data (Ch. 2). In bipolar mode this pin acts as the negative side of the bipolar data input pair, TPOS2 and TNEG2, which controls the signal transmitted to the line interface.
<u>Unipolar Mode</u>:
Tie TNEG2 low in unipolar mode.</td></tr>
<tr><td>25</td><td>TCLK2</td><td>DI</td><td>Transmit Clock Input (Ch. 2).</td></tr>
<tr><td>26</td><td>GNDIO</td><td>S</td><td>Ground (I/O).</td></tr>
<tr><td>27</td><td>VCCIO</td><td>S</td><td>Power (I/O). 3.3 V.</td></tr>
</table>

Table 1. LXT3104HE 208 Pin QFP Description (Continued)

QFP	Symbol	I/O	Description
28	RPOS1/ RDATA1	DO	**Receive Positive Data/Receive Data Output (Ch. 1).** In bipolar mode this pin acts as the positive side of the bipolar data output pair, RPOS1 and RNEG1, recovered from the line interface. In unipolar mode, RDATA1 acts as a single NRZ output of the data recovered from the line interface.
29	RNEG1	DO	**Receive Negative Data (Ch. 1).** In bipolar mode this pin acts as the negative side of the bipolar data output pair, RPOS1 and RNEG1, recovered from the line interface.
30	RCLK1	DO	**Receive Clock Output (Ch. 1).**
31	TPOS1/ TDATA1	DI	**Transmit Positive Data/Transmit Data Input (Ch. 1).** In bipolar mode this pin acts as the positive side of the bipolar data input pair, TPOS1 and TNEG1, which controls the signal transmitted to the line interface. In unipolar mode, TDATA1 acts as a single NRZ input data controlling the signal transmitted to the line interface.
32	TNEG1	DI	**Transmit Negative Data (Ch. 1).** In bipolar mode this pin acts as the negative side of the bipolar data input pair, TPOS1 and TNEG1, which controls the signal transmitted to the line interface. Unipolar Mode: Tie TNEG3 low in unipolar mode.
33	TCLK1	DI	**Transmit Clock Input (Ch. 1).**
34	NC		**This pin must be left floating.**
35	NC		**This pin must be left floating.**
36	NC		**This pin must be left floating.**
37	DVSS	S	**Digital Ground.**
38	DVSS	S	**Digital Ground.**
39	DVSS	S	**Digital Ground.**
40	NC		**This pin must be left floating.**
41	NC		**This pin must be left floating.**
42	NC		**This pin must be left floating.**
43	DVSS	S	**Digital Ground.**
44	DVSS	S	**Digital Ground.**
45	DVSS	S	**Digital Ground.**
46	RPOS0/ RDATA0	DO	**Receive Positive Data/Receive Data Output (Ch. 0).** In bipolar mode this pin acts as the positive side of the bipolar data output pair, RPOS0 and RNEG0 recovered from the line interface. In unipolar mode, RDATA0 acts as a single NRZ output of the data recovered from the line interface.
47	RNEG0	DO	**Receive Negative Data (Ch. 0).** In bipolar mode this pin acts as the negative side of the bipolar data output pair, RPOS0 and RNEG0, recovered from the line interface.
48	RCLK0	DO	**Receive Clock Output (Ch.0).**
49	TPOS0/ TDATA0	DI	**Transmit Positive Data/Transmit Data Input (Ch. 0).** In bipolar mode this pin acts as the positive side of the bipolar data input pair, TPOS0 and TNEG0, which controls the signal transmitted to the line interface. In unipolar mode, TDATA0 acts as a single NRZ input data controlling the signal transmitted to the line interface.
50	TNEG0	DI	**Transmit Negative Data (Ch. 0).** In bipolar mode this pin acts as the negative side of the bipolar data input pair, TPOS0 and TNEG0, which controls the signal transmitted to the line interface. Unipolar Mode: Tie TNEG3 low in unipolar mode.
51	TCLK0	DI	**Transmit Clock Input (Ch. 0).**

Table 1. LXT3104HE 208 Pin QFP Description (Continued)

QFP	Symbol	I/O	Description
52	GNDIO	S	**Ground (I/O).**
53	VCCIO	S	**Power (I/O).**
54	DVCC	S	**Digital Power 3.3V.**
55	DVSS	S	**Digital Ground.**
56	AVCC	S	**Analog Power 3.3V.**
57	RRING0	AI	**Receive Ring Input (Ch. 0).** This pin is one of the pair of inputs, RRING0/RTIP0, to the differential line receiver at the line interface for the port. Data and clock are recovered and output at the digital framer interface output pins.
58	RTIP0	AI	**Receive Tip Input (Ch. 0).** This pin is one of the pair of inputs, RRING0/RTIP0, to the differential line receiver at the line interface for the port. Data and clock are recovered and output at the digital framer interface output pins.
59	AVSS	S	**Analog Ground.**
60	TXVSS	S	**Transmit Ground.** Ground pin for transmit logic.
61	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.
62	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
63	TRING0	AO	**Transmit Ring Output (Ch. 0).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP0/TRING0. TTIP0/TRING0 will be in a high impedance state if the TCLK pin is static or if the OE pin is Low. TTIP0/TRING0 can be tristated on a port-by-port basis by writing a ‘1’ to the TXPD bit in “Port Master Control Page Register, 01h” on page 65, or the OES bit in “Transmit Control Page Register, 03h” on page 66. Please refer to “Transmit Idle Operation and Tristating Drivers” on page 43 for details.
64	TTIP0	AO	**Transmit Tip Output (Ch. 0).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP0/TRING0.
65	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
66	DVSS	S	**Digital Ground.**
67	DVCC	S	**Digital Power 3.3V**
68	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
69	DVSS	S	**Digital Ground.**
70	DVSS	S	**Digital Ground.**
71	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
72	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.
73	TXVSS	S	**Transmit Ground.** Ground pin for transmit logic.
74	AVSS	S	**Analog Ground**
75	DVSS	S	**Digital Ground.**
76	DVSS	S	**Digital Ground.**
77	AVCC	S	**Analog Power 3.3V.**
78	DVSS	S	**Digital Ground.**
79	DVCC	S	**Digital Power 3.3V.**
80	AVCC	S	**Analog Power 3.3V.**
81	DVSS	S	**Digital Ground.**
82	DVSS	S	**Digital Ground.**
83	AVSS	S	**Analog Ground.**

Table 1. LXT3104HE 208 Pin QFP Description (Continued)

QFP	Symbol	I/O	Description
84	TXVSS	S	**Transmit Ground.** Ground pin for transmit logic.
85	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.
86	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
87	DVSS	S	**Digital Ground.**
88	DVSS	S	**Digital Ground.**
89	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
90	DVCC	S	**Digital Power 3.3V.**
91	DVSS	S	**Digital Ground.**
92	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
93	TTIP1	AO	**Transmit Tip Output (Ch. 1).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP1/TRING1.
94	TRING1	AO	**Transmit Ring Output (Ch. 1).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP1/TRING1.
95	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
96	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.
97	TXVSS	S	**Transmit Ground.** Ground pin for transmit logic.
98	AVSS	S	**Analog Ground.**
99	RTIP1	AI	**Receive Tip Input (Ch. 1).** This pin is one of the pair of inputs, RRING1/RTIP1, to the differential line receiver at the line interface for the port.
100	RRING1	AI	**Receive Ring Input (Ch. 1).** This pin is one of the pair of inputs, RRING1/RTIP1, to the differential line receiver at the line interface for the port.
101	AVCC	S	**Analog Power 3.3V.**
102	DVSS	S	**Digital Ground.**
103	DVCC	S	**Digital Power 3.3V.**
104	GNDIO	S	**Ground (I/O).**
105	VCCIO	S	**Power (I/O). 3.3V.**
106	JRST	DI	**JTAG Controller Reset Input.** Input is used to reset the JTAG controller. This pin should be tied to ground through a 1K resistor.
107	TMS	DI	**JTAG Test Mode Select Input.** Used to control the test logic state machine. Sampled on rising edge of TCK. TMS is pulled up internally and may be left disconnected.
108	TDO	DO	**JTAG Data Output.** During JTAG operation, this pin is Test Data Output for JTAG. Used for reading all serial configuration and test data from internal test logic. It is updated on falling edge of TCK.
109	TDI	DI	**JTAG Data Input.** This pin is Test Data input for JTAG. Used for loading serial instructions and data into internal test logic. Sampled on rising edge of TCK. TDI is pulled up internally and may be left disconnected.
110	TCK	DI	**JTAG Clock Input.** This pin is clock input for JTAG. Connect to GND when not used.
111	$\overline{\text{RSTB}}$	DI	**Reset.** This pin is the reset pin for the LXT3104 quad LIU. One microsecond after $\overline{\text{RSTB}}$ goes Low, the internal registers will be restored to their default values.

Table 1. LXT3104HE 208 Pin QFP Description (Continued)

QFP	Symbol	I/O	Description
112	LOS0	DO	**Loss of Signal Output (Ch. 0).** When LOS0 output is High, it indicates a loss of signal at the port's line interface receiver. LOS goes active after the incoming signal has insufficient transitions for a specified time interval, which is determined by the page and global register settings. The LOS condition is cleared and the output pin returns to Low when the incoming signal has a sufficient number of transitions in a specified time interval, as determined by the register settings.
113	NC		**This pin must be left floating.**
114	NC		**This pin must be left floating.**
115	LOS1	DO	**Loss of Signal Output (Ch. 1).**
116	LOS2	DO	**Loss of Signal Output (Ch. 2).**
117	NC		**This pin must be left floating.**
118	NC		**This pin must be left floating.**
119	LOS3	DO	**Loss of Signal Output (Ch. 3).**
120	TYPE2	DI	**Microprocessor Type Select Inputs.** These pins control which microprocessor interface is active: TYPE2 TYPE1 Microprocessor 0 0 MPC860, M68360 0 1 i960, i486 1 0 M68302 1 1 8051 mux-mode
121	TYPE1	DI	
122	$\overline{CS}$	DI	**Chip Select.** This active Low input initiates each access to the parallel microprocessor interface. For each read or write operation, $\overline{CS}$ must transition from High to Low, and remain Low.
123	MCLK	DI	**Master Clock Input.** MCLK is an independent, free-running reference clock. The start up frequency is 16.382 MHz for T1/E1/J1 operation. After initialization the frequency can be set to 8, 4, 2 or 1x of the T1/E1/J1 frequency. This reference clock is used to generate several internal reference signals: • Timing reference for the integrated clock recovery unit. • Timing reference for the integrated digital jitter attenuator. • Generation of RCLK signal during a loss of signal condition. • Reference clock during a blue alarm transmit all ones (TAOS) condition. • Reference timing for the parallel processor wait state generation logic.
124	NC		**This pin must be left floating.**
125	NC		**This pin must be left floating.**
126	VMOAT	AI	**Substrate Ground.**
127	RBIAS	AI	**Resistor Bias Input.** A 30K Ω, 1% ±100 PPM/°C, resistor must be connected from this pin to analog ground.
128	QVSS	AI	**Ground for analog bias circuit.**
129	QVCC	AI	**Power for analog bias circuit. 3.3V.**
130	OE	DI	**Output Driver Enable Input.** If this pin is asserted low every port's analog driver/transmitter output immediately enters a high impedance state to support redundancy applications without external mechanical relays. All other internal circuitry stays active. TTIP and TRING for each port can also be tristated individually by writing a '1' to the TXPD bit in "Port Master Control Page Register, 01h" on page 65 or the OES bit in the "Transmit Control Page Register, 03h" on page 66. Please refer to "Transmit Idle Operation and Tristating Drivers" on page 43 for details.
131	GNDIO	S	**Ground (I/O).**

Table 1. LXT3104HE 208 Pin QFP Description (Continued)

QFP	Symbol	I/O	Description
132	VCCIO	S	**Power (I/O). 3.3V.**
133 134 135 136	DB0 DB1 DB2 DB3	DI/O DI/O DI/O DI/O	**Data Bus Input/Output.** When a non-multiplexed microprocessor interface is selected, these pins function as a bi-directional 8-bit data bus. When a multiplexed microprocessor interface is selected, these pins carry both bi-directional 8-bit data and address inputs A0 -A7.
137	GNDIO	S	**Ground (I/O).**
138	VCCIO	S	**Power (I/O). 3.3V.**
139 140 141 142	DB4 DB5 DB6 DB7	DI/O DI/O DI/O DI/O	**Data Bus Input/Output.** When a non-multiplexed microprocessor interface is selected, these pins function as a bi-directional 8-bit data bus. When a multiplexed microprocessor interface is selected, these pins carry both bi-directional 8-bit data and address inputs A0 -A7.
143	GNDIO	S	**Ground (I/O).**
144	VCCIO	S	**Power (I/O). 3.3V.**
145 146 147 148 149 150 151 152	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	DI DI DI DI DI DI DI DI	**Address Bus Input.** In non-multiplexed mode these inputs function as address input pins for the microprocessor bus. In muxed mode (8051), all pins must be tied low.
153	$\overline{RW}$	DI	This pin has one of two functions depending on the microprocessor interface selected by the TYPE1 and TYPE2 inputs. • **Read/Write Input** (Motorola Mode). • **Write Enable Active Low Input** (Intel mode).
154	$\overline{DS}$	DI	This pin has one of two functions depending on the microprocessor interface selected by the TYPE1 and TYPE2 inputs. • **Data Strobe Input** (Motorola Mode). • **Read Enable Active Low Input** (Intel mode)
155	$\overline{RDY}$	DO	This pin has one of two functions depending on the microprocessor interface selected by the TYPE1 and TYPE2 inputs. • **Data Transfer Acknowledge Output.** (Motorola Mode). • **Ready Output** (Intel mode). Motorola Mode: A Low signal on ACK during a read operation indicates that the information on the data bus is valid. A Low signal during a write operation acknowledges that a data transfer into the addressed register has been accepted (acknowledge signal).
156	MPI_CLK/ ALE	DI	This pin has one of two functions depending on the microprocessor interface selected by the TYPE1 and TYPE2 inputs. **Address Latch Enable Input** (8051 Mode). • The address on the multiplexed address/data bus is clocked into the device with the falling edge of ALE. **Microprocessor Clock** (Intel i486 Mode). • This pin is used to input the microprocessor clock in the synchronous i486 mode.
157	$\overline{INTR}$	DO	**Interrupt.** This active Low, maskable, open drain output requires an external 10k pull-up resistor. If the corresponding interrupt enable bit is enabled, INTR goes Low to flag the microprocessor when the LXT3104 changes state (see details in the interrupt handling section). The microprocessor interrupt input should be set to level triggering.

Table 1. LXT3104HE 208 Pin QFP Description (Continued)

QFP	Symbol	I/O	Description
158	DVCC	S	**Digital Power 3.3V.**
159	DVSS	S	**Digital Ground.**
160	AVCC	S	**Analog Power 3.3V.**
161	RRING2	AI	**Receive Ring Input (Ch. 2).** This pin is one of the pair of inputs, RRING2/RTIP2, to the differential line receiver at the line interface for the port.
162	RTIP2	AI	**Receive Tip Input (Ch. 2).** This pin is one of the pair of inputs, RRING2/RTIP2, to the differential line receiver at the line interface for the port.
163	AVSS	S	**Analog Ground.**
164	TXVSS	S	**Transmit Ground.** Ground pin for transmit logic.
165	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.
166	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
167	TRING2	AO	**Transmit Ring Output (Ch. 2).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP2/TRING2.
168	TTIP2	AO	**Transmit Tip Output (Ch. 2).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP2/TRING2.
169	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
170	DVSS	S	**Digital Ground.**
171	DVCC	S	**Digital Power 3.3V.**
172	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
173	DVSS	S	**Digital Ground.**
174	DVSS	S	**Digital Ground.**
175	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
176	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.
177	TXVSS	S	**Transmit Ground.** Ground pin for transmit logic.
178	AVSS	S	**Analog Ground.**
179	DVSS	S	**Digital Ground.**
180	DVSS	S	**Digital Ground.**
181	AVCC	S	**Analog Power 3.3V.**
182	DVCC	S	**Digital Power 3.3V.**
183	DVSS	S	**Digital Ground.**
184	AVCC	S	**Analog Power 3.3V.**
185	DVSS	S	**Digital Ground.**
186	DVSS	S	**Digital Ground.**
187	AVSS	S	**Analog Ground.**
188	TXVSS	S	**Transmit Ground.** Ground pin for transmit logic.
189	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.
190	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
191	DVSS	S	**Digital Ground.**
192	DVSS	S	**Digital Ground.**

Table 1. LXT3104HE 208 Pin QFP Description (Continued)

QFP	Symbol	I/O	Description
193	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
194	DVCC	S	**Digital Power 3.3V.**
195	DVSS	S	**Digital Ground.**
196	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
197	TTIP3	AO	**Transmit Tip Output (Ch. 3).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP3/TRING3.
198	TRING3	AO	**Transmit Ring Output (Ch. 3).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP3/TRING3.
199	TVSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
200	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.
201	TXVSS	S	**Transmit Ground.** Ground pin for transmit logic.
202	AVSS	S	**Analog Ground.**
203	RTIP3	AI	**Receive Tip Input (Ch. 3).** This pin is one of the pair of inputs, RRING3/RTIP3, to the differential line receiver at the line interface for the port.
204	RRING3	AI	**Receive Ring Input (Ch. 3).** This pin is one of the pair of inputs, RRING3/RTIP3, to the differential line receiver at the line interface for the port.
205	AVCC	S	**Analog Power 3.3V.**
206	DVSS	S	**Digital Ground.**
207	DVCC	S	**Digital Power 3.3V.**
208	GNDIO	S	**Ground (I/O).**

Table 2. LXT3104BE 256 PBGA Description

PBGA	Symbol	I/O	Description
Power Connections			
A1	VCCIO	S	**Power (I/O).**
J1	VCCIO	S	**Power (I/O).**
R2	VCCIO	S	**Power (I/O).**
T16	VCCIO	S	**Power (I/O).**
H15	VCCIO	S	**Power (I/O).**
F16	VCCIO	S	**Power (I/O).**
E14	VCCIO	S	**Power (I/O).**
T1	DVCC	S	**Digital Power 3.3V.**
T6	DVCC	S	**Digital Power 3.3V**
R11	DVCC	S	**Digital Power 3.3V.**
R14	DVCC	S	**Digital Power 3.3V.**
N8	DVCC	S	**Digital Power 3.3V.**
D9	DVCC	S	**Digital Power 3.3V.**
C12	DVCC	S	**Digital Power 3.3V.**
A16	DVCC	S	**Digital Power 3.3V.**
B6	DVCC	S	**Digital Power 3.3V.**
A2	DVCC	S	**Digital Power 3.3V.**
T3	AVCC	S	**Analog Power 3.3V.**
P9	AVCC	S	**Analog Power 3.3V.**
R8	AVCC	S	**Analog Power 3.3V.**
N11	AVCC	S	**Analog Power 3.3V.**
A15	AVCC	S	**Analog Power 3.3V.**
A8	AVCC	S	**Analog Power 3.3V.**
B9	AVCC	S	**Analog Power 3.3V.**
C3	AVCC	S	**Analog Power 3.3V.**
P7	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.
R4	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.
P12	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.
T10	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.
A13	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.
A7	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.
C9	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.
A4	TXVCC	S	**Transmit Power Supply.** Power supply pin for the transmit logic, 3.3V.
L13	QVCC	AI	**Power for analog bias circuit.**
T2	DVCC	S	**Digital Power 3.3V.**
E4	VSS	S	**Digital Ground.**

Table 2. LXT3104BE 256 PBGA Description (Continued)

PBGA	Symbol	I/O	Description
E3	VSS	S	**Digital Ground.**
E1	VSS	S	**Digital Ground.**
F3	VSS	S	**Digital Ground.**
F2	VSS	S	**Digital Ground.**
G4	VSS	S	**Digital Ground.**
L3	VSS	S	**Digital Ground.**
M1	VSS	S	**Digital Ground.**
L2	VSS	S	**Digital Ground.**
M2	VSS	S	**Digital Ground.**
N3	VSS	S	**Digital Ground.**
P1	VSS	S	**Digital Ground.**
T8	VSS	S	**Digital Ground.**
L6	VSS	S	**Digital Ground.**
R6	VSS	S	**Digital Ground.**
T7	VSS	S	**Digital Ground.**
R7	VSS	S	**Digital Ground.**
P8	VSS	S	**Digital Ground.**
N10	VSS	S	**Digital Ground.**
T9	VSS	S	**Digital Ground.**
R9	VSS	S	**Digital Ground.**
R10	VSS	S	**Digital Ground.**
T11	VSS	S	**Digital Ground.**
M11	VSS	S	**Digital Ground.**
M6	VSS	S	**Digital Ground.**
E12	VSS	S	**Digital Ground.**
C11	VSS	S	**Digital Ground.**
A10	VSS	S	**Digital Ground.**
B11	VSS	S	**Digital Ground.**
C8	VSS	S	**Digital Ground.**
A9	VSS	S	**Digital Ground.**
D6	VSS	S	**Digital Ground.**
C7	VSS	S	**Digital Ground.**
B8	VSS	S	**Digital Ground.**
B7	VSS	S	**Digital Ground.**
A6	VSS	S	**Digital Ground.**
C5	VSS	S	**Digital Ground.**
E9	VSS	S	**Digital Ground.**
P6	VSS	S	**Transmit Ground.** Ground pin for transmit logic.

Table 2. LXT3104BE 256 PBGA Description (Continued)

PBGA	Symbol	I/O	Description
N6	VSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
N7	VSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
N9	VSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
P10	VSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
P11	VSS	S	**Transmit Ground.** Ground pin for transmit logic.
R12	VSS	S	**Transmit Ground.** Ground pin for transmit logic.
P13	VSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
T15	VSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
M12	VSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
M10	VSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
M7	VSS	S	**Transmit Ground.** Ground pin for transmit logic.
D11	VSS	S	**Transmit Ground.** Ground pin for transmit logic.
B13	VSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
B12	VSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
D10	VSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
E10	VSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
B10	VSS	S	**Transmit Ground.** Ground pin for transmit logic.
E6	VSS	S	**Transmit Ground.** Ground pin for transmit logic.
B3	VSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
C4	VSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
C6	VSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
E5	VSS	S	**Transmit Driver Ground.** Ground pin for the output driver.
E8	VSS	S	**Transmit Ground.** Ground pin for transmit logic.
H2	VSS	S	**Ground (I/O).**
P4	VSS	S	**Ground (I/O).**
M5	VSS	S	**Ground (I/O).**
L12	VSS	S	**Ground (I/O).**
J15	VSS	S	**Ground (I/O).**
G15	VSS	S	**Ground (I/O).**
E11	VSS	S	**Ground (I/O).**
P5	VSS	S	**Analog Ground.**
G13	VSS	S	**Analog Ground**
L5	VSS	S	**Analog Ground.**
C13	VSS	S	**Analog Ground.**
C10	VSS	S	**Analog Ground.**
D7	VSS	S	**Analog Ground.**
E7	VSS	S	**Analog Ground.**
K14	VMOAT	AI	**Substrate Ground.**

Table 2. LXT3104BE 256 PBGA Description (Continued)

PBGA	Symbol	I/O	Description
K13	VSS	S	**Ground for analog bias circuit.**
D8, F5, F6, F7, F8, F9, F10, F11, F12, G5, G6, G7, G8, G9, G10, G11, G12, H5, H6, H7, H8, H9, H10, H11, H12, J5, J6, J7, J8, J9, J10, J11, J12, K5, K6, K7, K8, K9, K10, K11, K12, L7, L8, L9, L10, L11, M8	VSS	S	**Ground.**
Digital Interface Connections			
N2	RPOS0/ RDATA0	DO	**Receive Positive Data/Receive Data Output (Ch. 0).** In bipolar mode this digital framer interface pin acts as the positive side of the bipolar data output pair, RPOS0 and RNEG0 recovered from the line interface. In unipolar mode, RDATA0 digital framer interface pin acts as a single Non-Return-to-Zero (NRZ) output of the data recovered from the line interface. Bipolar Mode: This pin acts as an active high NRZ receive data output. A High signal on RPOS0 corresponds to receipt of a positive pulse on RTIP0/RRING0. This signal along with RNEG0 is valid on the falling edge of RCLK0. Unipolar Mode: RDATA0 acts as the receive data output.
N4	RNEG0	DO	**Receive Negative Data (Ch. 0).** In bipolar mode this digital framer interface pin acts as the negative side of the bipolar data output pair, RPOS0 and RNEG0, recovered from the line interface. Bipolar Mode: This pin acts as an active high NRZ receive signal output. A High signal on RNEG0 corresponds to receipt of a negative pulse on RTIP0/RRING0. This signal along with RPOS0 is valid on the falling edge of RCLK0. Unipolar Mode: Reserved TBD.
N5	RCLK0	DO	**Receive Clock Output (Ch. 0).** This digital framer interface pin provides the recovered clock from the signal received at RTIP0 and RRING0. Under LOS conditions there is a transition from RCLK0 signal (derived from the recovered data) to MCLK signal at the RCLK0 output.

Table 2. LXT3104BE 256 PBGA Description (Continued)

<table>
<tr><th>PBGA</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>R1</td><td>TPOS0/
TDATA0</td><td>DI</td><td>Transmit Positive Data/Transmit Data Input (Ch. 0). In bipolar mode this digital framer interface pin acts as the positive side of the bipolar data input pair, TPOS0 and TNEG0, which controls the signal transmitted to the line interface. In unipolar mode, TDATA0 digital framer interface pin acts as a single NRZ input data controlling the signal transmitted to the line interface.
Bipolar Mode:
TPOS0 is an active high NRZ input that operates together with TNEG0. TPOS0 starts the transmission of a positive pulse on TTIP0/TRING0 whereas TNEG0 starts the transmission of a negative pulse on TTIP0/TRING0.
<table>
<tr><th>TPOS0</th><th>TNEG0</th><th>Selection</th></tr>
<tr><td>0</td><td>0</td><td>Space</td></tr>
<tr><td>1</td><td>0</td><td>Positive Mark</td></tr>
<tr><td>0</td><td>1</td><td>Negative Mark</td></tr>
<tr><td>1</td><td>1</td><td>Space</td></tr>
</table>
Unipolar Mode:
TDATA0 acts as a single NRZ input controlling the signal transmitted to the line interface.</td></tr>
<tr><td>P2</td><td>TNEG0</td><td>DI</td><td>Transmit Negative Data (Ch. 0). In bipolar mode this digital framer interface pin acts as the negative side of the bipolar data input pair, TPOS0 and TNEG0, which controls the signal transmitted to the line interface.
Unipolar Mode:
Tie TNEG0 low in unipolar mode.</td></tr>
<tr><td>P3</td><td>TCLK0</td><td>DI</td><td>Transmit Clock Input (Ch. 0). During normal operation TCLK0 toggles at the line rate, which is 1.544 MHz for T1/J1 operation, and 2.048 MHz for E1 operation. TPOS0 and TNEG0, or TDATA0, are sampled on the falling edge of TCLK0.
<table>
<tr><th>TCLK</th><th>Operating Mode</th></tr>
<tr><td>Clocked</td><td>Normal operation</td></tr>
<tr><td>L</td><td>Driver outputs tristated, but powered on for redundancy.</td></tr>
<tr><td>H</td><td>Driver outputs tristated and powered down for reduced power draw.</td></tr>
</table>
Note: The Transmit All Ones (TAOS) generator uses MCLK as a timing reference. In order to assure that the output frequency is within specification limits, MCLK must have the applicable stability.</td></tr>
<tr><td>J4</td><td>RPOS1/
RDATA1</td><td>DO</td><td>Receive Positive Data/Receive Data Output (Ch. 1). In bipolar mode this pin acts as the positive side of the bipolar data output pair, RPOS1 and RNEG1, recovered from the line interface. In unipolar mode, RDATA1 acts as a single NRZ output of the data recovered from the line interface.</td></tr>
<tr><td>J3</td><td>RNEG1</td><td>DO</td><td>Receive Negative Data (Ch. 1). In bipolar mode this pin acts as the negative side of the bipolar data output pair, RPOS1 and RNEG1, recovered from the line interface.</td></tr>
<tr><td>J2</td><td>RCLK1</td><td>DO</td><td>Receive Clock Output (Ch. 1).</td></tr>
<tr><td>K1</td><td>TPOS1/
TDATA1</td><td>DI</td><td>Transmit Positive Data/Transmit Data Input (Ch. 1). In bipolar mode this pin acts as the positive side of the bipolar data input pair, TPOS1 and TNEG1, which controls the signal transmitted to the line interface. In unipolar mode, TDATA1 acts as a single NRZ input data controlling the signal transmitted to the line interface.</td></tr>
</table>

Table 2. LXT3104BE 256 PBGA Description (Continued)

PBGA	Symbol	I/O	Description
K4	TNEG1	DI	**Transmit Negative Data (Ch. 1).** In bipolar mode this pin acts as the negative side of the bipolar data input pair, TPOS1 and TNEG1, which controls the signal transmitted to the line interface. Unipolar Mode: Tie TNEG1 low in unipolar mode
K3	TCLK1	DI	**Transmit Clock Input (Ch. 1).**
G1	RPOS2/ RDATA2	DO	**Receive Positive Data/Receive Data Output (Ch. 2).** In bipolar mode this pin acts as the positive side of the bipolar data output pair, RPOS2 and RNEG2, recovered from the line interface. In unipolar mode, RDATA2 acts as a single NRZ output of the data recovered from the line interface.
G3	RNEG2	DO	**Receive Negative Data (Ch. 2).** In bipolar mode this pin acts as the negative side of the bipolar data output pair, RPOS2 and RNEG2, recovered from the line interface.
G2	RCLK2	DO	**Receive Clock Output (Ch. 2).**
H4	TPOS2/ TDATA2	DI	**Transmit Positive Data/Transmit Data Input (Ch. 2).** In bipolar mode this pin acts as the positive side of the bipolar data input pair, TPOS2 and TNEG2, which controls the signal transmitted to the line interface. In unipolar mode, TDATA2 acts as a single NRZ input data controlling the signal transmitted to the line interface.
H1	TNEG2	DI	**Transmit Negative Data (Ch. 2).** In bipolar mode this pin acts as the negative side of the bipolar data input pair, TPOS2 and TNEG2, which controls the signal transmitted to the line interface. Unipolar Mode: Tie TNEG2 low in unipolar mode
H3	TCLK2	DI	**Transmit Clock Input (Ch. 2).**
B1	RPOS3/ RDATA3	DO	**Receive Positive Data/Receive Data Output (Ch. 3).** In bipolar mode this pin acts as the positive side of the bipolar data output pair, RPOS3 and RNEG3 recovered from the line interface. In unipolar mode, RDATA3 acts as a single NRZ output of the data recovered from the line interface.
B2	RNEG3	DO	**Receive Negative Data (Ch. 3).** In bipolar mode this pin acts as the negative side of the bipolar data output pair, RPOS3 and RNEG3, recovered from the line interface.
D5	RCLK3	DO	**Receive Clock Output (Ch. 3).**
C1	TPOS3/ TDATA3	DI	**Transmit Positive Data/Transmit Data Input (Ch. 3).** In bipolar mode this pin acts as the positive side of the bipolar data input pair, TPOS3 and TNEG3, which controls the signal transmitted to the line interface. In unipolar mode, TDATA3 acts as a single NRZ input data controlling the signal transmitted to the line interface.
C2	TNEG3	DI	**Transmit Negative Data (Ch. 3).** In bipolar mode this pin acts as the negative side of the bipolar data input pair, TPOS3 and TNEG3, which controls the signal transmitted to the line interface. Unipolar Mode: Tie TNEG3 low in unipolar mode
D4	TCLK3	DI	**Transmit Clock Input (Ch. 3).**
Analog Interface Connections			
R3	RRING0	AI	**Receive Ring Input (Ch. 0).** This pin is one of the pair of inputs, RRING0/RTIP0, to the differential line receiver at the line interface for the port. Data and clock are recovered and output at the digital framer interface output pins.
T4	RTIP0	AI	**Receive Tip Input (Ch. 0).** This pin is one of the pair of inputs, RRING0/RTIP0, to the differential line receiver at the line interface for the port. Data and clock are recovered and output at the digital framer interface output pins.

Table 2. LXT3104BE 256 PBGA Description (Continued)

PBGA	Symbol	I/O	Description
R5	TRING0	AO	**Transmit Ring Output (Ch. 0).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP0/TRING0. TTIP0/TRING0 will be in a high impedance state if the TCLK pin is static or if the OE pin is Low. TTIP0/TRING0 can be tristated on a port-by-port basis by writing a '1' to the TXPD bit in "Port Master Control Page Register, 01h" on page 65, or the OES bit in "Transmit Control Page Register, 03h" on page 66. Please refer to "Transmit Idle Operation and Tristating Drivers" on page 43 for details.
T5	TTIP0	AO	**Transmit Tip Output (Ch. 0).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP0/TRING0.
T12	TTIP1	AO	**Transmit Tip Output (Ch. 1).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP1/TRING1.
T13	TRING1	AO	**Transmit Ring Output (Ch. 1).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP1/TRING1.
R13	RTIP1	AI	**Receive Tip Input (Ch. 1).** This pin is one of the pair of inputs, RRING1/RTIP1, to the differential line receiver at the line interface for the port.
T14	RRING1	AI	**Receive Ring Input (Ch. 1).** This pin is one of the pair of inputs, RRING1/RTIP1, to the differential line receiver at the line interface for the port.
A14	RRING2	AI	**Receive Ring Input (Ch. 2).** This pin is one of the pair of inputs, RRING2/RTIP2, to the differential line receiver at the line interface for the port.
B14	RTIP2	AI	**Receive Tip Input (Ch. 2).** This pin is one of the pair of inputs, RRING2/RTIP2, to the differential line receiver at the line interface for the port.
A12	TRING2	AO	**Transmit Ring Output (Ch. 2).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP2/TRING2.
A11	TTIP2	AO	**Transmit Tip Output (Ch. 2).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP2/TRING2.
A5	TTIP3	AO	**Transmit Tip Output (Ch. 3).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP3/TRING3.
B5	TRING3	AO	**Transmit Ring Output (Ch. 3).** This is one of the pair of differential line driver outputs to the line interface pins, TTIP3/TRING3.
B4	RTIP3	AI	**Receive Tip Input (Ch. 3).** This pin is one of the pair of inputs, RRING3/RTIP3, to the differential line receiver at the line interface for the port.
A3	RRING3	AI	**Receive Ring Input (Ch. 3).** This pin is one of the pair of inputs, RRING3/RTIP3, to the differential line receiver at the line interface for the port.
Control and Status Connections			
N15	LOS0	DO	**Loss of Signal Output (Ch. 0).** When LOS0 output is High, it indicates a loss of signal at the port's line interface receiver. LOS goes active after the incoming signal has insufficient transitions for a specified time interval, which is determined by the page and global register settings. The LOS condition is cleared and the output pin returns to Low when the incoming signal has a sufficient number of transitions in a specified time interval, as determined by the register settings.
N13	LOS1	DO	**Loss of Signal Output (Ch. 1).**
M15	LOS2	DO	**Loss of Signal Output (Ch. 2).**
N12	LOS3	DO	**Loss of Signal Output (Ch. 3).**

Table 2. LXT3104BE 256 PBGA Description (Continued)

PBGA	Symbol	I/O	Description
L15	TYPE2	DI	**Microprocessor Type Select Inputs.** These pins control which microprocessor interface is active: TYPE2 TYPE1 Microprocessor 0 0 MPC860, M68360 0 1 i960, i486 1 0 M68302 1 1 8051 mux-mode
K16	TYPE1	DI	
L14	$\overline{CS}$	DI	**Chip Select.** This active Low input initiates each access to the parallel microprocessor interface. For each read or write operation, $\overline{CS}$ must transition from High to Low, and remain Low.
M13	MCLK	DI	**Master Clock Input.** MCLK is an independent, free-running reference clock. The start up frequency is 16.382 MHz for T1/E1/J1 operation. After initialization the frequency can be set to 8, 4, 2 or 1x of the T1/E1/J1 frequency. This reference clock is used to generate several internal reference signals: • Timing reference for the integrated clock recovery unit. • Timing reference for the integrated digital jitter attenuator. • Generation of RCLK signal during a loss of signal condition. • Reference clock during a blue alarm transmit all ones (TAOS) condition. • Reference timing for the parallel processor wait state generation logic.
J14	RBIAS	AI	**Resistor Bias Input.** A 30K Ω, 1% ±100 PPM/°C, resistor must be connected from this pin to analog ground.
H16	OE	DI	**Output Driver Enable Input.** If this pin is asserted low every port's analog driver/ transmitter output immediately enters a high impedance state to support redundancy applications without external mechanical relays. All other internal circuitry stays active. TTIP and TRING for each port can also be tristated individually by writing a '1' to the TXPD bit in "Port Master Control Page Register, 01h" on page 65 or the OES bit in the "Transmit Control Page Register, 03h" on page 66. Please refer to "Transmit Idle Operation and Tristating Drivers" on page 43 for details.
H14	DB0	DI/O	**Data Bus Input/Output.** When a non-multiplexed microprocessor interface is selected, these pins function as a bi-directional 8-bit data bus. When a multiplexed microprocessor interface is selected, these pins carry both bi-directional 8-bit data and address inputs A0 - A7.
G16	DB1	DI/O	
J13	DB2	DI/O	
G14	DB3	DI/O	
H13	DB4	DI/O	**Data Bus Input/Output.** When a non-multiplexed microprocessor interface is selected, these pins function as a bi-directional 8-bit data bus. When a multiplexed microprocessor interface is selected, these pins carry both bi-directional 8-bit data and address inputs A0 - A7.
F14	DB5	DI/O	
F15	DB6	DI/O	
E16	DB7	DI/O	
E15	AD0	DI	**Address Bus Input.** In non-multiplexed mode these inputs function as address input pins for the microprocessor bus. In muxed mode (8051), all pins must be tied low.
D16	AD1	DI	
F13	AD2	DI	
D15	AD3	DI	
C16	AD4	DI	
D14	AD5	DI	
E13	AD6	DI	
C15	AD7	DI	
B16	$\overline{RW}$	DI	This pin has one of two functions depending on the microprocessor interface selected by the TYPE1 and TYPE2 inputs. • **Read/Write Input** (Motorola Mode). • **Write Enable Active Low Input** (Intel mode).

Table 2. LXT3104BE 256 PBGA Description (Continued)

PBGA	Symbol	I/O	Description
D13	$\overline{DS}$	DI	This pin has one of two functions depending on the microprocessor interface selected by the TYPE1 and TYPE2 inputs. • **Data Strobe Input** (Motorola Mode). • **Read Enable Active Low Input** (Intel mode)
D12	$\overline{RDY}$	DO	This pin has one of two functions depending on the microprocessor interface selected by the TYPE1 and TYPE2 inputs. • **Data Transfer Acknowledge Output.** (Motorola Mode). • **Ready Output** (Intel mode).
			Motorola Mode: A Low signal on ACK during a read operation indicates that the information on the data bus is valid. A Low signal during a write operation acknowledges that a data transfer into the addressed register has been accepted (acknowledge signal).
C14	MPI_CLK/ ALE	DI	This pin has one of two functions depending on the microprocessor interface selected by the TYPE1 and TYPE2 inputs.
			Address Latch Enable Input (Intel Mode). • The address on the multiplexed address/data bus is clocked into the device with the falling edge of ALE.
			Microprocessor Clock (Intel i486 Mode). • This pin is used to input the microprocessor clock in the synchronous i486 mode.
B15	$\overline{INTR}$	DO	**Interrupt.** This active Low, maskable, open drain output requires an external 10k pull-up resistor. If the corresponding interrupt enable bit is enabled, $\overline{INTR}$ goes Low to flag the microprocessor when the LXT3104 changes state (see details in the interrupt handling section). The microprocessor interrupt input should be set to level triggering.
R16	JRST	DI	**JTAG Controller Reset Input.** Input is used to reset the JTAG controller. This pin should be tied to ground through a 1K resistor.
R15	TMS	DI	**JTAG Test Mode Select Input.** Used to control the test logic state machine. Sampled on rising edge of TCK. TMS is pulled up internally and may be left disconnected.
P16	TDO	DO	**JTAG Data Output.** During JTAG operation, this pin is Test Data Output for JTAG. Used for reading all serial configuration and test data from internal test logic. It is updated on falling edge of TCK.
P15	TDI	DI	**JTAG Data Input.** This pin is Test Data input for JTAG. Used for loading serial instructions and data into internal test logic. Sampled on rising edge of TCK. TDI is pulled up internally and may be left disconnected.
N16	TCK	DI	**JTAG Clock Input.** This pin is clock input for JTAG. Connect to GND when not used.
P14	$\overline{RSTB}$	DI	**Reset.** This pin is the reset pin for the LXT3104 quad LIU. One microsecond after $\overline{RSTB}$ goes Low, the internal registers will be restored to their default values.
D3	NC		**This pin must be left floating.**
D1	NC		**This pin must be left floating.**
D2	NC		**This pin must be left floating.**
E2	NC		**This pin must be left floating.**
F4	NC		**This pin must be left floating.**
F1	NC		**This pin must be left floating.**
L1	NC		**This pin must be left floating.**
K2	NC		**This pin must be left floating.**
L4	NC		**This pin must be left floating.**
M4	NC		**This pin must be left floating.**
M3	NC		**This pin must be left floating.**

Table 2. LXT3104BE 256 PBGA Description (Continued)

PBGA	Symbol	I/O	Description
N1	NC		**This pin must be left floating.**
N14	NC		**This pin must be left floating.**
M16	NC		**This pin must be left floating.**
L16	NC		**This pin must be left floating.**
M14	NC		**This pin must be left floating.**
K15	NC		**This pin must be left floating.**
J16	NC		**This pin must be left floating.**
M9	NC		**This pin must be left floating.**

3.0 T1/E1 Nomenclature

The nomenclature in this document follows telecommunication industry standard conventions, i.e., bit, channel, and frame numbering increase sequentially with time. In the case of bit ordering, unless otherwise stated, the Most Significant Bit (MSB) is transmitted first and is designated Bit 1.

4.0 LXT3104 Nomenclature

The LXT3104 is a quad device, meaning that it supports up to four T1/E1/J1 ports. The ports are numbered sequentially, beginning with one (1) and ending with four (4).

A port is defined as the standard 4-wire receive/transmit pair T1/E1/J1 interface.

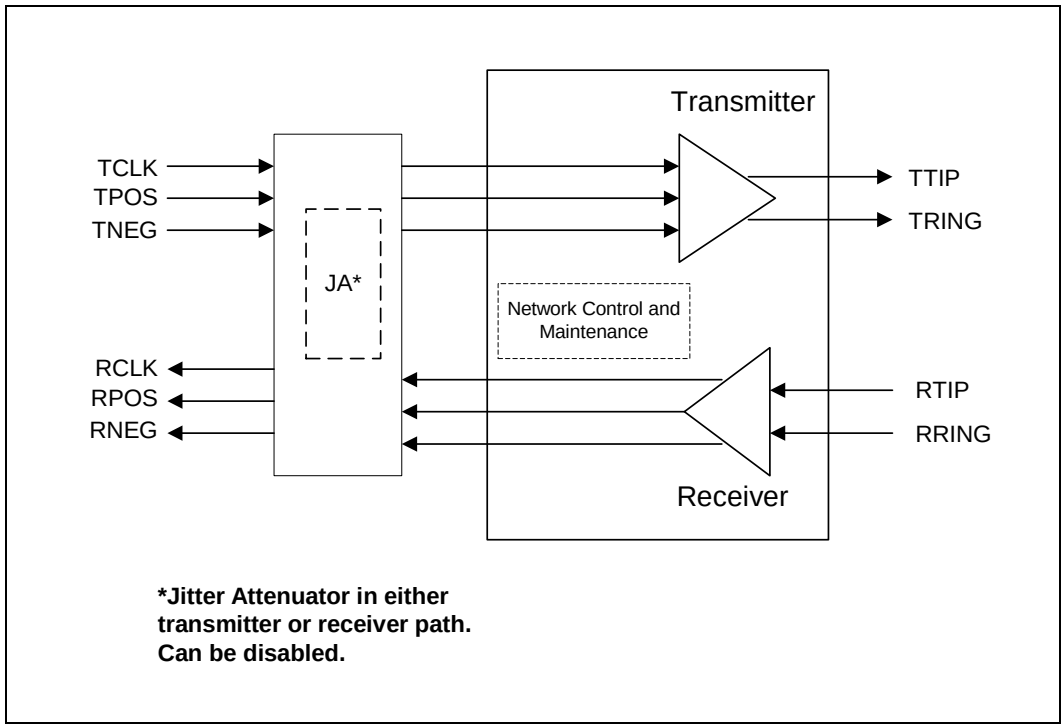
Port and channel are used interchangeably in this document and all related documents.

5.0 Functional Description

The LXT3104 is a port-by-port programmable, fully integrated four-port LIU with jitter attenuator, as well as network control and maintenance functions. Each LXT3104 port is suitable for mixed LH or SH, T1/E1/J1 telecommunications applications allowing full-duplex transmission of digital data over existing cable installations. Under microprocessor control and with a single MCLK source, each port can individually operate:

- at either T1/J1 or E1 line rates
- at separate line termination impedance settings
- with default or programmable transmit signal
- with preset or customized receiver sensitivity
- with the jitter attenuator in either the transmit or receive path, or disabled
- with or without zero suppression line coding

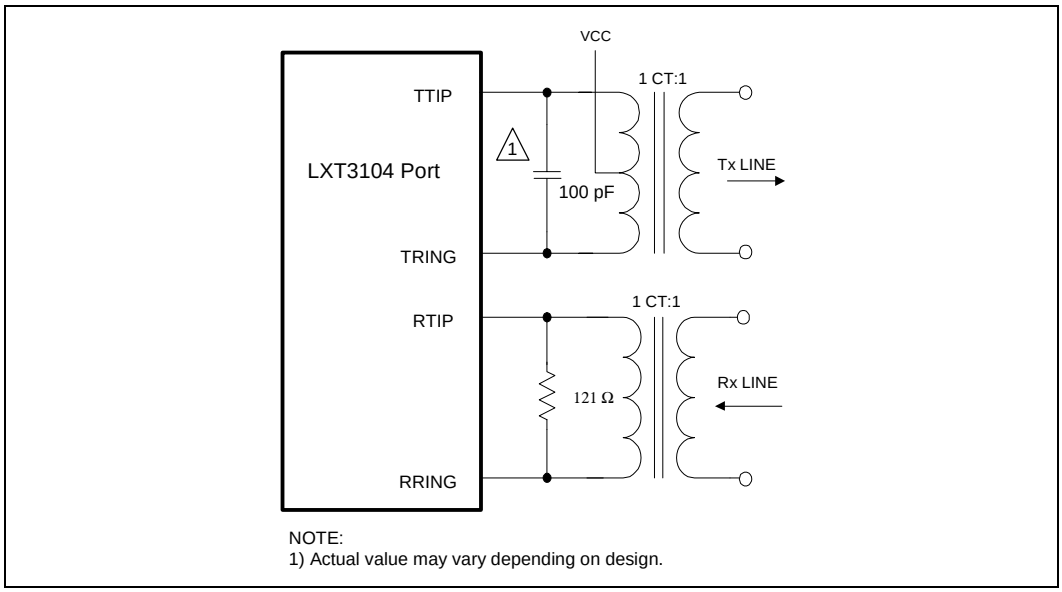
Figure 4. LXT3104 Port Block



An eight-bit wide data bus conveys commands from a microprocessor to each port individually or all ports at the same time by a two-step process. First, writing the port number to the global register described in Table 17, “Port Page Select Register, CPS, 00h” on page 62 chooses the port. The next read or write operation can then reach one of the 32 Port Page Registers (PPRs) adjusting preset port parameters. Besides the PPRs, the designer can also access 48 ATWG registers described in Table 41, “Transmit Coefficient Page Register Range, 40h-6Fh” on page 72.

The LXT3104 is fully T1/E1/J1 selectable without the need to change any external components for twisted pair applications, allowing the development of a single board design to support T1 and E1 designs. The J1 line rate and transformer configuration are the same for T1 and J1 cable. T1 will refer to both T1 and J1 operation throughout this document. The line interface to the cables is through standard T1 and E1 telecommunications transformers and resistors. Each LIU front-end interfaces with two twisted pairs: one pair for transmit, and one pair for receive. These two pairs comprise a digital data loop for full duplex transmission.

Figure 5. LXT3104 Port Circuit



Framed or unframed data clocked by TCLK to TPOS/TNEG or TDATA inputs activates the wave-shaping and line driver circuits. The port's transmitter will drive T1 or E1 lines from TTIP and TRING pins out to standard telecommunications T1 or E1 transformers. The line driver can handle both LH and SH lines for T1/E1/J1.

Preset and programmable pulse shaping suits both LH and SH environments. Each port provides eight built-in equalization settings for SH applications and six line build outs for LH applications. In addition, the Intel PTM software allows the transmitter performance to be tuned for a wide variety of line conditions or special applications. The PTM software provides eight bits of amplitude resolution and either 15 (T1) or 16 (E1) phases of time resolution for up to three Unit Intervals (UI). The combination of proven preset wave-shaping settings and the PTM software means the designer has increased flexibility in meeting design challenges of copper interfaces.

A simplified transmitter circuit configuration offers:

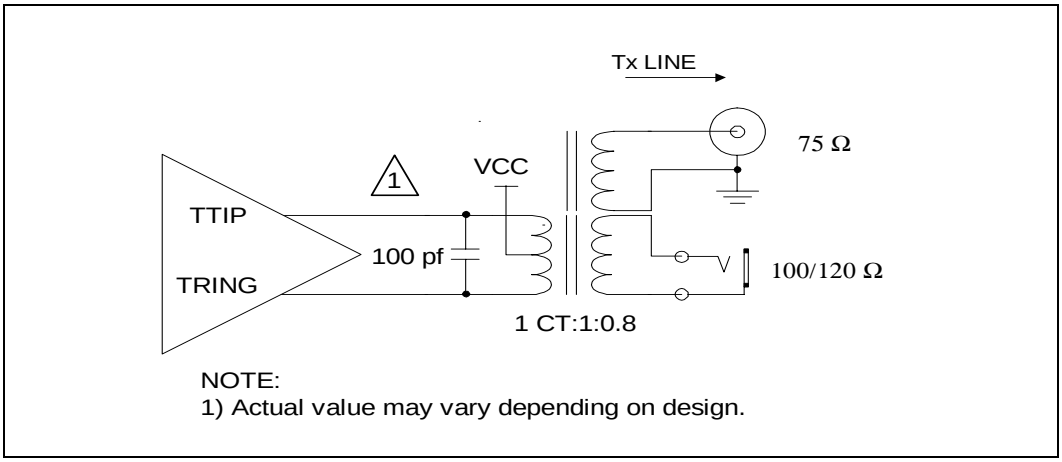
— Port-by-port programmable line impedance matching.

— Reduced port component count.

— Current limiting for short-circuits.

By programming the internal transmitter termination, matching the line impedance requires no component changes for twisted pair and coaxial cable applications, as shown in Figure 6.

Figure 6. Transmitter Circuit for Twisted Pair and Coaxial Cable



Trimming each port's transmitter circuit components to a single transformer and a capacitor increases design flexibility. The transmitter's current mode driver is self-limiting to provide built in short circuit protection. Efficient and flexible line circuit configuration increases designer options and maintains line protection.

A single mandatory clock reference, MCLK, shared between all eight clock recovery circuits, enables each receiver in the LXT3104 to recover the clock and data signals from the line interface. When selected, after smoothing the recovered signals through the jitter attenuator, RCLK clocks out RDATA or RPOS/RNEG at the port's digital framer interface. Each port's receiver dynamic range is from 0 to -43 dB for E1 operation and 0 to -36 dB for T1 operation. This translates to cable reach of at least 2.5 kilometers on 0.63 mm cables (E1) and at least 6000 feet on 22 AWG cables (T1).

The analog AMI waveform from the E1, T1, or J1 line is transformer coupled into the port's RTIP and RRING pins through the LXT3104's internal receive termination. This programmable input termination can select between 100, 110, or 120 Ω applications, eliminating the need to change external components for twisted-pair cable. The designer has the option of selecting by software the internal receive line termination, or bypassing this option with external terminating resistors. See Figure 6 for operating 75 Ω cable.

6.0 Software Support

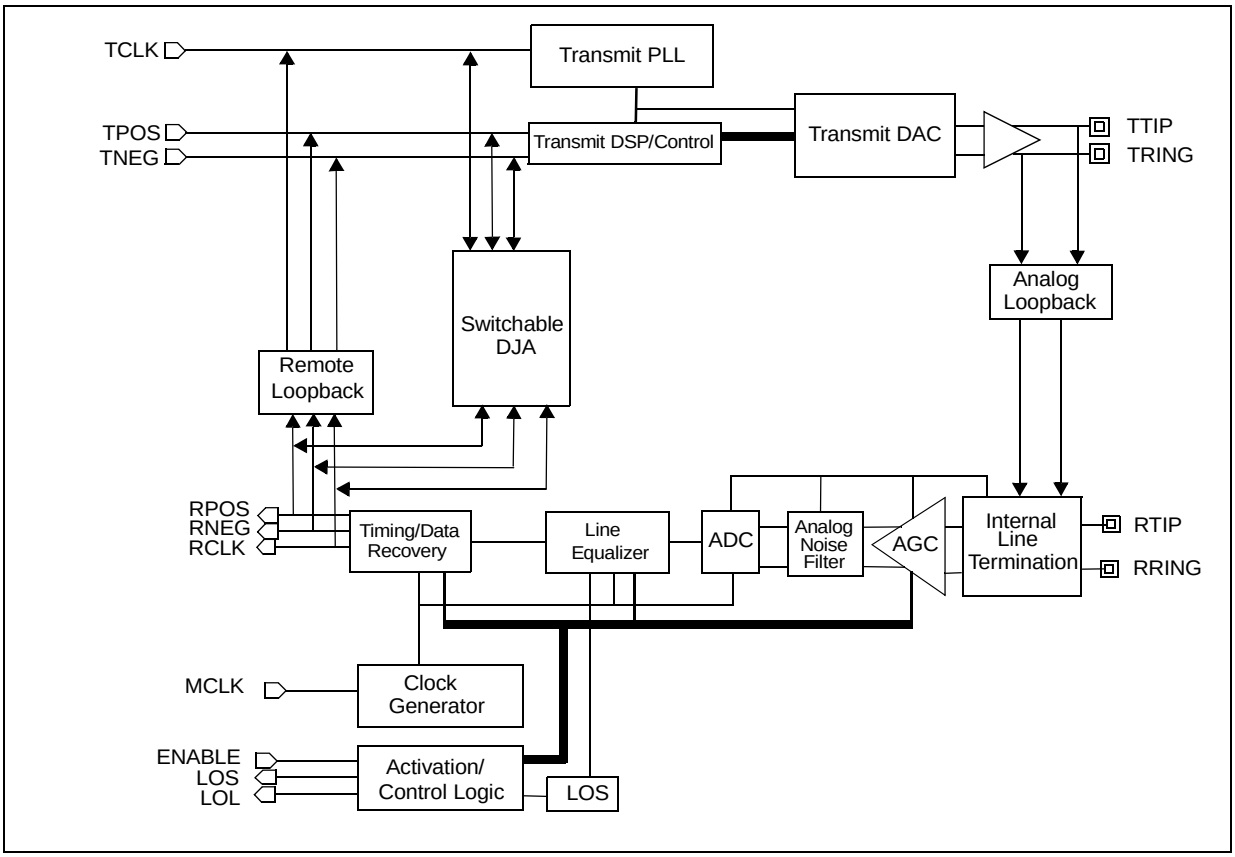
The LXT3104 comes with a complete set of software support. The various software modules allow you to:

- **Configure the device through a Graphical User Interface (GUI).** The LXT3104 GUI software allows you to configure the LXT3104 without having to worry about which bits to set in a particular register. Configuration of the LXT3104 can be accomplished by a series of mouse clicks within the GUI. Configurations can be saved as a series of LXT3104 API messages, which can be used by client applications. Additionally, the LXT3104 GUI allows you to monitor the performance of the device, as well as poll the interrupts.
- **Develop customized applications using the LXT3104 Application Programming Interface (API).** The LXT3104 API is an open source, ANSI C standard library that allows you to develop custom applications for communicating with the device. Programming with the API improves development time by relieving the programmer of having to know the register specifics of the LXT3104. The LXT3104 API complies with the Intel® IXA architecture for compatibility with other Intel communication building blocks.
- **Fine-tune the pulse shape of the device using the Intel® Pulse Template Matching (Intel® PTM) software.** The Intel PTM software provides a graphical view of the transmitting pulse shape (T1, J1 or E1) that the LXT3104 generates. PTM allows you to adjust the pulse shape to fit its respective template, without having to manually manipulate register settings. The PTM software, through the use of graphical controls, automatically adjusts the register settings of the LXT3104 for you. This simplifies the process of fine-tuning the pulse shape, which leads to faster development time.

7.0 LIU Functional Description

Each port consists of a transmitter and a receiver with a jitter attenuator switched between each path. Access to the host device is via a microprocessor parallel interface configured in either Intel or Motorola mode. JTAG built-in test chains enable verification on-board of digital pins and functions.

Figure 7. T1/E1/J1 LIU Block Diagram



Each of the four transmitters consists of a current mode output driver, a second-order charge pump Phase Lock Loop (PLL), a simple digital Finite Infinite Response (FIR) filter, and a switched-current Digital to Analog Converter (DAC). The FIR filter, in combination with the transmitter DAC, provides shaped pulses fitting the pulse shape to the various T1 and E1 pulse templates. A ROM is used to store coefficients and settings for the digital transmit waveform generator.

Each of the four receivers' Analog Front Ends (AFE) consists of an Automatic Gain Control (AGC) amplifier, anti-aliasing filter, and Analog to Digital Converter (ADC). The digital section consists of a digital noise filter, a root-f equalizer, a decision feedback equalizer, timing recovery, and adaptation control logic, as shown in Figure 7 on page 35. A ROM is used to store coefficients and settings for the receiver digital filters.

The programmer controls overall device operation of the LXT3104 through global registers. Each individual LIU is separately controlled by a set of PPRs. There are four sets of PPRs, one for each port. It is also possible to write to all ports at the same time in the case where all ports need to be set up with the same configuration.

The LXT3104 jitter attenuator enhances compatibility with the existing network by complying with jitter control standards The jitter performance of the LXT3104 conforms to the stringent specifications of AT&T Pub. 62411 and ITU TBR12/13. The jitter attenuator is completely digital and does not require an external crystal. The LXT3104 has the capability to insert a Jitter Attenuator (JA) in either the transmit or receive data path individually for each port.

8.0 Initialization

During power up, the Power-On-Reset (POR) circuit initiates a reset sequence after the power supply reaches approximately 60% of VCC. During power-up, an internal reset places all registers to their default values and resets the status and state machines for LOS and AIS. MCLK is mandatory for chip operation.

8.1 Reset Operation

The LXT3104 can be reset in two ways:

1) Writing to the reset bit as shown in the "Port Page Select Register, CPS, 00h" on page 62.

2) Asserting the reset pin low. In software, writing to the reset bit initiates a 1 microsecond reset cycle.

The reset pulse width must be a minimum of 500 µs, and then it is recommended to wait for another 500 µSec after reset is de-asserted before performing any read/write access to the port registers.

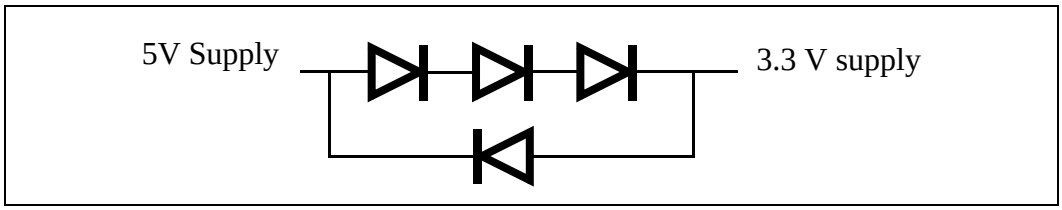
This operation sets all LXT3104 registers to their default values. In the same way, setting the hardware reset pin, $\overline{\text{RSTB}}$, low forces a reset condition and places all registers at their default values.

8.2 5V Tolerant I/O Pins

All digital input pins will tolerate 5.0 volts and are compatible with TTL logic. Please note that it is recommended to keep digital input pins less than 2 volts above the analog and digital supplies. The 5.0 V-tolerance of the LXT3104 is only applicable when the 3.3V (nominal) supplies are present.

Note: External devices such as pull-up resistors, TTL logic, microprocessors, and system-bus peripherals are potential sources of 5V signals to the digital pins. Power-cycling and power-supply failure can potentially cause situations where the LXT3104 is powered down, while external 5V devices are powered up. If the power supply is not guaranteed to prevent this situation, a diode network can be used as shown in Figure 8. The diodes must be capable of handling the entire load capacity of either the 3.3V or 5V supply, whichever is greater.

Figure 8. Diode Protection Network When Inputs Power Up Before Supplies



If the 5V supply fails, it be will held up to around 2.6 volts by the 3.3V supply. If the 3.3V supply fails, it will be held up to around 2.9 volts by the 5V supply. Each of these conditions is safe for the 5V tolerant pins.

8.3 Power Supply Requirements

This section identifies recommended practice for layout and decoupling of power and ground planes.

Long-term reliability of this device might be compromised if these guidelines are not followed.

8.3.1 Ground Plane

All ground pins should be connected to a solid ground plane with the shortest possible path to minimize inductive effects. All pins with names containing GND, VSS, or SUB are ground pins. The VMOAT pin should also be connected to the ground plane.

8.3.2 Analog Power Supply

The analog supply pins listed below require a 3.3V (nominal) supply, which should be filtered separately from the digital supply.

- TXVCC
- TVCC
- AVCC
- QVCC

The recommended method is to connect all of the analog pins to a wide PCB trace, and connect one end of the PCB trace to the power plane. Bypass capacitors from the ground plane to the analog supply trace should be placed as close as possible to the following pins:

- A 0.082 µF capacitor between each TXVCC pin and ground.
- A 0.082 µF capacitor between each AVCC pin and ground.
- A 0.082 µF capacitor between each DVCC pin and ground.

It is recommended that analog and digital power comes from the same power supply. To prevent excessive current through the device, due to one of the supplies failing or sequential power-cycling, it is suggested that the supplies be connected back to the same point.

8.3.3 Digital Power Supply

Digital power supply pins, I/O power, and DVCC should be connected to a solid power plane with the shortest possible path. Four 0.01 µF bypass capacitors, one per side, should be placed as close as possible to the LXT3104 to filter the ground and power planes of the circuit board. In addition, the circuit board should contain 10 µF tantalum and 0.01 µF ceramic capacitors where power is supplied to the board.

As with the analog power supply, it is recommended that analog and digital power come from the same power supply. To prevent excessive current through the device, due to one of the supplies failing or sequential power-cycling, it is suggested that the supplies be connected back to the same point.

9.0 Transmitter

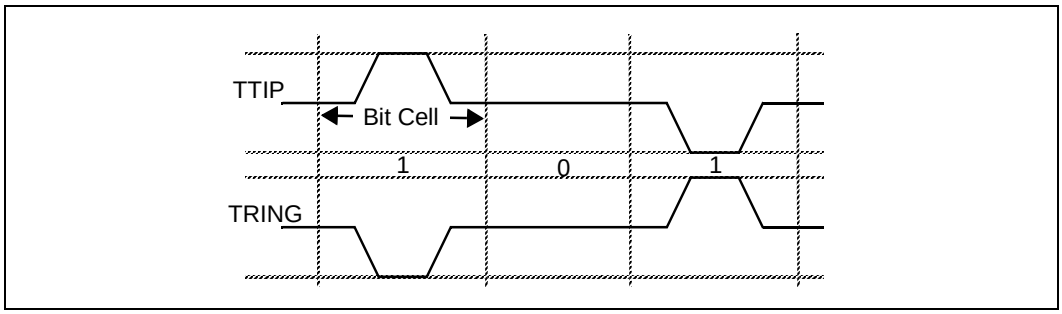
Each of the four ports' transmitters offers several features when interfacing with the framer device's port transmitter control signals TCLK and TDATA or TPOS/TNEG. With TCLK clocking at the line rate and TDATA or TPOS/TNEG carrying digital traffic, the line driver will output a T1/E1/J1 signal through a center tapped 1:1 transformer to the transmit cable pair.

The four low power transmitters of the LXT3104 are identical. Along with fourteen pre-programmed pulse shapes shown in Table 24, "Transmit Control Page Register, 03h" on page 66, the designer may choose the PTM software to tailor pulse shapes to the application. The PTM implements 48 8-bit registers described in Table 41, "Transmit Coefficient Page Register Range, 40h-6Fh" on page 72 that redefine the AMI transmit waveform.

The analog current driver uses programmable internal resistive feedback to synthesize an output impedance of either 100, 110 or 120 Ω for twisted-pair applications. The impedance is programmable through port page register in Table 26, "Termination Control Page Register, 05h" on page 68. When TCLK is not supplied, the transmitter remains powered down and the TTIP/TRING outputs are held in a high impedance state. All eight transmitters can be simultaneously tristated by setting the OE pin low. Also, the programmer can set the port's output enable control bit to individually tristate port transmitters as shown in "Transmit Control Page Register, 03h" on page 66. Please refer to "Transmit Idle Operation and Tristating Drivers" on page 43 for details.

Transmit data is clocked serially into the device at TPOS/TNEG in the bipolar mode or at TDATA in the unipolar mode. The transmit clock (TCLK) supplies the input synchronization. Unipolar I/O is selected by setting the appropriate bits as described in Table 37, "Line Coding Control One Page Register, 1Ch" on page 71. The transmitter samples TPOS/TNEG or TDATA inputs on the falling edge of TCLK. Refer to the Test Specifications Section, Table 52, "Master and Transmit Clock Timing Characteristics" on page 80, for MCLK and TCLK timing characteristics.

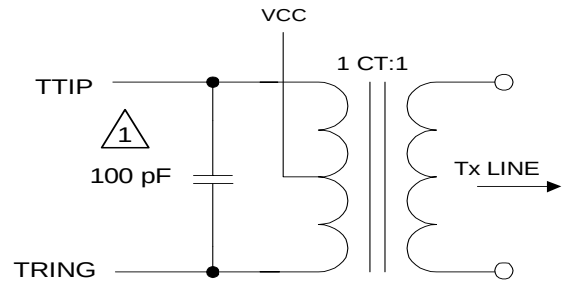
Figure 9. 50% AMI Encoding



9.1 Transmit Line Interface

Each of the four transmitters has pre-programmed and preset pulse shapes suited for driving T1 and E1 twisted-pair cables in LH or SH applications. The signal from TTIP and TRING of each port is coupled to a 1:1 center-tapped transformer as shown in Figure 10.

Figure 10. Typical Transmitter Interface Connections



The 1:1 center-tapped transformer is readily available in many packages as specified below.

Table 3. Transformer Specifications for the LXT3104

Tx/Rx	Frequency MHz	Turns Ratio	Primary Inductance µH (minimum)	Leakage Inductance µH (max)	Interwinding Capacitance pF (max)	DCR Ω (maximum)	Dielectric[1] Breakdown V (minimum)
Tx	1.544/2.048	1 CT:1	600	0.80	60	0.70 pri 1.20 sec	1500 V_{RMS}[2]
Rx	1.544/2.048	1:1	600	1.10	60	1.10 pri 1.10 sec	1500 V_{RMS}[2]

1. Some ETSI applications may require a 2.3 kV dielectric breakdown voltage.
2. Some applications require transformers with center tap on the line side of the transformer (LH applications with DC current in the E1/T1 loop).

The programmer can control from the Port Page Register Bank:

— Matching line impedance of the transmitter in "Termination Control Page Register, 05h" on page 68.

— LH or SH pulse shape "Transmit Control Page Register, 03h" on page 66.

— T1 or E1 port line clock rate "Port Master Control Page Register, 01h" on page 65.

Note: The transformer must be placed no more than one inch from its respective TTIP/TRING pins. If the distance is greater than 1 inch then the PTM software may have to be used to meet pulse template.

9.1.1 Transmit Impedance Termination

The LXT3104's LIU transmitter will synthesize its output impedance to match either a 100 Ω, a 110 Ω, or a 120 Ω line as set by the TXTERM bits in "Termination Control Page Register, 05h" on page 68.

For 75 Ω E1 coax applications, set the termination to 120 Ω and use 1 CT: 0.8 transformer. Refer to Figure 6.

Preset pulse shaping controls the transmit pulse equalization to determine the transmitted pulse shape as shown in Table 24, "Transmit Control Page Register, 03h" on page 66. Table 4 provides more detail about the settings. In order for the port to accurately produce the desired pulse, software must:

- Set T1 or E1 line clock rate in "Port Master Control Page Register, 01h".
- Set transmit line termination in "Termination Control Page Register, 05h".
- Load preset pulse shape setting in "Transmit Control Page Register, 03h".

Table 4. Preset Pulse Shaping Settings and Conditions

T1/E1/J1	TCLK Frequency, MHz	Register Bits 3-0 hex	Cable Range in Feet[1,2] or Line Build Out, LBO	Cable Impedance, Ω	Cable Attenuation, dB
DSX1	1.544	00	• 0 to 133	100	0 to 0.6
DSX1	1.544	01	• 133 to 266	100	0.6 to 1.2
DSX1	1.544	02	• 266 to 399	100	1.2 to 1.8
DSX1	1.544	03	• 399 to 533	100	1.8 to 2.4
DSX1	1.544	04	• 533 to 655	100	2.4 to 3.0
DS1	1.544	05	• 0dB LBO	100	0 to 36
DS1	1.544	06	• -7.5dB LBO	100	0 to 28.5
DS1	1.544	07	• -15dB LBO	100	0 to 21
DS1	1.544	08	• -22.5dB LBO	100	0 to 13.5
E1	2.048	09	• 0 to 655	75	0 to 3.0
E1	2.048	0A	• 0 to 655	120	0 to 3.0
E1	2.048	0B	• up to 2.5 km	75	0 to 43
E1	2.048	0C	• up to 2.5 km	120	0 to 43
J1	1.544	0D	• 0 - 655 ft.	110	0 to 3.0

9.1.2 Transmit Return Loss Performance

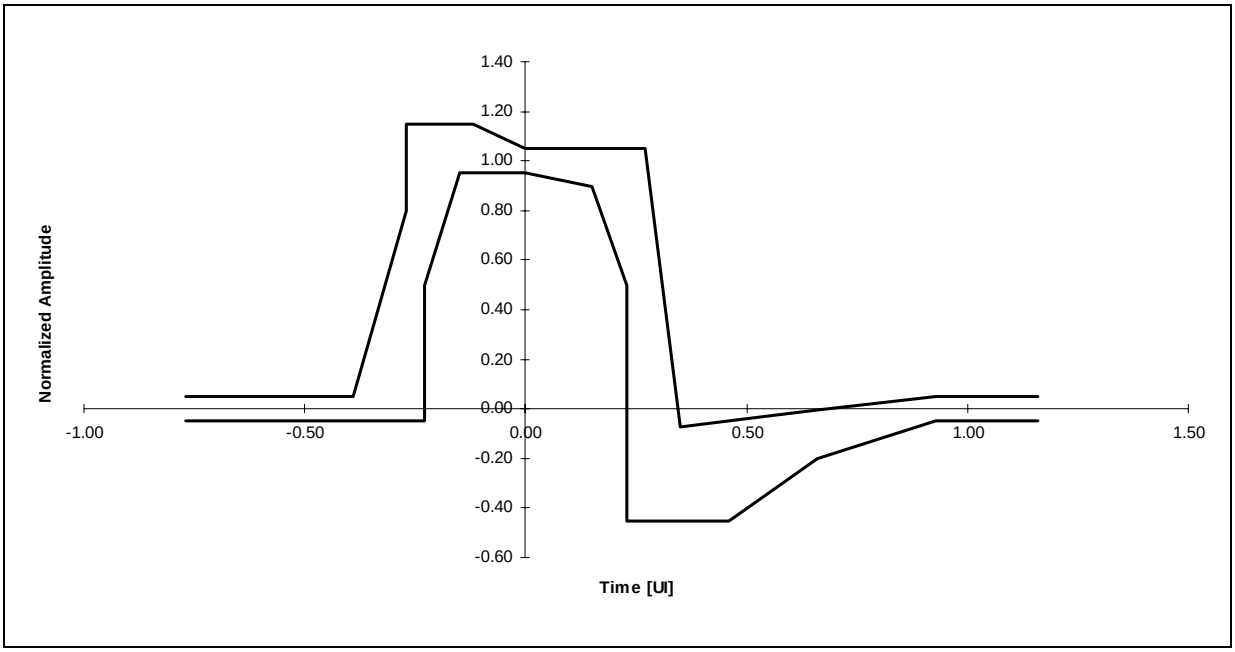
The LXT3104 transmitter will meet the applicable standard for transmit return loss, but there are several requirements. Because transmit return loss depends on the match between transmitter circuit output impedance and the characteristic cable impedance, ITU limits the reflections due to mismatch by specifying minimum transmit return loss. ANSI currently does not specify this parameter. In order to compare T1 performance to E1 performance, the ITU standard is adapted to show a similar T1 minimum return loss. This is a benchmark that might be suitable for some T1 applications.

By appropriate software control of the internal transmit impedance in “Termination Control Page Register, 05h”, the transmit return loss will be maximized. There are three standards that can be checked for minimum transmit return loss. For E1 line rate, ITU G.703 recommends ETSI 300166. For T1 line rate, 0 dB is the de facto standard; however, ETSI 300166 can be adapted to 1.544 MHz, as shown in Table 5.

Table 5. Transmit Return Loss Specifications for Frequency Range and Magnitude

T1/E1	Frequency Band	Transmit Return Loss		
		Actual Performance	ETS 300 166	Notes
E1	51-102 KHz	–	6 dB	ITU G.703 specification
	102-2048 KHz		8 dB	
	2048 - 3072 KHz		8 dB	
T1	39-77 KHz	-	6 dB	Adapted as a benchmark
	77-1544 KHz		8 dB	
	1544 - 2316 KHz		8 dB	

Figure 11. T1, T1.102 Mask Templates



9.1.2.1 Intel® Pulse Template Matching (Intel® PTM)

Each transmit baud, or UI, is divided into either 16 (E1) or 15 (T1) sub-phases. The pulse amplitude during each phase is described by an 8 bit, 2's compliment, binary word. Thus, each pulse can be described with a timing resolution of Tper/16 and an amplitude resolution of Full Scale/128. Up to 48 transmit words can be used, allowing each shaped pulse to extend up to three baud. Typically SH pulses use only 15 or 16 words, although all 48 bytes are available. LH pulse shaping may extend over three baud.

To use the PTM, two operations must take place.

- The desired 8-bit words must be loaded into the LXT3104's LIU local memory. This can be done through a host API. The coding is 2's complement from +127 to -127 where a code of +127 creates a full scale pulse at the output. Each LSB is approximately 1/127 of FS. Care must be taken by the users, as it is possible to create nonsensical pulse shapes either by mis-coding or by saturating the DAC.
- After the words are loaded, assert ATWG_EN by loading value "01h"as shown in "Transmit Control Page Register, 03h" on page 66.

The transmit DAC will use the codes from the local ROM registers. These settings are maintained as long as power is applied to the device and reset is not asserted. They can be overwritten at anytime and are not lost when the transmitter is powered-down as shown in Figure 13 on page 44. The contents of the local memory are lost when power is removed from the chip and initialized to all zeros when reset is asserted.

Note: The user must be careful not to assert ATWG_EN if the contents of the local memory have not been properly initialized.

Adjustments to the output signal can be made using the Intel PTM software. The Intel PTM software simplifies the process of modifying the output signal by handling all of the register manipulation for you.

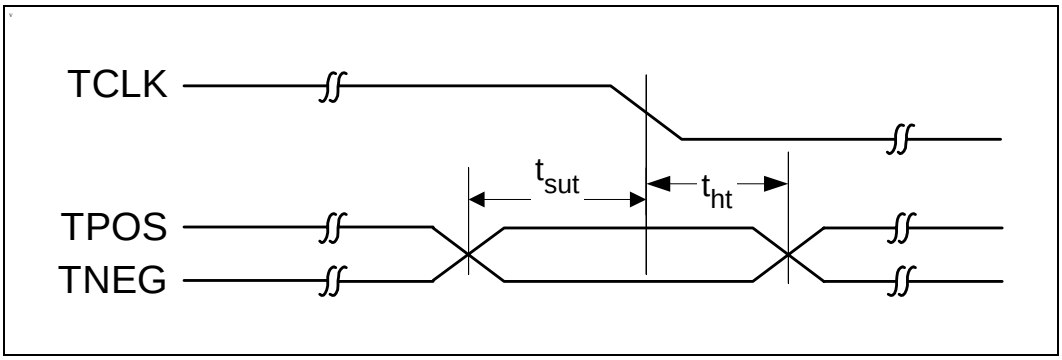
9.2 Transmit Digital Interface

Input data for transmission onto the line is clocked serially into the device at the TCLK rate. TPOS and TNEG are the bipolar data inputs, and TDATA accepts unipolar data. Software controls how input data passes through:

- The jitter attenuator, according to "JA Control Two Page Register, 1Dh" on page 72.
- The B8ZS/HD3 encoder, according to "Line Coding Control One Page Register, 1Ch" on page 71.

Data is clocked on the falling edge of TCLK as shown in Figure 12, "Transmit Interface Timing" on page 43.

Figure 12. Transmit Interface Timing



9.2.1 Transmit Idle Operation and Tristating Drivers

When the transmitter is not being used, the designer conserves power by powering down the driver circuit. There are two ways to power down the transmitter:

- Hold port TCLK high for 16 clock cycles.
- Assert the TXPD bit in "Port Master Control Page Register, 01h" on page 65, in software.

In this state, TTIP and TRING are at high impedance, and all of the analog circuitry associated with the transmitter is turned off. After restarting TCLK or clearing the TXPD bit, it may take several milliseconds for the transmitter to achieve steady state performance.

For redundancy applications, it is desirable to tristate each driver while leaving the transmitter circuitry turned on. In this case, there are three ways to tristate the drivers:

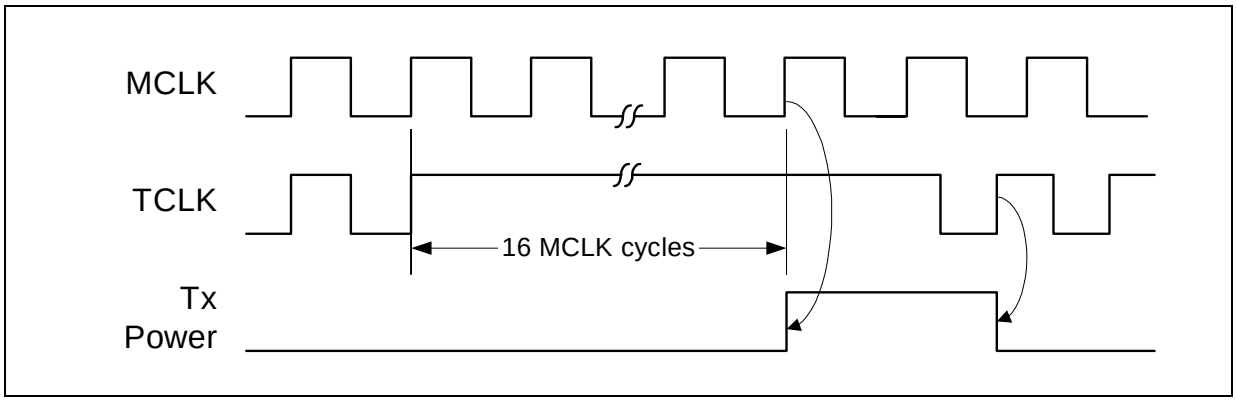
- Hold port TCLK low for 16 clock cycles.
- Set the OE pin low, which affects all four ports at the same time.
- Set the OES bit high in "Transmit Control Page Register, 03h" on page 66.

In this state, TTIP and TRING will enter a high impedance state. However, in this state the transmitter will remain powered up. This will allow two transmitters to be connected in parallel for redundancy applications.

Table 6. Powering Down the Transmitter with Static TCLK

TXCLK	Effect
TXCLK = 1 > 16 MCLK cycles OR TXPD = 1	Transmitter enters Powered-down State. TTIP & TRING enter high impedence state.
TXCLK = 0 > 16 MCLK cycles	TTIP & TRING enter high-impedance state.

Figure 13. TCLK Power Down Timing



10.0 Receiver

The four receivers in the LXT3104 are identical but operate independently. The following paragraphs describe the operation of one receiver.

The receiver is coupled to the line through a 1:1 transformer. The input common mode level is set on-chip. Recovered data is presented at the port's RPOS/RNEG or RDATA pins. The recovered clock is present at the port's RCLK pin. Upon loss of signal, RCLK is derived from MCLK. Refer to the test specification section for receiver timing.

10.1 Master Reference Clock

The MCLK input to the LXT3104 is an 8.192 MHz clock. MCLK is mandatory for device operation.

The data and timing recovery circuits provide input jitter tolerance significantly better than required by AT&T Pub 62411 and ITU G.823. See the Test Specifications section Table 45 to Table 55 and Figure 26 to 32 for more information.

10.2 Receiver Digital Interface

The recovered data goes to the Loss of Signal (LOS) Monitor and through the Alarm Indication Signal (AIS, Blue Alarm) Monitor. Received data may go through either the B8ZS or HDB3 decoder or neither. Finally, the data is sent to the framer either as unipolar or bipolar data on the RDATA or RPOS/RNEG pins, and the recovered clock drives the RCLK pin. Received data is clocked out of the LIU on the rising edge of RCLK as shown in Figure 14. The receiver LOS function monitors the received signal level and indicates if the signal drops below the levels given in Table 2.

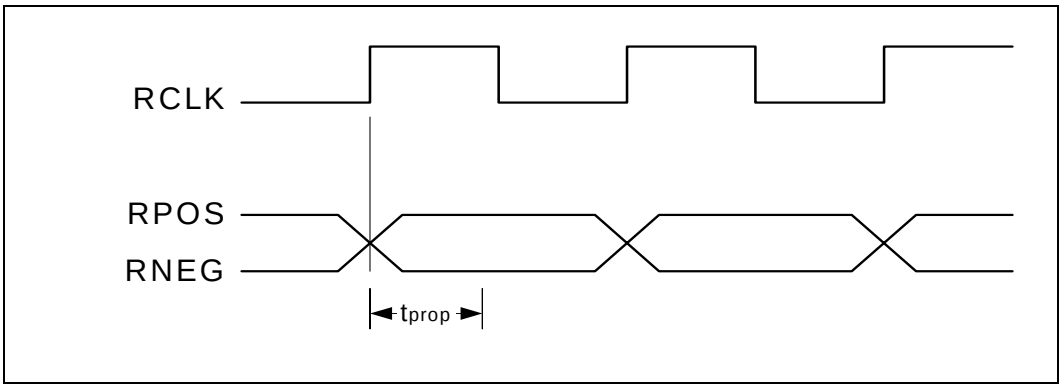
With AMI encoding/decoding, the receiver reports detecting bipolar violations by setting the BPV pin high and incrementing the BPV counter in T1 operation. With B8ZS (T1 operation) or HDB3 (E1 operation) encoding/decoding, the device reports B8ZS/HDB3 code violations and zero substitution violations also incrementing the BPV counter.

10.2.1 Receiver Idle Conditions

The receiver powers down and tristates the digital pins RCLK, RPOS/RDATA, and RNEG under either of the following conditions:

- When the RXPD bit described in "Port Master Control Page Register, 01h" on page 65 is set.
- When the CHANEN bit described in "Port Receive Enable Page Register, 02h" on page 65 is set.

Figure 14. Receiver Output Timing



10.3 Receiver Line Interface

The LXT3104 receiver line interface provides:

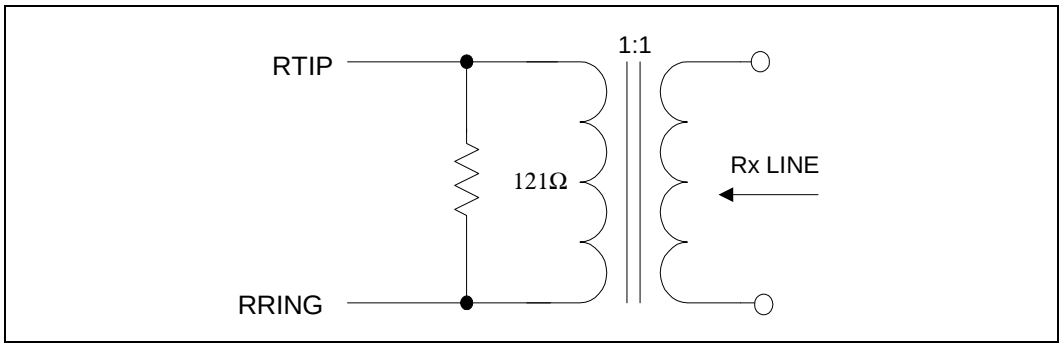
- Programmable line termination described in "Termination Control Page Register, 05h" on page 68.
- Programmable sensitivity described in "Receive Control Page Register, 04h" on page 67.
- Monitor mode, also in "Receive Control Page Register, 04h".

The LXT3104 internally terminates the input line for twisted pair applications with a combination of a single external resistor and programming the termination register to match the line impedance. An advanced DSP- based receiver provides equalization and timing recovery for signals with up to -43 dB of cable loss (E1) or -36 dB of cable loss (T1) in the presence of input noise and jitter as specified in ANSI T1.408. The receiver provides up to -43 dB of sensitivity @ 1024 KHz (E1), or up to 36 dB of sensitivity @ 772 KHz (T1) in steps of approximately 2 db under software control as described in "Receive Control Page Register, 04h". The advantage these features provide is industry standard performance without component changes.

10.3.1 Receive Termination Impedance

The receiver is coupled to the line through a 1:1 transformer. Since part of the receive termination is on-chip the input is low impedance.

Figure 15. Typical Receiver Interface Connections



The receive input impedance is set by the parallel combination of a precision external resistor and an internal resistor. With an external resistor of 121 Ω ± 1%, Figure 5, the total input impedance can be set by the user by setting the appropriate bits in register RXTERM, address 05h, in the page registers.

10.3.2 Receiver Sensitivity Programming

Under some conditions, it may be desirable to limit the sensitivity of the receiver. This can be done by programing "Receive Control Page Register, 04h" on page 67. This limits the range of the receiver equalizer to the approximate values shown in Table 7. The designer selects the affected port as described in the "Port Page Select Register, CPS, 00h" on page 62 for all ports simultaneously or for each port individually.

Table 7. Receiver Sensitivity

RXCON RX[4:0] hex	T1/E1	Maximum receiver sensitivity (dB)	T1/E1	Maximum receiver sensitivity (dB)
00	E1	-43	T1	-36
01		-40		-34
02		-38		-32
03		-36		-30
04		-34		-28
05		-32		-26
06		-30		-24
07		-28		-22
08		-26		-20
09		-24		-18
0A		-22		-28
0B		-20		-26
0C		-18		-22
0D		-16		-20
0F		-14		-18
0F TO 1F		-43		-18

10.3.2.1 Receiver Monitor Mode

The receive equalizer of the LXT3104 can be used in Monitor Mode applications. Monitor Mode applications require a resistive attenuation of the signal in addition to a small amount of cable attenuation (less than 6 dB). Asserting the MON bit in "Receive Control Page Register, 04h" on page 67 configures the device to work in its Monitor Mode. The device must be in its LH receiver mode for Monitor Mode, which is controlled by the RXSH bit in "Receive Control Page Register, 04h".

With the device in Monitor Mode, the receive equalizer handles signals attenuated resistively by 20 to 35 dB, plus 0 to 6 dB of cable attenuation for both E1 and T1 applications.

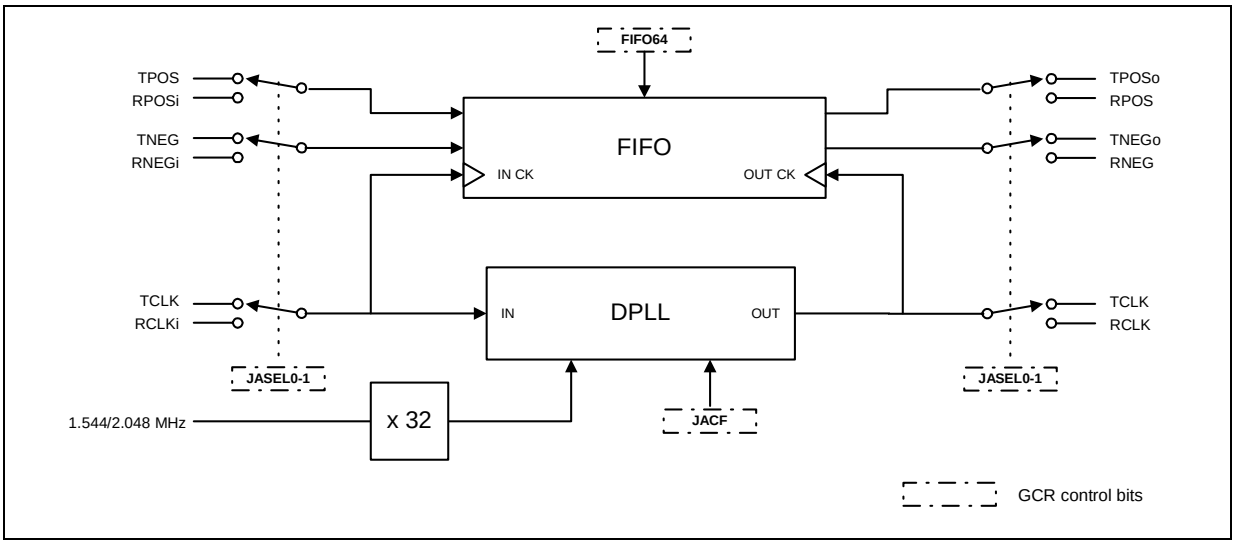
10.4 Receiver Status Information

The status of the receiver can be monitored though "Receiver Equalizer Status Zero Page Register, 06h" on page 68, while equalizer settings can be checked with "Receiver Equalizer Status One Page Register, 07h" on page 68 and "Receiver Equalizer Status Two Page Register, 08h" on page 69. "Receiver Equalizer Status Two Page Register, 08h" contains status bits that indicate LOS, LOL, and overflow conditions in the DSP. The contents of "Receiver Equalizer Status Zero Page Register, 06h"and "Receiver Equalizer Status One Page Register, 07h" can be used to estimate the line attenuation, which can be translated to line length.

11.0 Jitter Attenuation (JA)

A digital Jitter Attenuation Loop (JAL) combined with an Elastic Store (ES) FIFO provides Jitter attenuation. The FIFO depth is selectable for either 32 or 64 bits through "JA Control Two Page Register, 1Dh" on page 72. The JAL is internal and does not require an external crystal or a high-frequency (higher than line rate) reference clock. JA can be placed in either the receive or transmit data path. The "JA Control Two Page Register, 1Dh" selects JA enabled or disabled and selects receive or the transmit path.

Figure 16. Jitter Attenuation Loop



The FIFO is a 32 x 2-bit or 64 x 2-bit register (selected by the register x1D). Data is clocked into the FIFO with the associated clock signal (TCLK or RCLK), and clocked out of the FIFO with the dejittered JAL clock, as seen in Figure 16. When the FIFO is within two bits of overflowing or underflowing, the FIFO adjusts the output clock by 1/8 of a bit period. The Jitter Attenuator produces a constant delay of 16 or 32 bits in the associated path. Please refer to "Test Specifications" for details. This feature can be used for switching redundancy applications. This advanced digital jitter attenuator meets the latest jitter attenuation specifications shown in Table 8.

Table 8. Jitter Attenuation Specifications

T1	E1
AT&T Pub 62411	ITU-T G.735
GR-253-CORE	ITU-T G.742
TR-TSY-000009	ITU-T G.783
	ETSI CTR12/13
	BAPT 220

11.1 Digital Jitter Attenuator (DJA) Status

DJA status detection for both underflow and overflow conditions is reported in "Alarm Status One Page Register, 12h" on page 70. Two maskable processor interrupts for the DJA are controlled by "Interrupt Enable Page Register, 11h" on page 70. Details about both types of DJA interrupt status are reported in "Interrupt Status Two Page Register, 13h" on page 71.

12.0 Network Control and Maintenance Functions

12.1 Diagnostic Modes

The LXT3104 offers the following diagnostic modes:

- Network Loop (NLOOP) Code Generator/Detector.
- Analog loopback (ALOOP) digital transmitter to analog transmitter/receiver pins back to digital receiver pins.
- Remote loopback (RLOOP) analog receiver to analog transmitter pins.
- Digital loopback (DLOOP) digital transmitter to digital receiver pins.
- Transmit All Ones (TAOS) signal sent by transmitter driver to line.

The LXT3104 offers three loopback modes for diagnostic purposes: Analog, Remote, and Digital Loopback. Network Loop codes activate Remote Loopback from a pattern contained in the signal traffic passing through the LIU receiver. Loopbacks are selected by writing to the appropriate port's ALOOP bit in "Port Master Control Page Register, 01h" on page 65, or DLOOP, NLOOP or RLOOP bits in "Loopback Enable Page Register, 10h" on page 70. Transmit All Ones control bit is set in "Transmit Control Page Register, 03h" on page 66.

12.1.1 In-Band Network Loop Up or Down Code Generator/Detector

LXT3104 can transmit in-band Network Loop Up or Loop Down code. The Loop Up code is 00001; Loop Down code is 001. A Loop Up code transmission occurs when the respective bits in register x10 are set. A Loop Down code transmission occurs when the respective bits in register x10 are set.

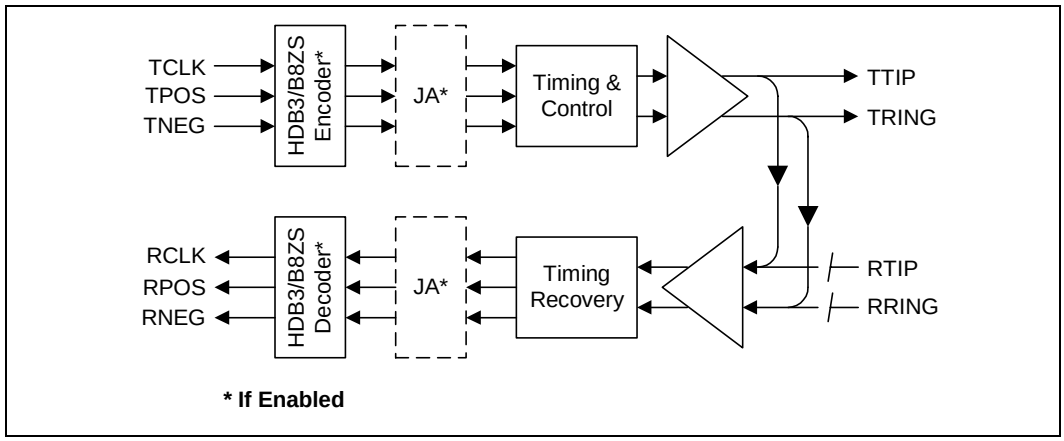
Network Loopback (NLOOP) can be initiated only when the Network Loopback detect function is enabled. Writing a “1” to the NLOOP bit in “Loopback Enable Page Register, 10h”enables this mode.

With NLOOP detection enabled, the receiver looks for the NLOOP data patterns (00001 = enable, 001 = disable) in the input data stream. When the receiver detects an NLOOP enable data pattern repeated for a minimum of five seconds, the device enables RLOOP. The device responds to both framed and unframed NLOOP patterns. Once NLOOP detection is enabled at the chip and activated by the appropriate data pattern, it is identical to Remote Loopback (RLOOP). NLOOP is disabled by receiving the 001 pattern for five seconds, or by activating RLOOP or ALOOP, or by disabling NLOOP detection in software.

12.1.2 Analog Loopback

Analog Loopback (ALOOP) exercises the maximum number of functional blocks. ALOOP operation disconnects the RTIP/RRING signal path inputs from the line and routes the transmit outputs back into the receive inputs. This tests the transmitter, receiver, and timing recovery sections. The ALOOP function overrides all other loopback modes. When analog loopback is selected, the receive line is still terminated by the internal termination. When selected, the transmitter outputs (TTIP & TRING) are connected internally to the receiver inputs (RTIP & RRING) as shown in Figure 17. Data and clock are output at RCLK, RPOS & RNEG pins for the corresponding LIU. Note that signals on the RTIP & RRING pins are ignored during analog loopback. ALOOP bit is in“Loopback Enable Page Register, 10h”.

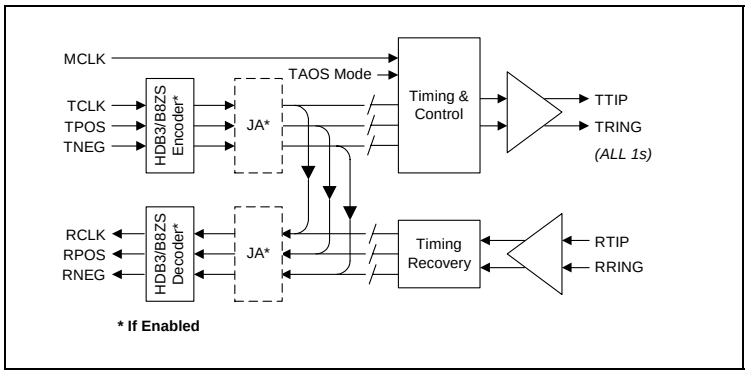
Figure 17. Analog Loopback



12.1.3 Digital Loopback

When digital loopback is selected, the transmit clock and data inputs (TCLK, TPOS & TNEG) are looped back and are output on the RCLK, RPOS, and RNEG pins (see Figure 18). The data presented on TCLK, TPOS, and TNEG is also output on the TTIP and TRING pins. Note that signals on the RTIP and RRING pins are ignored during digital loopback.

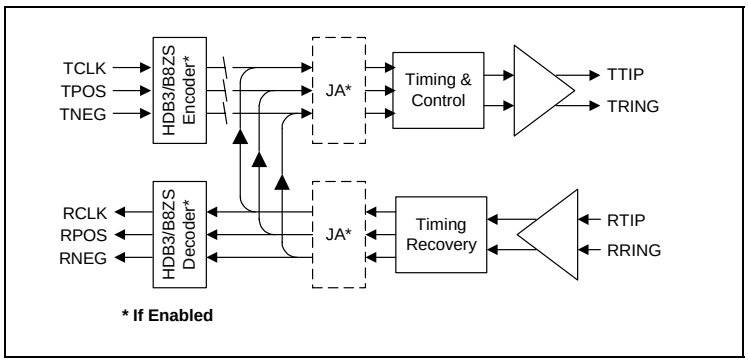
Figure 18. Digital Loopback



12.1.4 Remote Loopback

During remote loopback as shown in Figure 19, the RTIP and RRING inputs are routed to the transmit circuits and are output on the TTIP and TRING pins. Note that input signals on the TCLK, TPOS, and TNEG pins are ignored during remote loopback.

Figure 19. Remote Loopback



12.1.5 Transmit All Ones (TAOS)

TAOS mode is set by asserting TAOS bit in “Transmit Control Page Register, 03h”. Note that the TAOS generator uses MCLK as a timing reference. In order to assure that the output frequency is within specification limits, MCLK must have the applicable stability as shown in Table 52, “Master and Transmit Clock Timing Characteristics” on page 80.

Both DLOOP and ALOOP modes function correctly with TAOS active. However, TAOS is inhibited when RLOOP mode is active.

Figure 20. TAOS Data Path

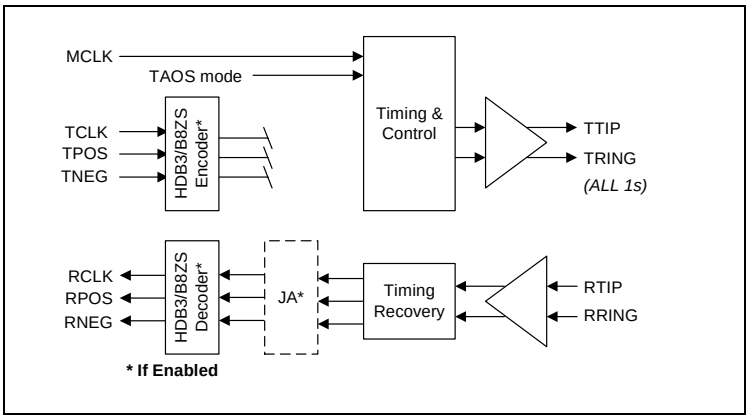


Figure 21. TAOS with Digital Loopback

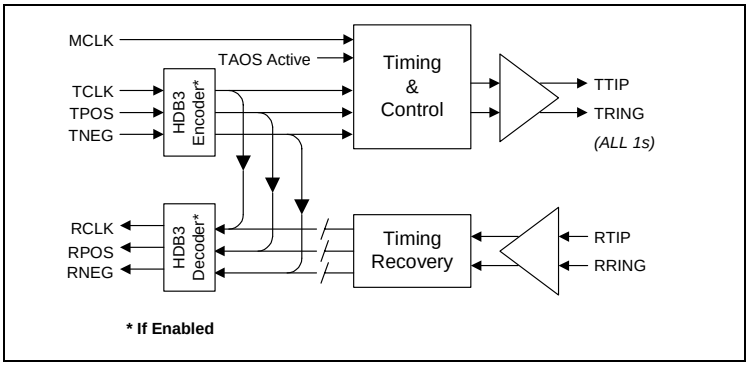
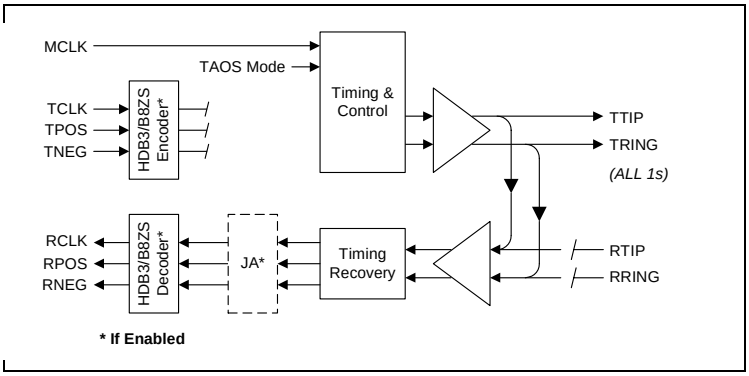


Figure 22. TAOS with Analog Loopback



12.2 Line Coding

This section describes the LXT3104 functionality related to line coding and monitoring.

The LIU's digital framer interface performs two functions:

- Provides a bipolar or unipolar interface to a framer.

- Offers line coding and decoding of AMI, B8ZS, and HDB3.

Each of these functions is described in detail below:

The LIU digital framer interface can be operated in one of two functional modes as described in Table 37, “Line Coding Control One Page Register, 1Ch” on page 71:

- BIPOLAR - Digital Positive/Negative/Clock signals indicating signal polarity.
- UNIPOLAR - Digital Data/Clock indicating NRZ data.

12.2.1 Alternate Mark Inversion (AMI)

(per: ITU G.703)

AMI is a Return-to-Zero (RZ) format where a binary “one” (mark) is represented by either a positive or negative going pulse and a binary “zero” (space) is represented by the absence of a pulse. The LXT3104 supports either of the standards listed below by user selection in Table 37, “Line Coding Control One Page Register, 1Ch” on page 71 as well as Table 30, “LOS Window Page Register, 0Bh” on page 69 through Table 32 on Page 69. AMI coding alone does not provide any method of ensuring compliance to mark/space requirements. The term “AMI coding” is often used to mean that no specific methods are used to suppress excess zeroes in the signal.

— ANSI T1.403:

No more than 15 consecutive zeros.

At least N ones in each and every time window of 8*(N+1) bits, where N = 1 through 23.

— FCC Part 68.318:

No more than 80 consecutive zeroes.

An average ones density of at least 12.5%.

Each consecutive pulse should alternate in polarity (i.e., a positive pulse should always be followed by a negative pulse and a negative pulse should always be followed by a positive pulse) regardless of the number of intervening spaces between the two pulses. AMI comes from this: *alternating marks inversion.* Two consecutive pulses of the same polarity are known as a bipolar violation (BPV). The LXT3104 actively monitors the line signal and provides a count of detected BPVs for performance monitoring purposes. By definition, *all* T1 line signals use basic AMI line coding. However, because T1 receivers rely on the presence of marks in the signal to recover clocking, various standards specify maximum space and minimum mark density requirements. These are cited below.

12.2.1.1 Bipolar with Eight Zero Substitution (B8ZS)

(per: ANSI T1.102)

The LXT3104 allows separately controlled transmit and receive B8ZS encoding for each port at T1 line rate described in “Line Coding Control One Page Register, 1Ch” on page 71. The LXT3104 performs both B8ZS coding (on the T1 transmitted signal) and B8ZS decoding (on the T1 received signal). Received BPVs that are part of the B8ZS pattern are not counted as BPVs in the coding error counter.

B8ZS overcomes limitations of ZCS discussed below and allows the support of clear port (64 kbps) data. It is compatible with all standard T1 framing formats. In B8ZS coding, eight consecutive zeroes in the T1 data stream will be replaced by the B8ZS substitution pattern of “000VB0VB” in which “V” is an intentional BiPolar Violation (BPV) and “B” is a valid bipolar mark. Note that the

polarity of the BPVs and marks depends upon the polarity of the last mark before the “eighth zero” occurs. This substitution is made regardless of where the eight consecutive zeros occur in the datastream, including framing, signaling, and alarm bits. As opposed to ZCS which operates on data within a DS0 port, B8ZS coding can occur across frame boundaries.

12.2.1.2 High Density Bipolar Three (HDB3)

(per: ITU G.703)

The LXT3104 allows separately controlled transmit and receive HDB3 encoding for each port at E1 line rate described in “Line Coding Control One Page Register, 1Ch” on page 71.

Receive side HDB3 decoding is selected by setting the decoding bit in “Line Coding Control One Page Register, 1Ch”. Similarly, transmit side HDB3 encoding is selected by setting the encoding bit in “Line Coding Control One Page Register, 1Ch”. Received BPVs that are part of the HDB3 pattern are not counted as BPVs in the coding violation error counter.

In HDB3 coding, four consecutive zeroes in the E1 data stream will be replaced by the HDB3 substitution pattern of either “000V” or “B00V, in which “V” is an intentional bipolar violation (BPV) and “B” is a valid bipolar mark. This limits the maximum number of consecutive spaces to three. The choice of substitution pattern is made so that the number of B pulses between consecutive V pulses is odd (i.e., successive V pulses are of alternate polarity). This substitution is made regardless of where the four consecutive zeroes occur in the datastream, including framing, signaling, and alarm bits. The LXT3104 performs both HDB3 coding on the E1 transmitted signal and HDB3 decoding on the E1 received signal.

12.3 Network Maintenance Functions

12.3.1 Loss Of Signal (LOS)

While LOS appears at each port's LOS pin, it can be detected by software reading the LOS bit in the "Receiver Equalizer Status Two Page Register, 08h" on page 69. A maskable processor interrupt controlled by "Interrupt Enable Page Register, 11h" on page 70 is available. Details about LOS interrupt status are reported in "Interrupt Status Two Page Register, 13h" on page 71. Depending on whether the port is configured for T1 or E1 service, the LOS will be cleared for the appropriate zeros density after the detection of LOS as discussed below.

Three user registers are provided for customizing the received marks density LOS detector. Users can select:

- The number of consecutive spaces that must be received to declare LOS in "LOS Window Page Register, 0Bh" on page 69.
- The number of marks that must be received within that window to clear LOS "LOS Set Threshold One Page Register, 0Ch" on page 69.
- The number of consecutive zeros that, if received while LOS is asserted, will continue to re-assert LOS in "LOS Reset Threshold Two Page Register, 0Dh" on page 69.

The default values are given in Table 9. Each receiver has a multi-function LOS detector that is used to meet ITU T1.231 or G.775 requirements for T1 or E1 systems.

These detectors monitor both the received signal amplitude and the received marks density according to the following table.

Table 9. LOS Selection Defaults

T1/E1	Window Size	Marks in Window to Clear	Marks in Window to Reset
T1	175	21	100
E1	32	4	16

Users may change these values by setting the USR_LOS bit in "Port Master Control Page Register, 01h" on page 65. If this bit is set, then the desired LOS Window, LOS Set, and LOS Reset values must be programmed for proper LOS operation.

For E1 SH operation the LOS operates based on the peak received amplitude during a fixed window. For G.775 the window length can be programmed by "LOS Window Page Register, 0Bh".

A minimum data density of 1 in 16 is required to clear LOS.

The receiver monitor loads a digital counter at the RCLK frequency. The counter will increment each time a zero is received and reset to zero each time a one (mark) is received. Depending on the operation mode, a certain number of consecutive zeros sets the LOS signal. The recovered clock is replaced by MCLK at the RCLK output with a minimum amount of phase errors. (MCLK is required for receive operation). When the LOS condition is cleared, the LOS flag is reset and another transition replaces MCLK with the recovered clock at RCLK. RPOS/RNEG will be high during the entire LOS detection period for that port.

12.3.2 Alarm Indication Signal (AIS)

Alarm Indication Signal reports all ones signal received at RTIP and RRING pins. Once AIS is detected, the port status flag is set in "Alarm Status One Page Register, 12h" on page 70. A maskable processor interrupt controlled by "Interrupt Enable Page Register, 11h" on page 70 is available. Details about AIS interrupt status are reported in "Interrupt Status Two Page Register, 13h" on page 71. Depending on whether the port is configured for T1 or E1 service, the AIS will be cleared for the appropriate zeros density after the detection of AIS as shown below.

Table 10. AIS Service Condition Variations

T1/E1	Window Size	Spaces in Window to Clear	Spaces in Window to Reset
T1	3 msec.	6	5
E1	512	3	2

(per: ITU G.775)

E1 AIS is declared when less than three spaces (i.e., 2 or less zeros) are detected in a 250 µsec period of data (512 bit window). This condition should be reliably detected in the presence of a 1.0E-03 Bit Error Rate (BER), implying that a framed all-ones pattern will not be mistaken as an AIS.

(per: ANSI T1.231)

T1 AIS (Blue Alarm) is declared when less than five spaces are detected in a 3 msec. window of data. This condition will be reliably detected in the presence of a 1.0E-03 Bit Error Rate (BER). When AIS is detected, the appropriate bit in the status register is set and a microprocessor interrupt is generated (unless masked).

12.3.3 NLOOP Status

With NLOOP detection enabled in "Loopback Enable Page Register, 10h" on page 70, the receiver looks for the NLOOP data patterns (00001 = enable, 001 = disable) in the input data stream. When the receiver detects an NLOOP enable data pattern repeated for a minimum of five seconds, the device enables RLOOP and the port status flag is set in "Alarm Status One Page Register, 12h" on page 70. The device responds to both framed and unframed NLOOP patterns. NLOOP is cleared by:

- Receiving the 001 pattern for five seconds.
- Activating RLOOP in "Loopback Enable Page Register, 10h" on page 70 or ALOOP in "Port Master Control Page Register, 01h" on page 65.
- Disabling NLOOP detection in "Loopback Enable Page Register, 10h".

A maskable processor interrupt for NLOOP is controlled by "Interrupt Enable Page Register, 11h" on page 70. Details about NLOOP interrupt status are reported in "Interrupt Status Two Page Register, 13h" on page 71.

12.3.4 BPV and EXZ Line Coding Violations

BPV and EXZ line coding violations are reported on signal traffic received at RTIP and RRING pins. Once a BPV or EXZ condition is detected, the port status flag is set in "Alarm Status One Page Register, 12h" on page 70. The LXT3104 has two registers that form a 16-bit counter for each

port to monitor BPVs and excess zeros. The counter mode is set by bits 7 through 5 in "Line Coding Control One Page Register, 1Ch". The counter can be enabled to count both BPVs and excess zeros or, for trouble-shooting purposes, to count either BPVs or Excess Zeros only. These counters, "BPV Counter High Byte Page Register, 1Eh" and "BPV Counter Low Byte Page Register, 1Fh", will increment when there is a valid code violation. The counter has a shadow register that is updated at one second intervals. The count value stored in the shadow register can be read by the host. The counter is reset every second.

12.3.4.1 T1 AMI/B8ZS BPVs

In T1 service, only one type of T1 BPV line coding violation is used:

A Bipolar Violation (BPV) is defined as any two consecutive pulses (marks) of the same polarity with AMI coded bit stream. When a B8ZS encoded signal is present and B8ZS decoding is active, no BPV's will be detected or reported.

The LXT3104 actively monitors the line signal for this type of coding violation and increments the BPV counter for performance monitoring purposes.

12.3.4.2 E1 AMI/HDB3 BPVs

Two basic types of E1 line coding violations are defined:

1. ITU G.703 - A BiPolar Violation (BPV) is defined as any two consecutive pulses (marks) of the same polarity with AMI coded bit stream.
2. ITU O.161- An HDB3 coding violation is defined as the occurrence of two consecutive BPVs of the same polarity that are not part of the HDB3 zero substitution coding.

The LXT3104 actively monitors the line signal for both types coding violations and increments the BPV counter for performance monitoring purposes.

12.3.4.3 Excess Zeroes (EXZ)

The definition of an EXZ depends upon the line coding format as explained in Table 11. The line signal is monitored for any violations of the maximum space rule as set in "Line Coding Control One Page Register, 1Ch" on page 71. If selected, EXZ occurrences increment the BPV counter for performance monitoring purposes.

Table 11. Excess Zero (EXZ) Definitions

Coding Method	EXZ Definition (ANSI)	EXZ Definition (FCC)
AMI	Any string greater than 15 consecutive 0s	Any string with greater than 80 consecutive zeroes
HDB3	Any string greater than 3 consecutive 0s	Any string with greater than 3 consecutive zeroes
B8ZS	Any string greater than 8 consecutive 0s	Any string with greater than 8 consecutive zeroes

13.0 Host Interface

The microprocessor interface is used to relay configuration, control, status, and data information between the LXT3104 and an external microprocessor or micro controller.

The microprocessor interface supports MPC860/M68360 (memory like bus), M68302 (standard Motorola bus), the i960/i486 processor bus, and the 8051 type micro controllers. 8-bit address and data buses are supported. Non-multiplexed address and data buses are supported along with a multiplexed address and data bus mode for an 8051-type micro controller. The user selects the processor type by tying the MPI_TYPE 1 & 2 pins appropriately. The processor interface can operate up to a bus cycle of 33Mhz. The MPC860 requires one cycle relaxed timing and the i960 requires one wait state. Handshaking and automatic wait state generation are supported. The latency of processor access is fixed so the use of the wait state signal is optional.

The LXT3104 provides extensive interrupt support. All interrupts are independently maskable. One interrupt output is provided. The interrupt signal is an open-drain output.

13.1 Supported Processors and Connections

The LXT3104 supports direct connection to the MPC860, M68360, M68302 (M68000 family), i486, and i960 processors. The user selects the type of processor by tying the TYPEx pins to the appropriate GND and Vcc connections. The connections between the processor pins and the MPI_TYPE programming are defined as below. Intel processor requires 1 wait state, MPC860 requires relaxed timing.

13.1.1 MPC860/M68360

The Motorola MPC860 and M68360 are supported in this mode. Note the LXT3104 host interface pins follow the MPC860 data endian fashion. For the MPC860, though there is no need for asynchronous wait states, relaxed write timing should be used. The LXT3104 requires write data to be valid prior to the falling edge of the write enable.

Table 12. MPC860/M68360 Mode 8-Bit Mode

Pin	MPC860	68360
TYPE1	0	0
TYPE2	0	0
DB0	D0	D7
...		
DB7	D7	D0
AD0	A24	A7
...		
AD7	A31	A0
CS	CS	CS
DS	OE	OE
RW	R/W#	R/W#
MPI_CLK	WE0	WE0
RDY	TA	DSACK1

13.1.2 M68302

The M68302 (or the M68000) is supported in this mode. This is commonly referred to as the Motorola bus.

Table 13. 68302 8-bit mode

Pin	68302
TYPE1	0
TYPE2	1
DB0	D0
...	
DB7	D7
AD0	A0
...	
AD7	A7
CS	CS
DS	DS
RW	R/W#
MPI_CLK	1
RDY	DTACK

13.1.3 i960/i486

The Intel i960/i486 family is supported in this mode. This is a synchronous bus interface with the timing being derived from the MPI_CLK input. Internally all operations will be performed on the next cycle after ADS is asserted. One wait state is required.

Table 14. i960/i486 Mode

Pin	
TYPE1	1
TYPE2	0
DB0	D0
DB1	D1
...	
DB7	D7
AD0	A0
...	
AD7	A7
CS	CS
DS	ADS
RW	W/R#
MPI_CLK	CLKO1
RDY	READY

13.1.4 8051 Mode

Table 15. 8051 Mode

Pin	
TYPE1	1
TYPE2	1
DB0	AD0
DB1	AD1
...	
DB7	AD7
AD0	0
...	0
AD7	0
CS	CS
DS	RD
RW	WR
MPI_CLK	ALE
RDY	0

13.2 Interrupts

There are four interrupt sources:

1. Status change in the Loss of Signal, LOS, bit of “Receiver Equalizer Status One Page Register, 07h” The LXT3104’s analog/digital LOS processor continuously monitors the receiver signal and updates the specific LOS status bit to indicate presence or absence of a LOS condition.
2. Status change in the AIS (Alarm Indication Signal) bit of “Alarm Status One Page Register, 12h”. The LXT3104’s receiver monitors the incoming data stream and updates the specific AIS status bit to indicate presence or absence of an AIS condition.
3. Status change in NLOOP (Network Loop Code) bit of “Alarm Status One Page Register, 12h”.
4. Elastic Store overflow or underflow (DJA overflow or underflow) bits of “Alarm Status One Page Register, 12h”. The LXT3104 jitter attenuator updates these based on DJA response to jitter on incoming signal.

13.2.1 Interrupt Enable

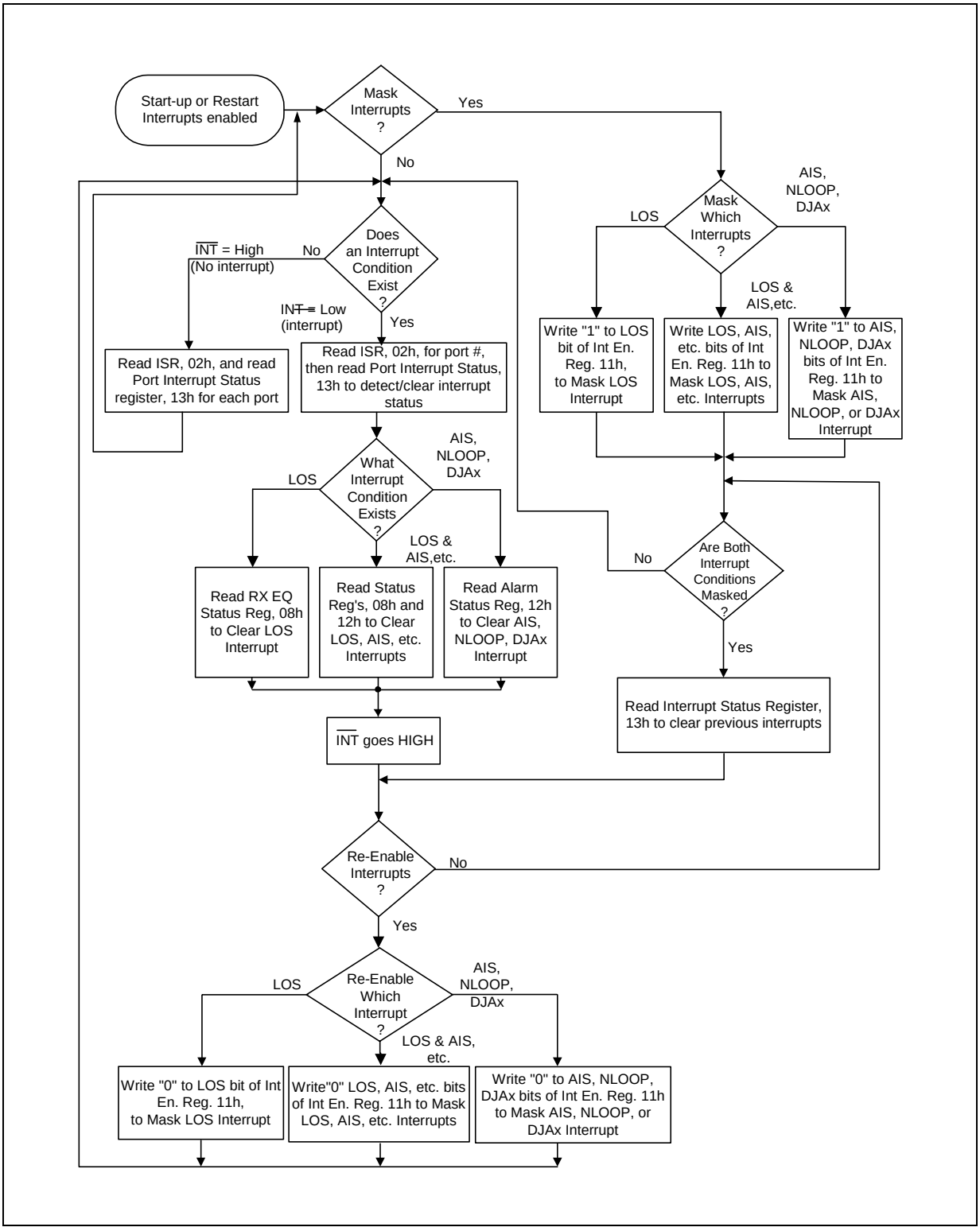
The LXT3104 provides a latched interrupt output ($\overline{INT}$). An interrupt occurs any time there is a transition on any enabled bit in the status register. Writing a logic “1” into the mask register will enable the respective bit in the respective Interrupt status register to generate an interrupt. The power-on default value is all zeros. The setting of the interrupt enable bit does not affect the operation of the status registers.

When there is a transition on any enabled bit in a status register, the associated bit of the interrupt status register is set and an interrupt is generated (if one is not already pending). When an interrupt occurs, the $\overline{INT}$ pin is asserted Low. The output stage of the $\overline{INT}$ pin consists only of a pull-down device; an external pull-up resistor of approximately 10k Ω is required to support wired-OR operation.

13.2.2 Interrupt Clearing

There are three status registers: LOS, AIS, and NLOOP. Reading either status register will clear the corresponding interrupts with the rising edge of the read or data strobe. When there are no pending interrupts left $\overline{INT}$ pin will go back to high. Refer to Figure 23, “Interrupt Processing FlowChart” on page 61 for details.

Figure 23. Interrupt Processing FlowChart



14.0 Register Definitions

Since the LXT3104 has both global registers and Page Port Registers (PPRs), the first subsection covers the global registers and the second subsection covers the PPRs. The global registers control parameters affecting operation for the entire device. One set of PPR registers controls parameters affecting operation for a single port. Of the five sets of PPR registers, there is one for each of the four ports and there is an additional set that controls all four ports at the same time.

Because global registers are programmed differently than PPRs, this section describes the differences:

- Access a global register by reading or writing directly to the global register address. This is a single operation to read or write a global register.
- Access PPRs by writing to a global register, Port Page Select (PPS) at address 00h, with the selected port number. Immediately following this action, access the PPR for the selected port by reading or writing to the chosen PPR address. This is a double operation, one write access to the PPS with the port number followed by a single read or write to a PPR.

14.1 Global Registers

This subsection is organized with a summary of the global registers in Table 16 followed by a descriptive listing of each global register starting at Table 17 on Page 62 and ending at Table 41 on Page 72. Table 16 includes the global register names and addresses for the LXT3104.

Table 16. Global Register Addresses

Name	Symbol	Parallel Port A7-A0	HEX Address	Mode
Port Page Select Register	CPS	00000000	00	R/W
ID Register	ID	00000001	01	R
Interrupt Port Register	ICR	00000010	02	R

Table 17. Port Page Select Register, CPS, 00h

Bit	Name	Function
7-0	PS4-PS0	Writing to this register selects the index to the page for individual port control registers. 7 Soft-reset, resets all ports, and the entire device. 6:4 not used [3 2 1 0] Index/Page 0000 Selects Global Register Page 0001 Selects Page 1 - control registers for Port 0 0100 Selects Page 2- control registers for Port 1 0101 Selects Page 3- control registers for Port 2 1000 Selects Page 4- control registers for Port 3 1001 Selects write to all page control registers at one time. *Note: When CPS Register value equals 9h, Read is disabled*

Table 18. ID Register, ID, 01h

Bit	Name	Function
7-0	ID7-ID0	This register contains a unique revision code and is mask programmed.

Table 19. Interrupt Status Register, ISR, 02h

Bit	Name	Function
7-0	ICR7-ICR0	A “1” indicates that an interrupt occurred in the respective port.

Table 20. Register Bit Names

Register			Bit							
Name	Sym	RW	7	6	5	4	3	2	1	0
Page select register	PSR	R/W	Soft_RST				PSR3	PSR2	PSR1	PSR0
ID Register	ID	R	ID7			ID4	ID3			ID0
Interrupt Port Register	ICR	R	4			3	2			CH1

14.2 Port Page Register Bank (PPRB)

Each of the four LIU ports in the LXT3104 has independent register control available through its Port Page Register Bank. Writing to each bank of registers is a two-step process:

- Select port by writing port number to global register Port Page Select (PPS), address 00h. The CPS register at address 00h is a global register across all the pages. Therefore, writing to address 00h at any time will switch the register to read/write access to the last specified value written to address 00h.
- Immediately after, access LIU registers for a port by reading or writing chosen CPRB address.

There is an additional mode where all four ports can be set up to the identical settings by writing first to address 00h with a 09h.

Table 17 on Page 62 gives an overview of the CPRB structure for each port's LIU. Each port in the LXT3104 has an individual CPRB. The registers in the port bank structure are descriptively listed in the range of Table 22 on Page 65 through Table 41 on Page 72.

Table 21. Port Page Register Bank Addresses

Name	Symbol	Parallel Port A7-A0	Address	Mode
Port Master Control	MASTER	0000 0001	01h	R/W
Port Enable, Not Used	RENEN	0000 0010	02h	R/W
Transmit Control	TXCON	0000 0011	03h	R/W
Receiver Control	RXCON	0000 0100	04h	R/W
Termination Control	TERM	0000 0101	05h	R/W
RX Equalizer Status 0	RXSTATUS0	0000 0110	06h	R
RX Equalizer Status 1	RXSTATUS1	0000 0111	07h	R
RX Equalizer Status 2	RXSTATUS2	0000 1000	08h	R
LOS Window	LOSWINLEN	0000 1011	0Bh	R/W
LOS Set Threshold	LOSTHRES1	0000 1100	0Ch	R/W
LOS Reset Threshold	LOSTHRES2	0000 1101	0Dh	R/W
Loopback Enable Register	LER	0001 0000	10h	R/W
Interrupt Enable Register	IER	0001 0001	11h	R/W
Alarm Status Register 1	SR1	0001 0010	12h	R
Interrupt Status Register 2	SR2	0001 0011	13h	R
Control Register 1	CR1	0001 1100	1Ch	R/W
Control Register 2	CR2	0001 1101	1Dh	R/W
BPV counter High Byte	BPVCTRHB	0001 1110	1Eh	R
BPV counter Low Byte	BPVCTRLB	0001 1111	1F	R
Transmit Pulse Shape Coefficients	TXCOEF		40h-6Fh	R/W

Table 22. Port Master Control Page Register, 01h

Address	Description	Name	Status	Bit	Description
01h	Port Master Control	MASTER	R/W	7	Reserved
				6	TXPD, “1” powers down transmitter section
				5	RXPD, “1” powers down receiver section
				4	USR_LOS, “1” enables programmable control of digital LOS window, set, and clear conditions
				3	I431, “1” enables programmable control of analog LOS levels for set and clear
				2	Reserved
				1	ALOOP, “1” enable analog loopback diagnostic mode
				0	T1E1, “1” enables T1, 1.544 MHz operation, while “0” enables E1, 2.048 MHz operation
Note: Upon reset, restored default value is 0h.					

Table 23. Port Receive Enable Page Register, 02h

Address	Description	Name	Status	Function
02h	Port Enable	CHANEN	R/W	If bit 0 is set high, port receiver starts
Note: Upon reset, restored default value is 0h.				

Table 24. Transmit Control Page Register, 03h

Address	Description	Name	Status	Bit	Function
03h	Transmit Control	TXCON	R/W	7	Transmit all ones enable (TAOS)
				6	Transmit output high impedance (OES)
				5	Transmit Clock Detect Enable
				[4..1]	***Decode bits 4 to 0 for pre-programmed pulse shapes.***
				0h	• T1 SH 0-133 ft.
				1h	• T1 SH 134 -266 ft.
				2h	• T1 SH 267 - 399 ft.
				3h	• T1 SH 400 -533 ft.
				4h	• T1 SH 534 - 655 ft.
				5h	• T1 0dB LH
				6h	• T1 LH -7.5 dB
				7h	• T1 LH -15 dB
				8h	• T1 LH -22.5 dB
				9h	• E1 SH 75 Ω
				0Ah	• E1 SH 120 Ω
				0Bh	• E1 LH 75 Ω
				0Ch	• E1 LH 120 Ω
				0Dh	• J1 (no encoded pulse)
				0Eh	• Not used
				0Fh	• Not used
				0	• ATWG_EN active high enables ATWG operation
Note: Upon reset, restored default value is 0h.					

Table 25. Receive Control Page Register, 04h

Address	Description	Name	Status	Bit	Function
04h	Receiver Control	RXSH	R/W	7	active high limits receiver to SH operation
		MON_MOD		6	active high enables monitor mode
				5	Not used
		RXCON		***[4..0]***	***Decode bits 4 to 0 selecting receive sensitivity in dB.***
				0h	• E1-43; T1-36
				1h	• E1-40; T1-34
				2h	• E1-38; T1-32
				3h	• E1-36; T1-30
				4h	• E1-34; T1-28
				5h	• E1-32; T1-26
				6h	• E1-30; T1-24
				7h	• E1-28; T1-22
				8h	• E1-26; T1-20
				9h	• E1-24; T1-18
				0Ah	• E1-22; T1-16
				0Bh	• E1-20; T1-14
				0Ch	• E1-18; T1-12
				0Dh	• E1-16; T1-10
				0Eh	• E1-14; T1-8
				0Fh	• E1-22; T1-6
				10h	• E1-20; T1-4
				11h	• E1-18; T1-2
				12h	• E1-16; T1-0
				13h	• E1-14; T1-36
				1Bh - 1Fh	• E1-43; T1-36

Note: Upon reset, restored default value is 0h.

Table 26. Termination Control Page Register, 05h

Address	Description	Name	Status	Bit	Function
05h	Termination Control TX/RX	TERM	R/W	***[7..6]***	***Decode bits 7 to 6 selecting transmit termination control***
				0	• 100 Ω
				1	• 110 Ω
				2	• 120 Ω
				3	• 120 Ω
				[5..2]	***Bit 5 through 2 are not assigned***
				[1..0]	***Decode bits 1 to 0 selecting receive termination control***
				0	• 100 Ω
				1	• 110 Ω
				2	• 120 Ω
				3	• 100 Ω
Note: Upon reset, restored default value is 0h.					

Table 27. Receiver Equalizer Status Zero Page Register, 06h

Address	Description	Name	Status	Bit	Function
06h	RX Equalizer Status0	RXSTATUS0	R	***[7..0]***	***Reserved***
Note: Upon reset, restored default value is 0h.					

Table 28. Receiver Equalizer Status One Page Register, 07h

Address	Description	Name	Status	Bit	Function
07h	RX Equalizer Status1	RXSTATUS1	R	***[7..4]***	***Reserved***
				[3..0]	***Decode bits 3 to 0 selecting AGC state settings*** Attenuation reading determines cable length by this formula: TBD
Note: Upon reset, restored default value is 0h.					

Table 29. Receiver Equalizer Status Two Page Register, 08h

Address	Description	Name	Status	Bit	Function
08h	RX Equalizer Status 2	RXSTATUS2	R	4	LOS
				3	Not used
				2	Reserved
				1	Reserved
				0	Reserved
Note: Upon reset, restored default value is 0h.					

Table 30. LOS Window Page Register, 0Bh

Address	Description	Name	Status	Function
0Bh	LOS Window	LOSWINLEN	R/W	LOS detector evaluation window. When LOS USER Mode is selected, this register must be programmed to the length of the LOS evaluation window. This is the number of consecutive bits for which the LOS condition must be true before LOS is asserted, (e.g. If set to 256, then 256 consecutive 0s will assert LOS).
Note: Upon reset, restored default value is 0h.				

Table 31. LOS Set Threshold One Page Register, 0Ch

Address	Description	Name	Status	Function
0Ch	LOS Set Threshold	LOSTHRES1	R/W	This register controls two functions: • In LOS AMP detection mode, it is the treshold to set LOS • In LOS DEN detection mode, it is RSPACELIM
Note: Upon reset, restored default value is 0h.				

Table 32. LOS Reset Threshold Two Page Register, 0Dh

Address	Description	Name	Status	Function
0Dh	LOS Reset Threshold	LOSTHRES2	R/W	This register controls two functions: • In P detection mode, it is threshold to reset LOS • In LOS DEN detection mode, it is RMARKCLR
Note: Upon reset, restored default value is 0h.				

Table 33. Loopback Enable Page Register, 10h

Address	Description	Name	Status	Bit	Function
10h	Loopback Enable Register	LER	R/W	***[7..5]***	***Bits 7 to 5 not used***
				4	DLOOP, Digital loopback, if set to ‘1’
				3	Transmit network Loop Down code
				2	Transmit network Loop Up code
				1	NLOOP, Network loopback enabled if set to ‘1’, (Receive)
				0	RLOOP, Remote loopback, if set to ‘1’
Note: Upon reset, restored default value is 0h.					

Table 34. Interrupt Enable Page Register, 11h

Address	Description	Name	Status	Bit	Function
11h	Interrupt Enable Register	IER	R/W	***[7..5]***	***Bits 7 to 5 not used***
				4	DJA Underflow Interrupt Enable, if set to ‘1’
				3	DJA Overflow Interrupt Enable, if set to ‘1’
				2	NLOOP Interrupt Enable, if set to ‘1’
				1	AIS Interrupt Enable, if set to ‘1’
				0	LOS Interrupt Enable, if set to ‘1’
Note: Upon reset, restored default value is 0h.					

Table 35. Alarm Status One Page Register, 12h

Address	Description	Name	Status	Bit	Function
12h	Status Register 1	SR1	R	***[7..5]***	***Bits 7 to 5 not used.***
				4	BPV status
				3	DJA overflow status
				2	DJA underflow status
				1	NLOOP status
				0	AIS status
Note: Upon reset, restored default value is 0h.					

Table 36. Interrupt Status Two Page Register, 13h

Address	Description	Name	Status	Bit	Function
13h	Interrupt Status Register 2	SR2	R	***[7..5]***	***Bits 7 to 5 not used.***
				4	LOS interrupt status
				3	DJA overflow interrupt status
				2	DJA underflow interrupt status
				1	NLOOP interrupt status
				0	AIS interrupt status
Note: Upon reset, restored default value is 0h.					

Table 37. Line Coding Control One Page Register, 1Ch

Address	Description	Name	Status	Bit	Function
1Ch	Control Register 1	CR1	R/W	7	ez mode - 0: ANSI, 1: FCC
				[6..5]	***Decode bits 6 to 5 selecting BPV Counter mode***
				0h	• Enable counting of both BPVs and Excess Zero
				1h	• Enable counting of BPVs only
				2h	• Enable counting of Excess Zeroes only
				3h	• invalid code
				Bit	***Functions***
				4	E1AIS_Sel, 0 = ITU G.775, 1 = ETSI 300233
				3	Transmit B8ZS/HDB3 enable, 1 = HDB3/B8ZS
				2	Receive B8ZS/HDB3 enable, 1 = HDB3/B8ZS
				1	Transmit Unipolar/Bipolar select, 0 = Bipolar
				0	Receive Unipolar/Bipolar select, 0 = Bipolar
Note: Upon reset, restored default value is 0h.					

Table 38. JA Control Two Page Register, 1Dh

Address	Description	Name	Status	Bit	Function
1Dh	Control Register 2	JARES	R/W	7	1 = reset DJA's elastic store
		JARST		6	1 = completely reset DJA
		JAJC		5	0=jamming enabled, 1=jamming disabled
		ES64		4	DJA depth select, 0 = 32 bits, 1 = 64 bits
		JABW1		3	JABW1
		JABW0		2	JABW0
		JA transmit or receive path		1	0 = JA in receive path; 1 = JA in transmit path
		JA enable		0	1 = JA enable
Note: Upon reset, restored default value is 0h.					

Table 39. BPV Counter High Byte Page Register, 1Eh

Address	Description	Name	Status	Function	
1Eh	BPV counter high byte	BPVCTRHB	R		High byte of the 16-bit BPV counter shadow register
Note: Upon reset, restored default value is 0h.					

Table 40. BPV Counter Low Byte Page Register, 1Fh

Address	Description	Name	Status	Function	
1Fh	BPV counter low byte	BPVCTRLB	R		Low byte of the 16-bit BPV counter shadow register
Note: Upon reset, restored default value is 0h.					

Table 41. Transmit Coefficient Page Register Range, 40h-6Fh

Address	Description	Name	Status	Function	
40-6F	Transmit Coefficients for pulse shaping	TXCOEF	R/W		16/48 8-bit TX filter coefficients
Note: Upon reset, restored default value is 0h.					

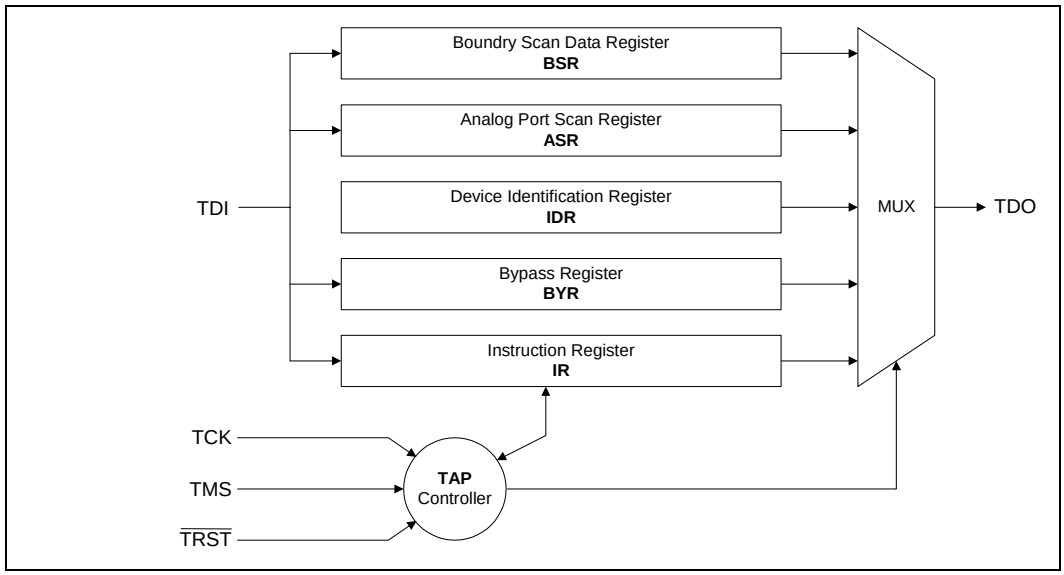
15.0 JTAG Boundary Scan

The LXT3104 supports IEEE 1149.1 compliant JTAG boundary scan. Boundary scan allows easy access to the interface pins for board testing purposes.

15.1 Architecture

Figure 24 represents the LXT3104 basic JTAG architecture:

Figure 24. LXT3104 JTAG Architecture



The LXT3104 JTAG architecture includes a TAP Test Access Port Controller, data registers and an instruction register. The following paragraphs describe these blocks in detail.

15.2 TAP Controller

The TAP controller is a 16-state synchronous state machine controlled by the TMS input and clocked by TCK (see Figure 25). The TAP controls whether the LXT3104 is in reset mode, receiving an instruction, receiving data, transmitting data or in an idle state. Table 42 describes in detail each of the states represented in Figure 25.

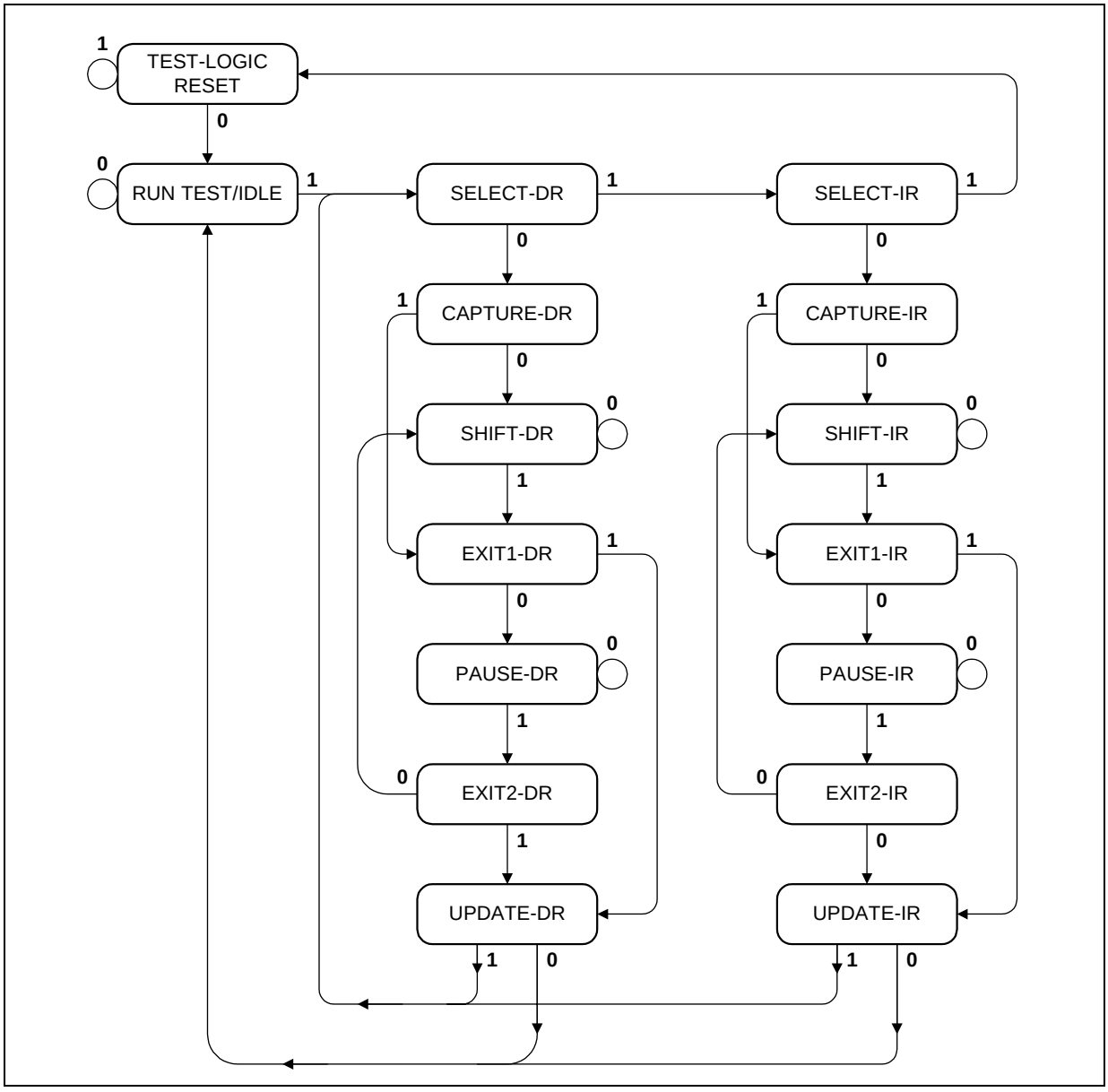
Table 42. TAP State Description

State	Description
Test Logic Reset	In this state, the test logic is disabled. The device is set to normal operation mode. While in this state, the instruction register is set to the ICODE instruction.
Run -Test/Idle	The TAP controller stays in this state as long as TMS is low. Used to perform tests.
Capture - DR	The Boundary Scan Data Register (BSR) is loaded with input pin data.
Shift - DR	Shifts the selected test data registers by one stage toward its serial output.
Update - DR	Data is latched into the parallel output of the BSR when selected.
Capture - IR	Used to load the instruction register with a fixed instruction.
Shift - IR	Shifts the instruction register by one stage.

Table 42. TAP State Description

State	Description
Update - IR	Loads a new instruction into the instruction register.
Pause - IR Pause - DR	Momentarily pauses shifting of data through the data/instruction registers.
Exit1 - IR Exit1 - DR Exit2 - IR Exit2 - DR	Temporary states that can be used to terminate the scanning process.

Figure 25. JTAG State Diagram



15.3 JTAG Register Description

The following paragraphs describe each of the registers represented in Figure 24.

15.3.1 Boundary Scan Register (BSR)

The BSR is a shift register that provides access to all the digital I/O pins. The BSR is used to apply and read test patterns to/from the board. Each pin is associated with a scan cell in the BSR register. Bidirectional pins or tristatable pins require more than one position in the register. Data into the BSR is shifted in LSB first.

15.3.2 Device Identification Register (IDR)

The IDR register provides access to the manufacturer number, part number and the LXT3104 revision. The register is arranged per IEEE 1149.1 and is represented in Table 43. Data into the IDR is shifted in LSB first.

Table 43. Device Identification Register (IDR)

Bit #	Comments
31 - 28	Revision Number
27 - 12	Part Number
11 - 1	Manufacturer Number
0	Set to “1”

15.3.3 Bypass Register (BYR)

The Bypass Register is a 1-bit register that allows direct connection between the TDI input and the TDO output.

15.3.4 Instruction Register (IR)

The IR is a 3-bit shift register that loads the instruction to be performed. The instructions are shifted LSB first. Table 44 shows the valid instruction codes and the corresponding instruction description.

Table 44. Instruction Register (IR)

Instruction	Code #	Comments
EXTEST	000	Connects the BSR to TDI and TDO. Input pins values are loaded into the BSR. Output pins values are loaded from the BSR.
INTEST_ANALOG	010	Connects the ASR to TDI and TDO. Allows voltage forcing/sensing through AT1 and AT2.
SAMPLE/PRELOAD	100	Connects the BSR to TDI and TDO. The normal path between the LXT3104 logic and the I/O pins is maintained. The BSR is loaded with the signals in the I/O pins.
IDCODE	110	Connects the IDR to the TDO pin.
BYPASS	111	Serial data from the TDI input is passed to the TDO output through the 1 bit Bypass Register.

16.0 Test Specifications

Table 45. Absolute Maximum Ratings

Parameter	Sym	Min	Max	Unit
DC supply (reference to GND)[1]	V_{CC}, T_{VCC}	-0.5	3.6	V
Input voltage, RTIP/RRING	VRX	-6.0	TVCC + 0.3 V	V
Input voltage, any digital pin	V_{IN}	GND-0.5	5.5	V
Input current, any pin	I_{IN}	-10	10	mA
Storage temperature	T_{STG}	-65	150	° C
Thermal Resistance, junction to ambient, QFP		TBD	–	C/W
Thermal Resistance, junction to ambient, PBGA		TBD	–	C/W
ESD voltage, any pin[2,3]	V_{IN}	2000	–	V

Caution: Operation at these limits may permanently damage the device. Normal operation at these extremes not guaranteed.
1. TVCC and VCC must not differ by more than 0.3 V during operation. TGND and GND must not differ by more than 0.3 V during operation.
2. Human body model.
3. This is a design target and not a product specification.

Table 46. Recommended Operating Conditions

Parameter			Sym	Min	Typ[1]	Max	Unit	Test Conditions
DC supply [2]			V_{CC}, T_{VCC}	3.135	3.3	3.465	V	3.3V +/- 5%
Ambient operating temperature			T_A	-40	–	85	° C	
Total power dissipation[3, 4]	T1	SH	P_D	–	TBD	–	mW	100% mark density
			P_D	–	TBD	–	mW	50% mark density
		LH	P_D	–	TBD	–	mW	100% mark density
			P_D	–	TBD	–	mW	50% mark density
	E1	SH/ LH	P_D	–	TBD	–	mW	100% mark density
			P_D	–	TBD	–	mW	50% mark density
Recommended line load to TTIP/ TRING			–	TBD	–	TBD	Ω	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. TVCC and VCC must not differ by more than 0.3 V.
3. Power dissipation specifications are TBD.
4. Power dissipation values include shared circuit.

Table 47. Electrical Characteristics (Over Recommended Operating Conditions)

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
High level input voltage[1]	V_{IH}	2	–	5	V	In idle and power down
Low level input voltage[1]	V_{IL}	–	–	0.8	V	
Output High voltage[2]	V_{OH}	2.4		VCCIO	V	
Output Low voltage[2]	V_{OL}	–	–	0.4	V	
Quiescent current	IDDQ	0	–	±10	µA	
Input leakage current	I_{LL}	0	–	±50	µA	
Three-state leakage current (all outputs)	I_{3L}	0	–	±10	µA	
TTIP/TRING leakage current	I_{TR}	–	–	±10	µA	In idle and power down
Output driver rise time	T_R	–	–	10	ns	1 pF load
1. LXT3104 interface via CMOS logic levels. 2. Output drivers will output TTL logic levels.						

Table 48. E1 Transmitter Analog Characteristics

Parameter		Sym	Min.	Typ.	Max.	Unit	Test Condition
Internal transmitter impedance tolerance		–	–	TBD	–	%	Matching line load
Pulse amplitude variation per LSB	CEPT (ITU)	–	TBD	–	TBD	mV	**TBD**
Output pulse amplitude	75 Ω	–	2.14	2.37	2.60	V	Tested at the line side
	120 Ω	–	2.7	3.0	3.3	V	Tested at the line side
Peak voltage of a space	75 Ω	–	-0.237	–	0.237	V	
	120 Ω	–	-0.3	–	0.3	V	
Transmit amplitude variation with supply		–	-1	–	+1	%	
Difference between pulse sequences		–		–	200	mV	For 17 consecutive pulses
Pulse width ratio of the positive and negative pulses		–	0.95	–	1.05	–	***Note:*** At the nominal half amplitude
Transmit return loss 75 Ω coaxial cable[1]	51 kHz to 102 kHz	–	TBD	TBD	–	dB	
	102 kHz to 2.048 MHz	–	TBD	TBD	–	dB	
	2.048 MHz to 3.072 MHz	–	TBD	TBD	–	dB	
Transmit return loss 120 Ω twisted pair cable[1]	51 kHz to 102 kHz	–	6	TBD	–	dB	
	102 kHz to 2.048 MHz	–	8	TBD	–	dB	
	2.048 MHz to 3.072 MHz	–	8	TBD	–	dB	
Transmit intrinsic jitter; 20 Hz to 100 kHz		–	.05	TBD	–	UI	Tx path TCLK is jitter free
Transmit path delay	Bipolar mode	–	TBD	TBD	–	UI	JA Disabled
	Unipolar mode	–	TBD	TBD	–	UI	
1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing. 2. Guaranteed by design and other correlation methods.							

Table 49. E1 Receiver Analog Characteristics

Parameter		Sym	Min.	Typ.[1]	Max.	Unit	Test Condition
Permissible cable attenuation		–	–	–	43	dB	@1024 kHz
Receiver sensitivity @ 1024 kHz (E1 line loss)	(E1 SH/12 dB)	–	0	–	13.6	dB	Receiver sensitivity @ 1024 kHz (E1 line loss)
	(E1 LH/43 dB)	–	0	–	43	dB	
Receiver dynamic range		DR	–	–	–	Vp	
Signal to noise interference margin		S/I	–	–	–	dB	Per G.703, O.151 @ 6 dB cable Attenuation
Loss of signal threshold		–	–	TBD	–	mV	
Consecutive zeros before loss of signal		–	–	32	–	–	G.775 recommendation
		–	–	2048	–	–	ETSI 300 233 specification
LOS reset		–	12.5%	–	–	–	1s density
LOS delay time		–	–	30	–	µs	Data recovery mode
LOS reset		–	10	–	255	marks	Data recovery mode
Low limit input jitter tolerance [2]	1 Hz	–	37	–	–	U.I	G.823 recommendation Cable Attenuation is 6 dB
	20 Hz to 2.4 kHz	–	1.5	–	–	U.I	
	100 kHz	–	0.2	–	–	U.I	
Differential receiver input impedance		–	–	TBD	TBD	k Ω	@1.024 MHz
Common mode input impedance to ground		–	–	TBD		k Ω	
Input termination resistor tolerance		–	–	–	±1	%	
Input return loss[2]	51 kHz - 102 kHz	–	TBD	–	12	dB	
	102 - 2048 kHz	–	TBD	–	18	dB	
	2048 kHz - 3072 kHz	–	TBD	–	14	dB	
Receive intrinsic jitter, RCLK output		–	–	TBD	0.05	UI	Wide band jitter
Receive path delay	Bipolar mode	–	–	TBD	–	UI	JA Disabled
	Unipolar mode	–	–	TBD	–	UI	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Guaranteed by design and other correlation methods.

Table 50. T1 Transmitter Analog Characteristics

Parameter		Sym	Min.	Typ.[1]	Max.	Unit	Test Condition
Internal transmitter impedance tolerance		–	–	TBD	–	%	Matching line load
Pulse amplitude variation per LSB	DSX-1, DS1	–	TBD	–	TBD	mV	**TBD**
Output pulse amplitude		–	2.4	3.0	3.6	V	Measured at the DSX
Peak voltage of a space		–	-0.15	–	+0.15	V	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Guaranteed by design and other correlation methods.
3. Power measured in a 3 KHz bandwidth at the point the signal arrives at the distribution frame for an all 1's pattern.

Table 50. T1 Transmitter Analog Characteristics (Continued)

Parameter		Sym	Min.	Typ.[1]	Max.	Unit	Test Condition
Transmit amplitude variation with power supply		–	-1	–	+1	%	
Imbalance between positive and negative pulse amplitude			0.95	–	1.05	–	T1.102, isolated pulse
Difference between pulse sequences		–	–	–	200	mV	For 17 consecutive pulses, GR-499-CORE
Pulse width variation at half amplitude[1]		–	–	–	20	ns	
Line side short circuit current (T1)		–	–	–	150	mA RMS	
Jitter added by Transmitter[2]	10Hz - 8 KHz	–	–	–	TBD	UI_{pk-pk}	AT&T Pub 62411 TCLK is jitter free
	8KHz - 40 KHz	–	–	–	TBD	UI_{pk-pk}	
	10Hz - 40 KHz	–	–	–	TBD	UI_{pk-pk}	
	Wide Band	–	–	–	0.05	UI_{pk-pk}	
Output power levels[3]	@ 772 KHz	–	12.6	–	17.9	dBm	T1.102 - 1993 Referenced to power at 772 KHz
	1544 KHz	–	-29	–	17.9	dBm	
Transmit Return Loss [2]	39 KHz - 77KHz	–	6	TBD	–	dB	
	77- 1544 KHz	–	8	TBD	–	dB	
	1544 KHz - 2316KHz	–	8	TBD	–	dB	
Transmit path delay	Bipolar mode	–		TBD	–	UI	JA Disabled
	Unipolar mode	–		TBD	–	UI	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Guaranteed by design and other correlation methods.
3. Power measured in a 3 KHz bandwidth at the point the signal arrives at the distribution frame for an all 1's pattern.

Table 51. T1 Receiver Analog Characteristics

Parameter		Sym	Min.	Typ.[1]	Max.	Unit	Test Condition
Permissible cable attenuation		–	–	–	36	dB	@ 772 KHz
Receiver sensitivity @ 772 kHz (T1 line loss)	(T1 SH/12 dB)	–	0	–	13.6	dB	Receiver sensitivity @ 772 kHz (T1 line loss)
	(T1 LH/36 dB)	–	0	–	36	dB	
Receiver dynamic range		DR	TBD	–	–	Vp	
Signal to noise interference margin		S/I	-16.5	–	–	dB	@ 655 ft of 22 ABAM cable
Loss of signal threshold		–	–	TBD	–	mV	
LOS hysteresis		–	–	TBD	–	mV	
Consecutive zeros before loss of signal		–	100	175	250	–	T1.231 - 1993
Low limit input jitter tolerance [2]	1 Hz	–	138	–	–	UI	AT&T Pub. 62411
	10 Hz to 300 Hz	–	28	–	–	UI	
	10 KHz to 100 KHz	–	0.4	–	–	UI	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Guaranteed by design and other correlation methods.

Table 51. T1 Receiver Analog Characteristics (Continued)

Parameter		Sym	Min.	Typ.[1]	Max.	Unit	Test Condition
Differential receiver input impedance		–	–	100	–	Ω	@772 kHz
Common mode input impedance to ground		–	–	120	–	Ω	
Input termination resistor tolerance		–	–	–	±1	%	
Input return loss[1]	39 KHz - 77KHz	–	TBD	–	12	dB	
	77- 1544 KHz	–	TBD	–	18	dB	
	1544 KHz - 2316KHz	–	TBD	–	14	dB	
Receive intrinsic jitter, RCLK output[2]		–	–	TBD	0.05	UI	Wide band jitter
Receive path delay	Bipolar mode	–	–	TBD	–	UI	JA Disabled
	Unipolar mode	–	–	TBD	–	UI	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Guaranteed by design and other correlation methods.

Table 52. Master and Transmit Clock Timing Characteristics

Parameter	Sym	Min	Typ[1]	Max	Unit	Notes
Master clock frequency	MCLK	–	8.192	–	MHz	Must be supplied
Master clock tolerance	MCLKt	–	±50	–	ppm	
Master clock duty cycle	MCLKd	40	–	60	%	
T1 Transmit clock frequency	TCLK	–	1.544	–	MHz	
E1 Transmit clock frequency	TCLK	–	2.048	–	MHz	
Transmit clock tolerance	TCLKt	–	–	±50	ppm	
Transmit clock duty cycle	TCLKd	10	–	100	%	
TPOS/TNEG to TCLK setup time	Tsut	50	–	–	ns	
TCLK to TPOS/TNEG hold time	Tht	50	–	–	ns	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 26. Transmit Clock Timing Diagram

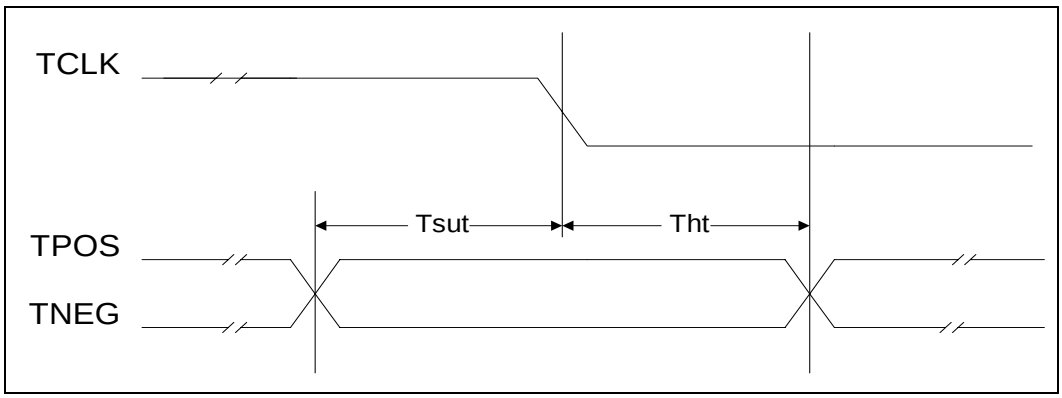


Table 53. Jitter Attenuator Characteristics

Parameter			Min.	Typ.[1]	Max.	Unit	Test Condition
E1 jitter attenuator 3dB corner frequency	JACF=0	32bit FIFO	–	2.5	–	Hz	Sinusoidal jitter modulation
		64bit FIFO	–	3.5	–	Hz	
	JACF=1	32bit FIFO	–	2.5	–	Hz	
		64bit FIFO	–	3.5	–	Hz	
T1 jitter attenuator 3dB corner frequency	JACF=0	32bit FIFO	–	3	–	Hz	
		64bit FIFO	–	3	–	Hz	
	JACF=1	32bit FIFO	–	6	–	Hz	
		64bit FIFO	–	6	–	Hz	
Jitter attenuator 3dB corner frequency[2]		E1	–	3.5	–	Hz	
		T1	–	6	–	Hz	
Data latency delay		32bit FIFO	–	16	–	UI	Delay through the Jitter attenuator only. Add TBD UI for total receive path delay and TBD UI for total transmit path delay.
		64bit FIFO	–	32	–	UI	
Input jitter tolerance before FIFO overflow or underflow		32bit FIFO	–	24	–	UI	
		64bit FIFO	–	56	–	UI	
E1 jitter attenuation	@ 3 Hz	–	-0.5	TBD	–	dB	ITU-T G.736
	@ 40 Hz	–	-0.5	TBD	–	dB	
	@ 400 Hz	–	+19.5	TBD	–	dB	
	@ 100 KHz	–	+19.5	TBD	–	dB	
T1 jitter attenuation	@ 1 Hz	–	0	TBD	–	dB	AT&T Pub. 62411
	@ 20 Hz	–	0	TBD	–	dB	
	@ 1 KHz	–	33.3	TBD	–	dB	
	@ 1.4 KHz	–	40	TBD	–	dB	
	@ 70 KHz	–	40	TBD	–	dB	
Output jitter in remote loopback[2]		–	TBD	0.11	–	UI	ETSI CTR12/13 Output jitter

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Guaranteed by design and other correlation methods.

Table 54. Receive Timing Characteristics for T1 Operation

Parameter	Sym	Min	Typ[1]	Max	Unit
Receive clock duty cycle [2, 3]	RLCKd	40	50	60	%
T1 Receive clock pulse width [2, 3]	t_{PW}	–	648	–	ns
T1 Receive clock pulse width High	t_{PWH}	–	324	–	ns
T1 Receive clock pulse width Low[1,3]	t_{PWL}	260	324	388	ns
RPOS/RNEG to RCLK rising time	t_{DRPN}	0	–	274	ns

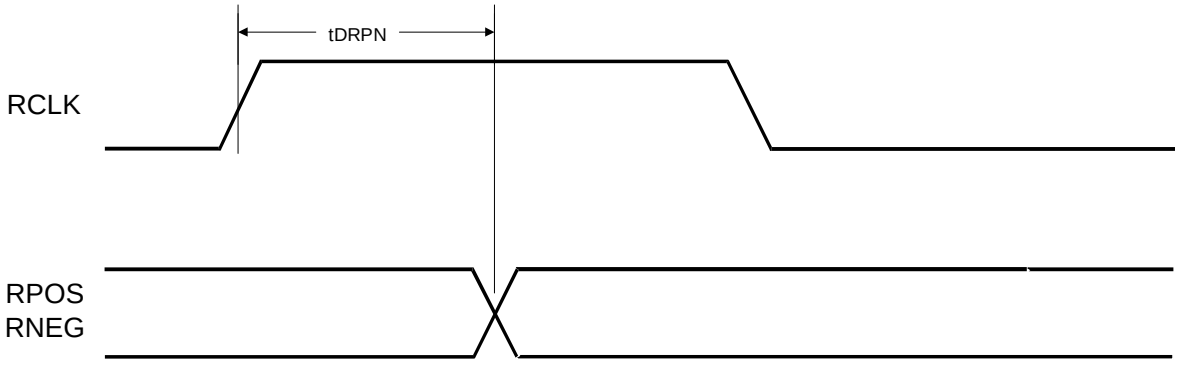
1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary according to extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions.
3. Worst case conditions guaranteed by design only.

Table 55. Receive Timing Characteristics for E1 Operation

Parameter	Sym	Min	Typ[1]	Max	Unit
E1 Receive clock duty cycle [2, 3]	RLCKd	40	50	60	%
E1 Receive clock pulse width [2, 3]	t_{PW}	–	488	–	ns
E1 Receive clock pulse width High	t_{PWH}	–	244	–	ns
E1 Receive clock pulse width Low[1,3]	t_{PWL}	195	244	293	ns
RPOS/RNEG to RCLK rising time	t_{DRPN}	0	–	194	ns

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle widths will vary according to extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst case jitter conditions.
3. Worst case conditions guaranteed by design only.

Figure 27. Receive Clock Timing Diagram



Note: RCLK active-edge selected by CLKE configuration bit.

Figure 28. LXT3104 Output Jitter for CTR12/13 Applications

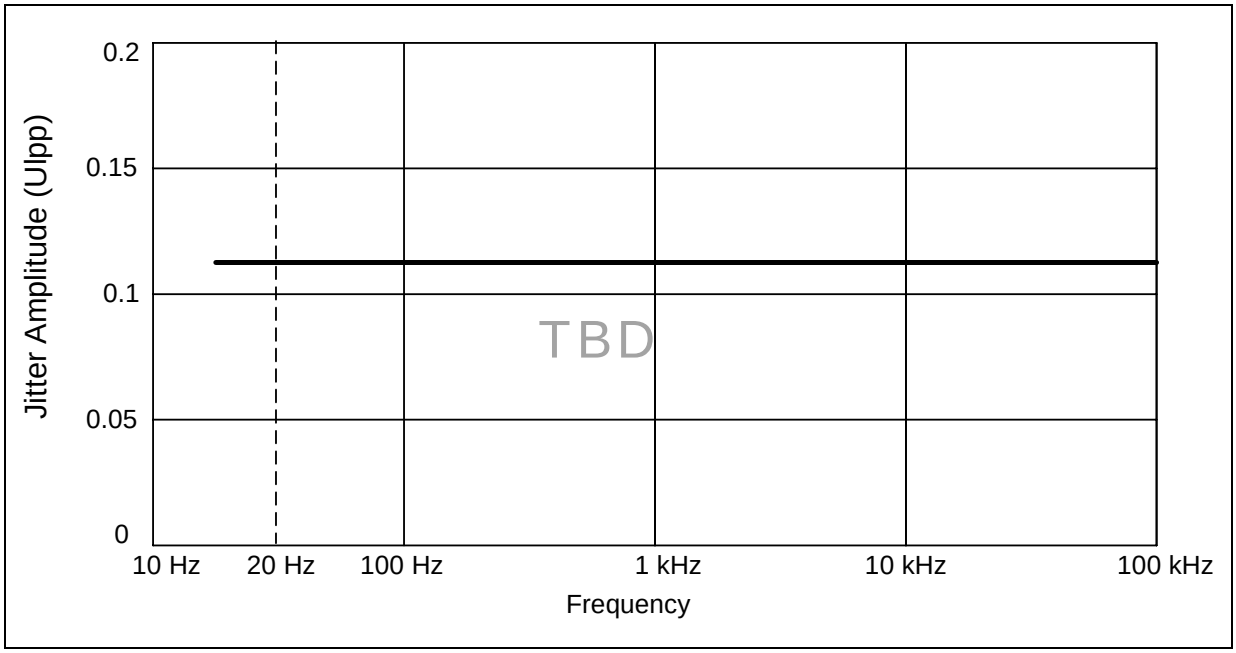


Figure 29. JTAG Timing

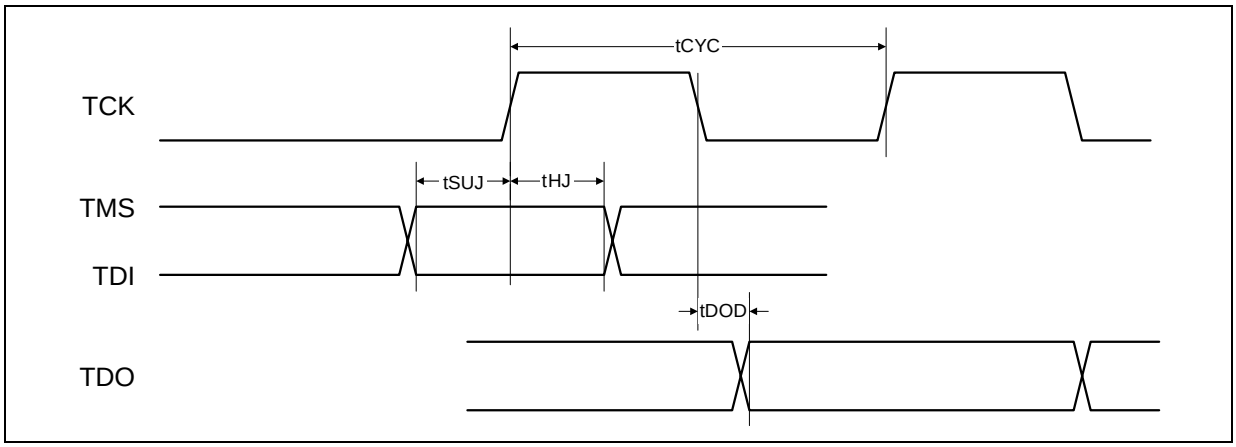


Table 56. JTAG Timing Characteristics

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
Cycle time	tcyc	200	–	–	ns	
J-TMS/J-TDI to J-TCK rising edge time	t_{SUJ}	50	–	–	ns	
J-CLK rising to J-TMS/L-TDI hold time	t_{HJ}	50	–	–	ns	
J-TCLK falling to J-TDO valid	t_{DOD}	-	–	50	ns	

Table 57. G.703 2.048 Mbps Pulse Mask Specifications

Parameter	Cable		Unit
	TWP	Coax	
Test load impedance	120	75	Ω
Nominal peak mark voltage	3.0	2.37	V
Nominal peak space voltage	0 ±0.30	0 ±0.237	V
Nominal pulse width	244	244	ns
Ratio of positive and negative pulse amplitudes at center of pulse	95-105	95-105	%
Ratio of positive and negative pulse amplitudes at nominal half amplitude	95-105	95-105	%

Figure 30. E1, G.703 Mask Templates

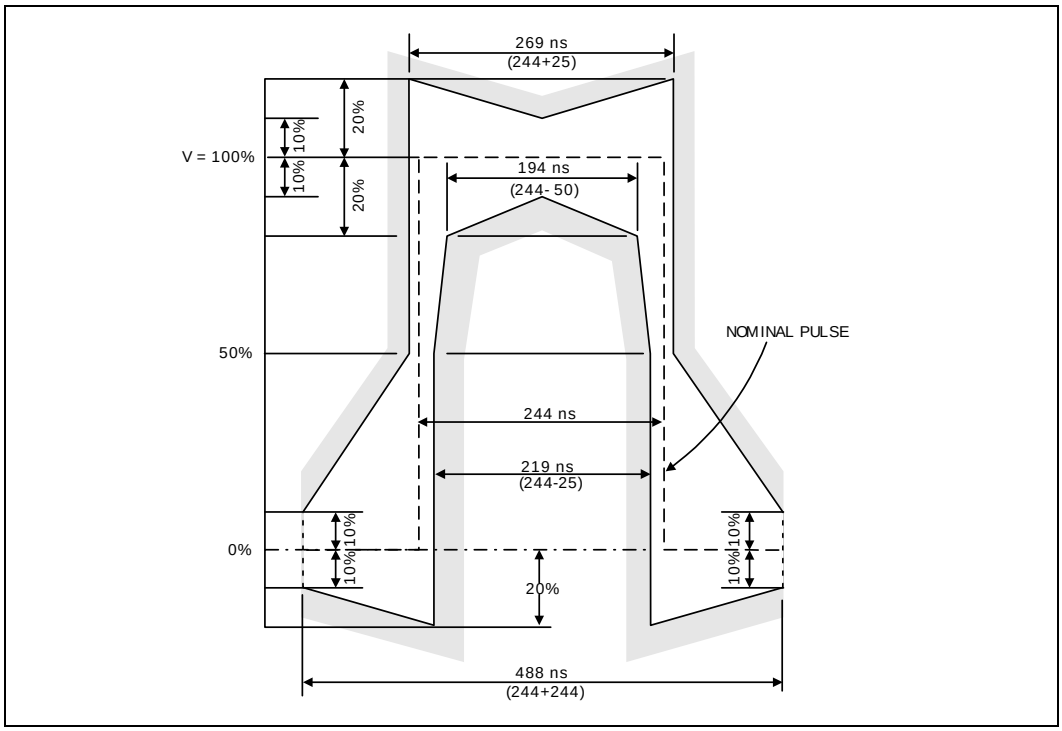


Table 58. T1.102 1.544 Mbps Pulse Mask Specifications

Parameter	Cable	Unit
	TWP	
Test load impedance	100	Ω
Nominal peak mark voltage	3.0	V
Nominal peak space voltage	0 ±0.15	V
Nominal pulse width	324	ns
Ratio of positive and negative pulse amplitudes	95-105	%

Figure 31. LXT3104 Jitter Tolerance Performance

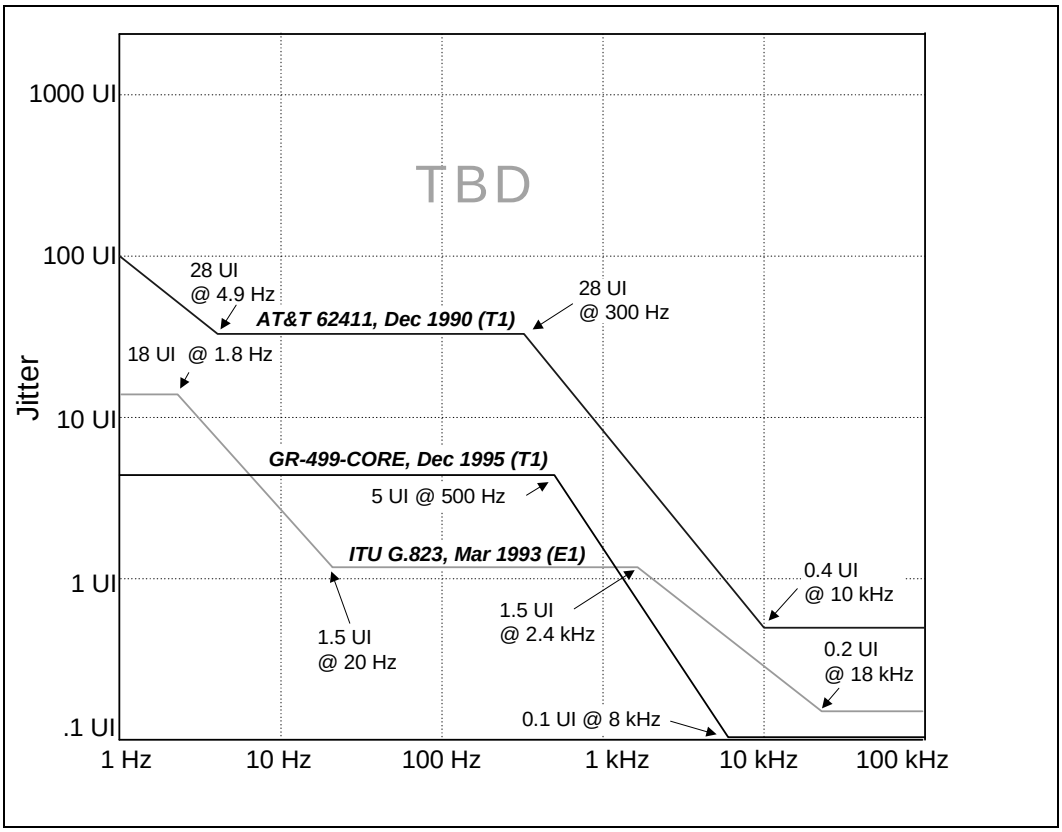
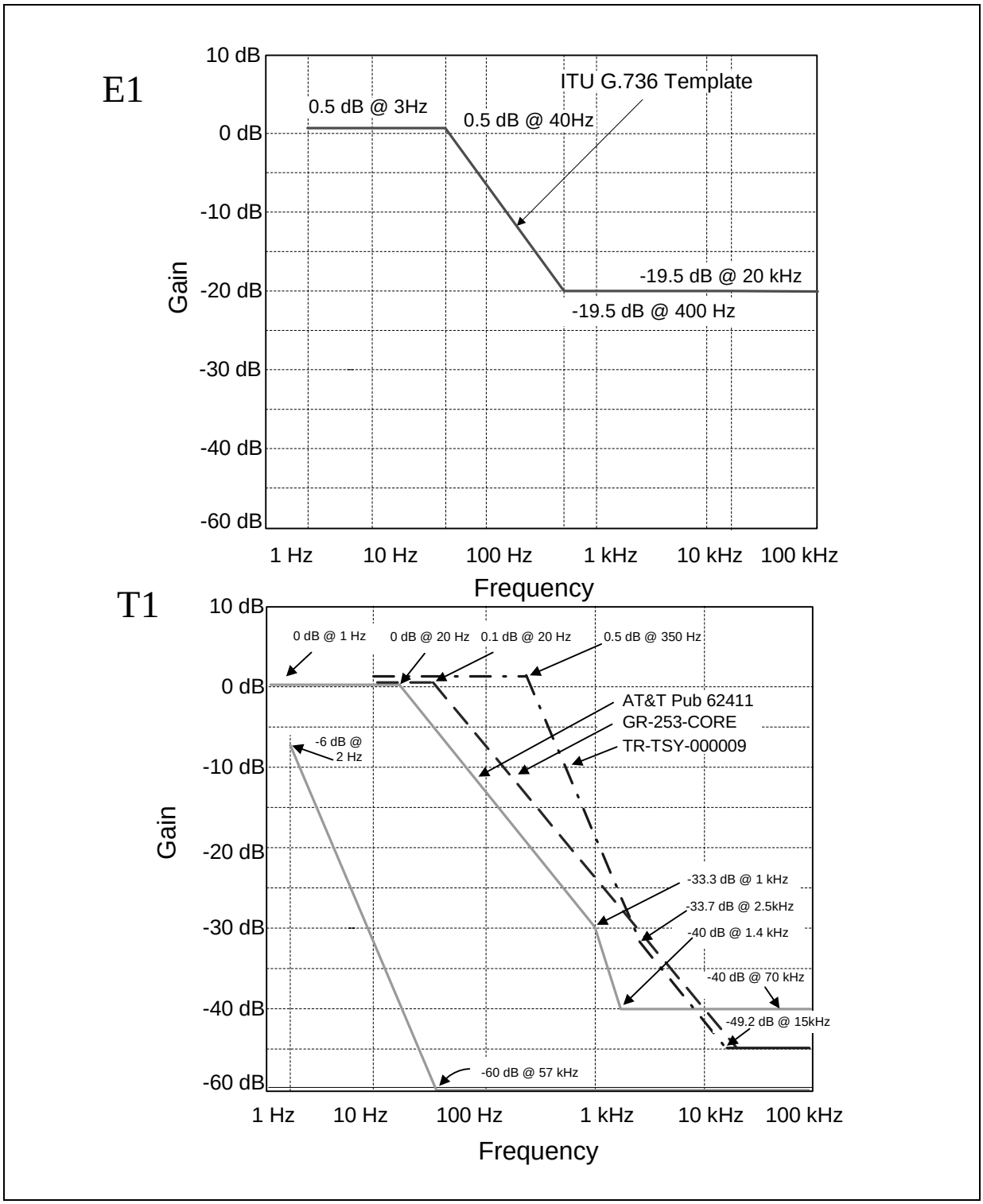


Figure 32. LXT3104 Jitter Transfer Performance



16.1 Supported Microprocessors and Connections

LXT3104 supports direct connection to MPC860, M68360, M68302, i486, i960, and 8051 microprocessors. It has an 8-bit address and data bus. The user can select a particular microprocessor by connecting TYPE1 and TYPE2 pins to VCC or ground. See tables for details.

16.1.1 MPC860/M68360

LXT3104 host interface address and data pins follow the MPC860 endian fashion.

Table 59. MPC860/M68360 Mode

Pin	MPC860	M68360
TYPE1	0	0
TYPE2	0	0
DB(7:0)	D(7:0)	D(0:7)
AD(7:0)	A(31:24)	A(0:7)
CS	CS	CS
DS	OE	OE
RW	R/W#	R/W#
MPI_CLK	WE0	WE0
RDY	TA	DSACK1

16.1.2 M68302

The M68302 (or the M68000 family) is supported in this mode.

Table 60. M68302 Mode

Pin	M68302
TYPE1	0
TYPE2	1
DB(7:0)	D(7:0)
AD(7:0)	A(7:0)
CS	CS
DS	DS
RW	R/W#
MPI_CLK	1
RDY	DTACK

16.1.3 i960/i486

The Intel i960/i486 family is supported in this mode. This is a synchronous bus interface for which most timing is derived off of the MPI_CLK input. Internally, all operations will be performed on the next cycle after ADS is asserted. Two wait state is required.

Table 61. i960/i486 Mode

Pin	i960/i486
TYPE1	1
TYPE2	0
DB(7:0)	D(7:0)
AD(7:0)	A(7:0)
CS	CS
DS	ADS
RW	W/R#
MPI_CLK	CLKO1
RDY	READY

16.1.4 Intel 8051 mode

The MCS-51 family microprocessors are supported. This is the only muxed address and data mode that the LXT3104 supports.

Table 62. 8051 Mode

Pin	Intel 8051
TYPE1	1
TYPE2	1
DB(7:0)	AD(7:0)
AD(7:0)	0
CS	CS
DS	RD
RW	WR
MPI_CLK	ALE
RDY	0

17.0 Host Interface Timing Specifications

17.1 Timing Diagrams

Figure 33. MPC860 Write Timing

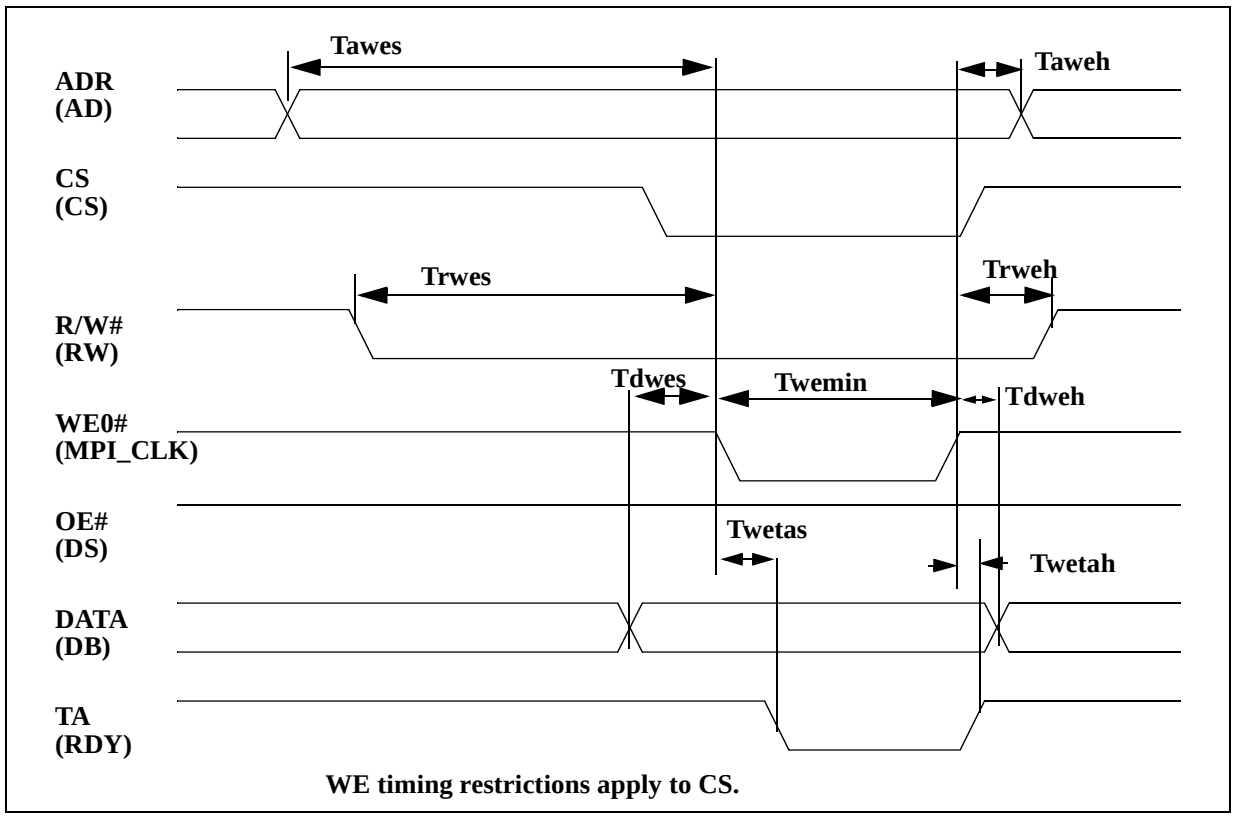


Table 63. MPC860 Write Timing Characteristics

Symbol	Parameter	Min	Max	Unit
Tawes	Address setup to WE	15	--	ns
Taweh	Address hold from WE	5	--	ns
Trwes	R/W# setup to WE	5	--	ns
Trweh	R/W# hold from WE	5	--	ns
Tdwes	Data setup to WE	0	--	ns
Tdweh	Data hold from WE	5	--	ns
Twemin	WE minimum width	30	--	ns
Twetas	WE low to TA asserted	TBD	TBD	ns
Twetah	WE high to TA inactive	TBD	TBD	ns

Figure 34. MPC860 Read Timing

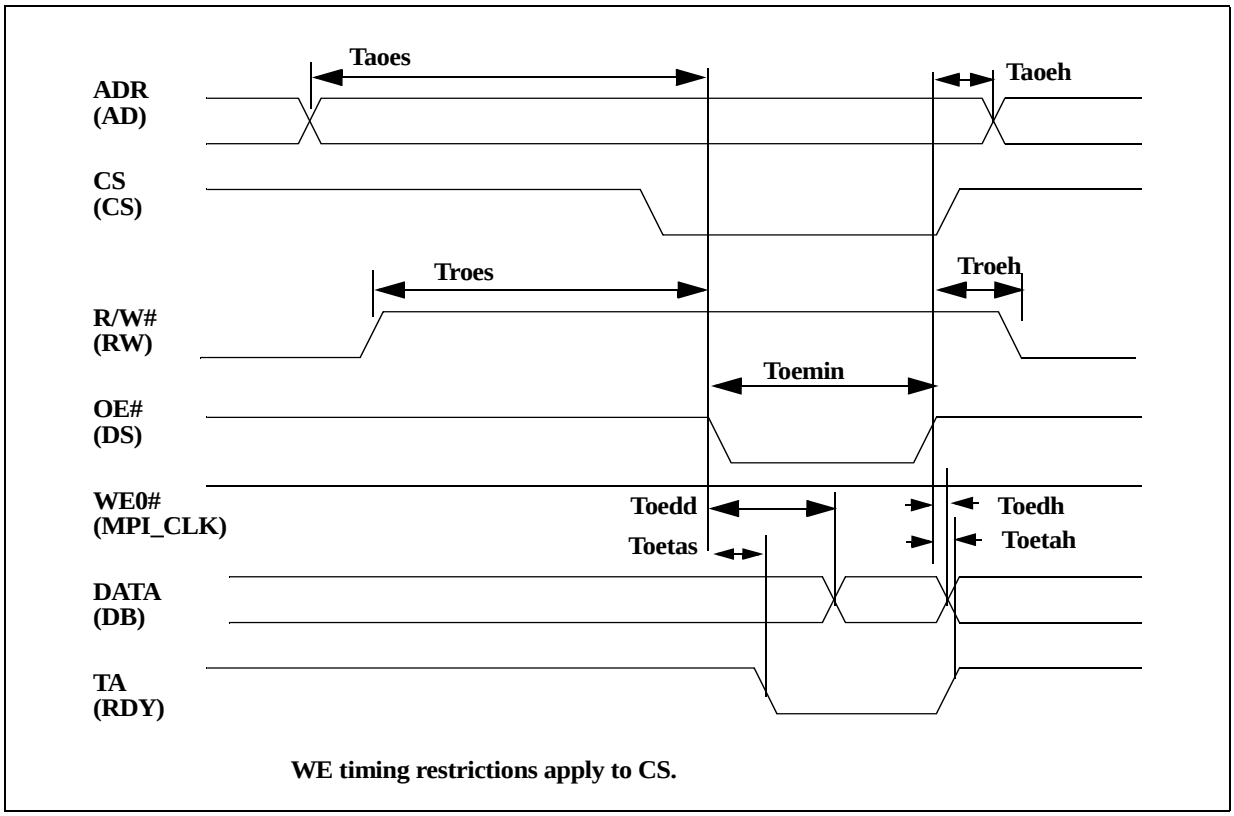


Table 64. MPC860 Read Timing Characteristics

Symbol	Parameter	Min	Max	Unit
Taoes	Address setup to OE	15	--	ns
Taoeh	Address hold from OE	5	--	ns
Troes	R/W# setup to OE	5	--	ns
Troeh	R/W# hold from OE	5	--	ns
Toedd	OE asserted to data valid	TBD	TBD	ns
Toedh	OE high to data invalid	5	--	ns
Toemin	OE minimum width	65	--	ns
Toetas	OE low to TA asserted	TBD	TBD	ns
Toetah	OE high to TA inactive	TBD	TBD	ns

Figure 35. M68302 Write Timing

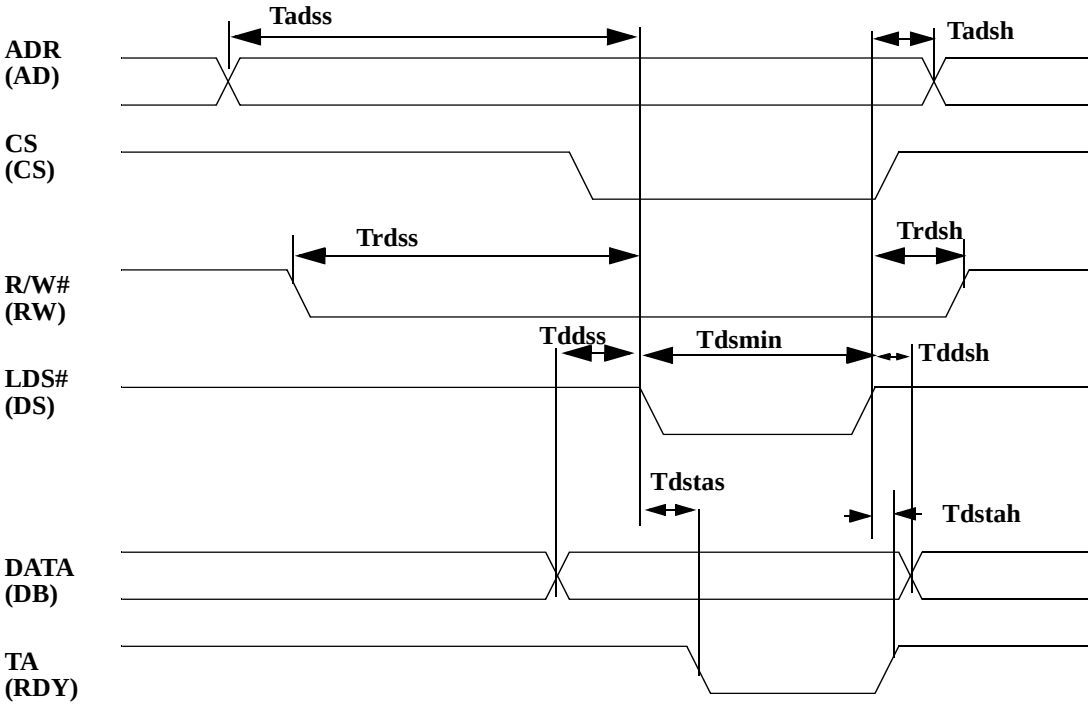


Table 65. M68302 Write Timing Characteristics

Symbol	Parameter	Min	Max	Unit
Tadss	Address setup to LDS	10	--	ns
Tadsh	Address hold from LDS	5	--	ns
Trdss	R/W# setup to LDS	5	--	ns
Trdsh	R/W# hold from LDS	5	--	ns
Tddss	Data setup to LDS	0	--	ns
Tddsh	Data hold from LDS	5	--	ns
Tdsmin	LDS minimum width	55	--	ns
Tdstas	LDS asserted to TA valid	TBD	TBD	ns
Tdstah	LDS desserted to TA invalid	TBD	TBD	ns

Figure 36. M68302 Read Timing

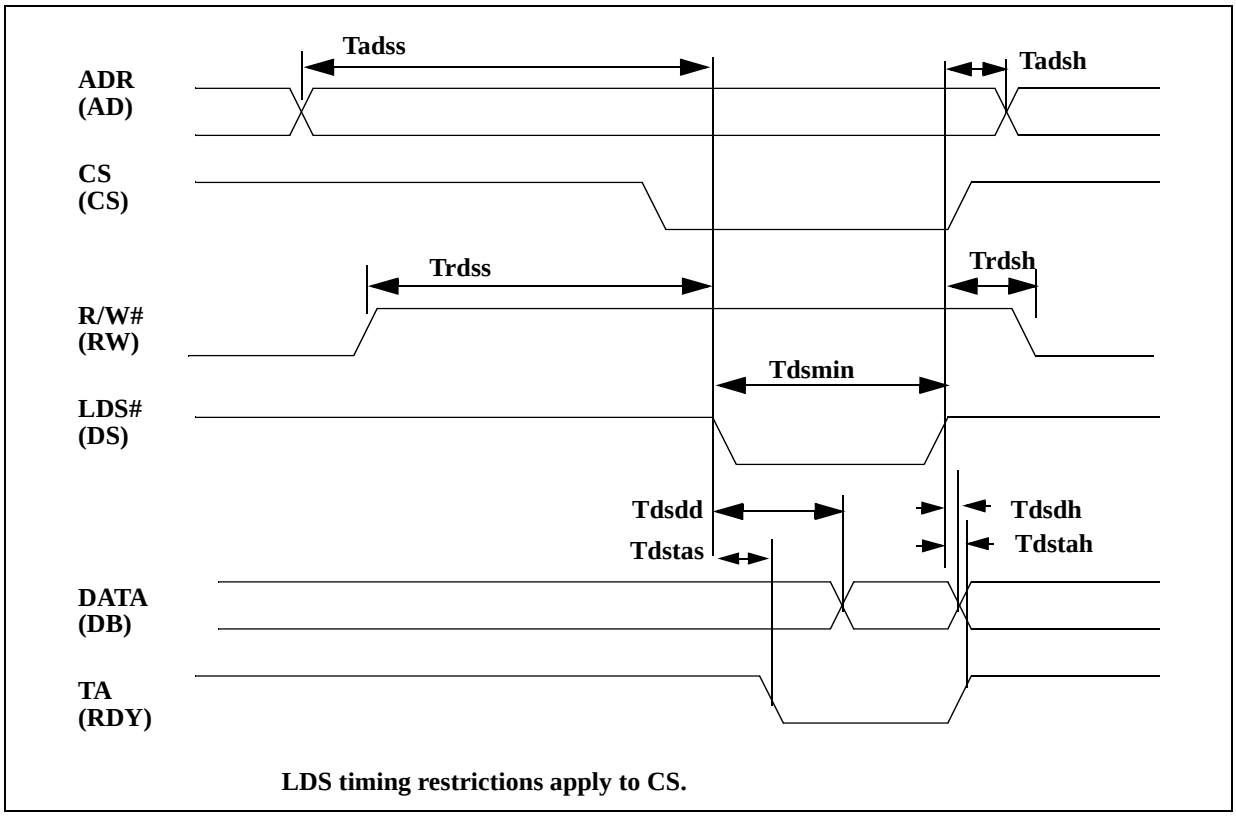


Table 66. M68302 Read Timing Characteristics

Symbol	Parameter	Min	Max	Unit
Tadss	Address setup to LDS	10	--	ns
Tadsh	Address hold from LDS	5	--	ns
Trdss	R/W# setup to LDS	5	--	ns
Trdsh	R/W# hold from LDS	5	--	ns
Tdsdd	LDS low to data valid	TBD	TBD	ns
Tdsdh	Data hold from LDS high	5	--	ns
Tdsmin	LDS minimum width	65	--	ns
Tdstas	LDS low to TA valid	TBD	TBD	ns
Tdstah	LDS high to TA invalid	TBD	TBD	ns

Figure 37. i486/i960 Write Timing

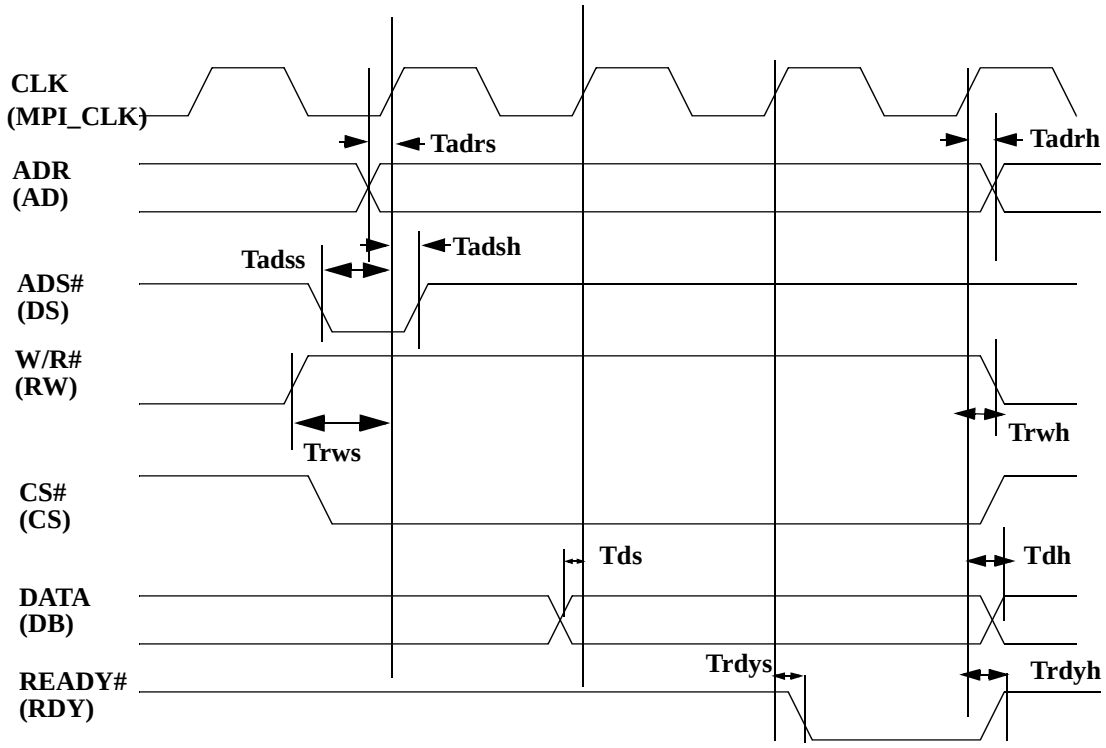


Table 67. i486 Write Timing Characteristics

Symbol	Parameter	Min	Max	Unit
Tadrs	Address setup to clock	14	--	ns
Tadrh	Address hold from clock	3	--	ns
Tadss	ADS setup to clock	5	--	ns
Tadsh	ADS hold from clock	3	--	ns
Trws	W/R# setup to clock	14	--	ns
Trwh	W/R# hold from clock	5	--	ns
Tds	Data setup to clock	19	--	ns
Tdh	Data hold from clock	5	--	ns
Trdys	Clock to READY# asserted	TBD	TBD	ns
Trdyh	Clock to READY# deasserted	TBD	TBD	ns

Figure 38. i486/i960 Read Timing

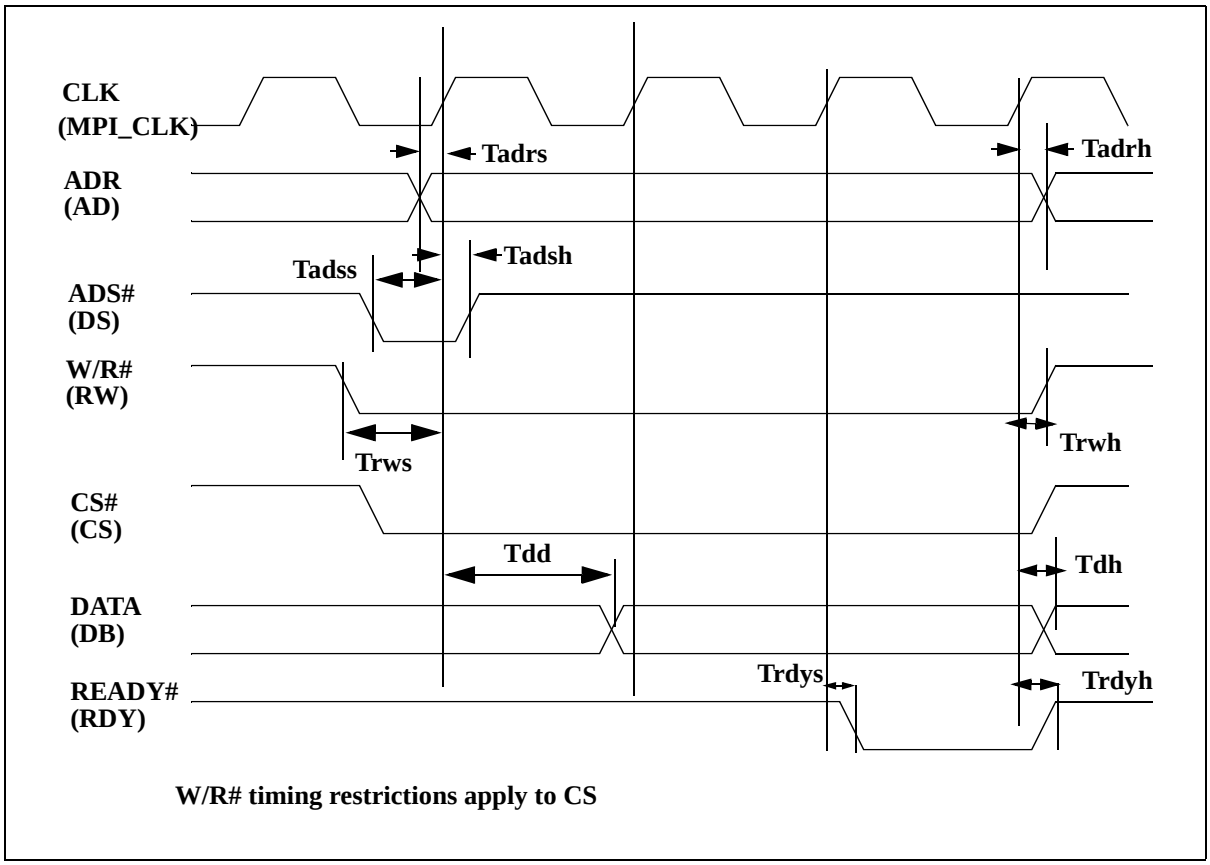


Table 68. i486/i960 Read Timing Characteristics

Symbol	Parameter	Min	Max	Unit
Tadrs	Address setup to clock	14	--	ns
Tadrh	Address hold from clock	3	--	ns
Tadss	ADS setup to clock	5	--	ns
Tadsh	ADS hold from clock	3	--	ns
Trws	W/R# setup to clock	14	--	ns
Trwh	W/R# hold from clock	3	--	ns
Tdd	Clock to Data valid	TBD	TBD	ns
Tdh	Data hold from clock	3	--	ns
Trdys	Clock to READY# asserted	TBD	TBD	ns
Trdyh	Clock to READY# deasserted	TBD	TBD	ns

Figure 39. 8051 Write Timing

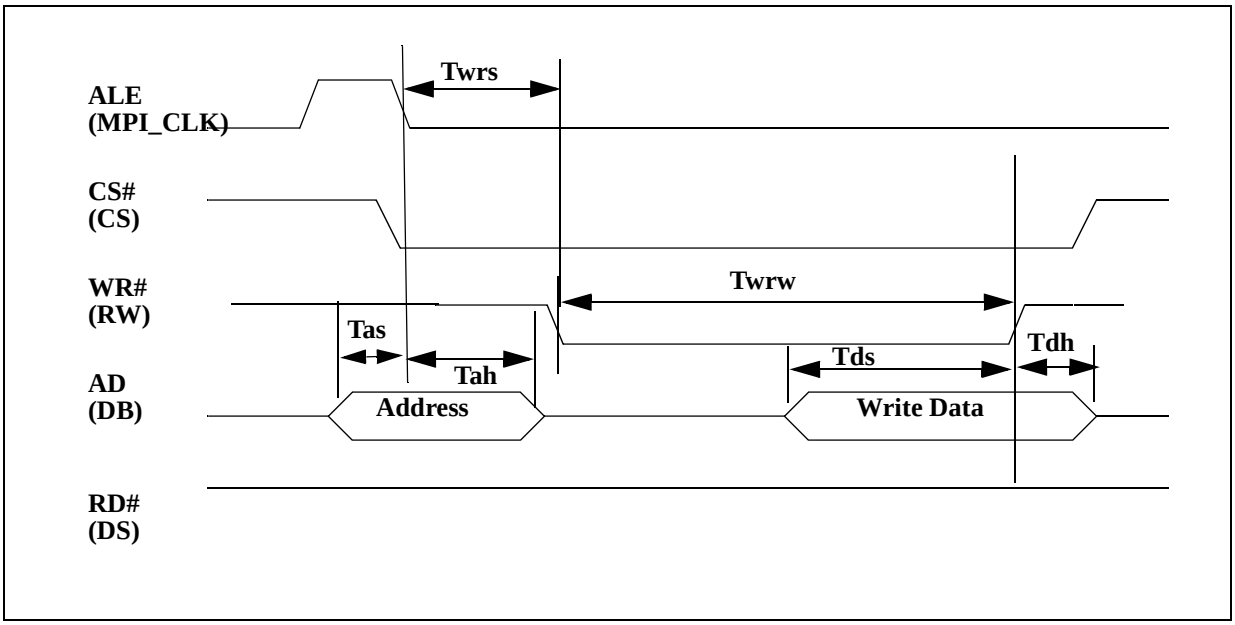


Table 69. 8051 Write Timing Characteristics

Symbol	Parameter	Min	Max	Unit
Twrs	ALE low to WR# low	9	--	ns
Twrw	WR# active width	55	--	ns
Tas	Address setup to ALE	9	--	ns
Tah	Address hold from ALE	9	--	ns
Tds	Write data setup to WR#	40	--	ns
Tdh	Write data hold from WR#	10	--	ns

Figure 40. 8051 Read Timing

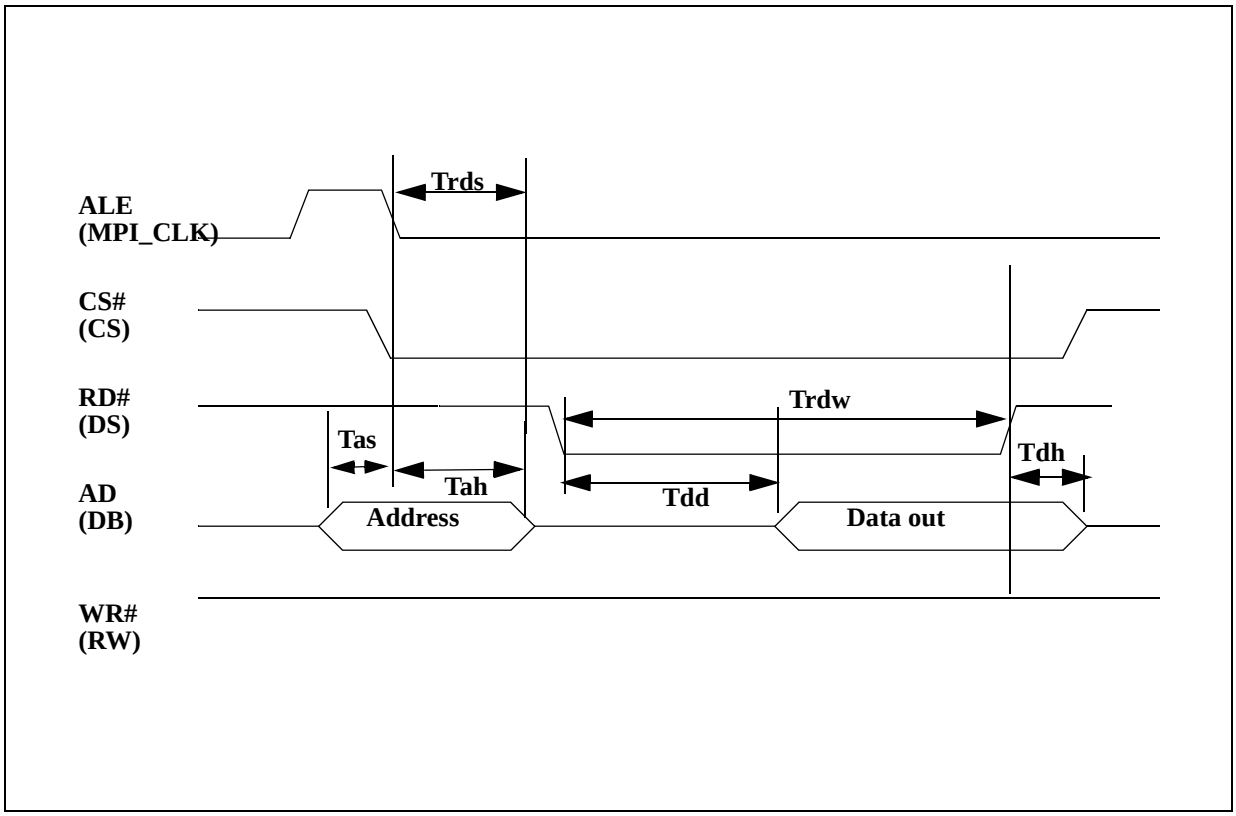


Table 70. 8051 Read Timing Characteristics

Symbol	Parameter	Min	Max	Unit
Trds	ALE low to RD# low	9	--	ns
Trdw	RD# active width	76	--	ns
Tdd	RD# asserted to read data valid	30	40	ns
Tdh	Data hold from RD# deasserted	9	--	ns
Tas	Address setup to ALE	9	--	ns
Tah	Address hold from ALE	9	--	ns

17.2 Referenced Standards

AT&T Pub 62411

Bellcore TR-TSY-000009 Asynchronous Digital Multiplexes Requirements and Objectives

Bellcore GR-253-CORE SONET Transport Systems Common Generic Criteria

Bellcore GR-499-CORE Transport Systems Generic Requirements

ANSI T1.102 - 199X Digital Hierarchy Electrical Interface

ANSI T1.231 -1993 Digital Hierarchy Layer 1 In-Service Digital Transmission Performance Monitoring

ETS 300166 Physical and Electrical Characteristics

ETS 300386-1 Electromagnetic Compatibility Requirement

G.703 Physical/electrical characteristics of hierarchical digital interfaces

G.704 Functional characteristics of interfaces associated with network nodes

G.735 Characteristics of Primary PCM multiplex equipment operating at 2048 kbps and offering digital access at 384 kbps and/or synchronous digital access at 64 kbps

G.736 Characteristics of a synchronous digital multiplex equipment operating at 2048 kbps

G.772 Protected Monitoring Points provided on Digital Transmission Systems

G.775 Loss of signal (LOS) and alarm indication (AIS) defect detection and clearance criteria

G.783 Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks

G.823 The control of jitter and wander within digital networks which are based on the 2048 kbps hierarchy

O.151 Specification of instruments to measure error performance in digital systems

OFTEL OTR-001 Short Circuit Current Requirements

18.0 Mechanical Specification

Figure 41. LXT3104BE 256 PBGA Mechanical Specification

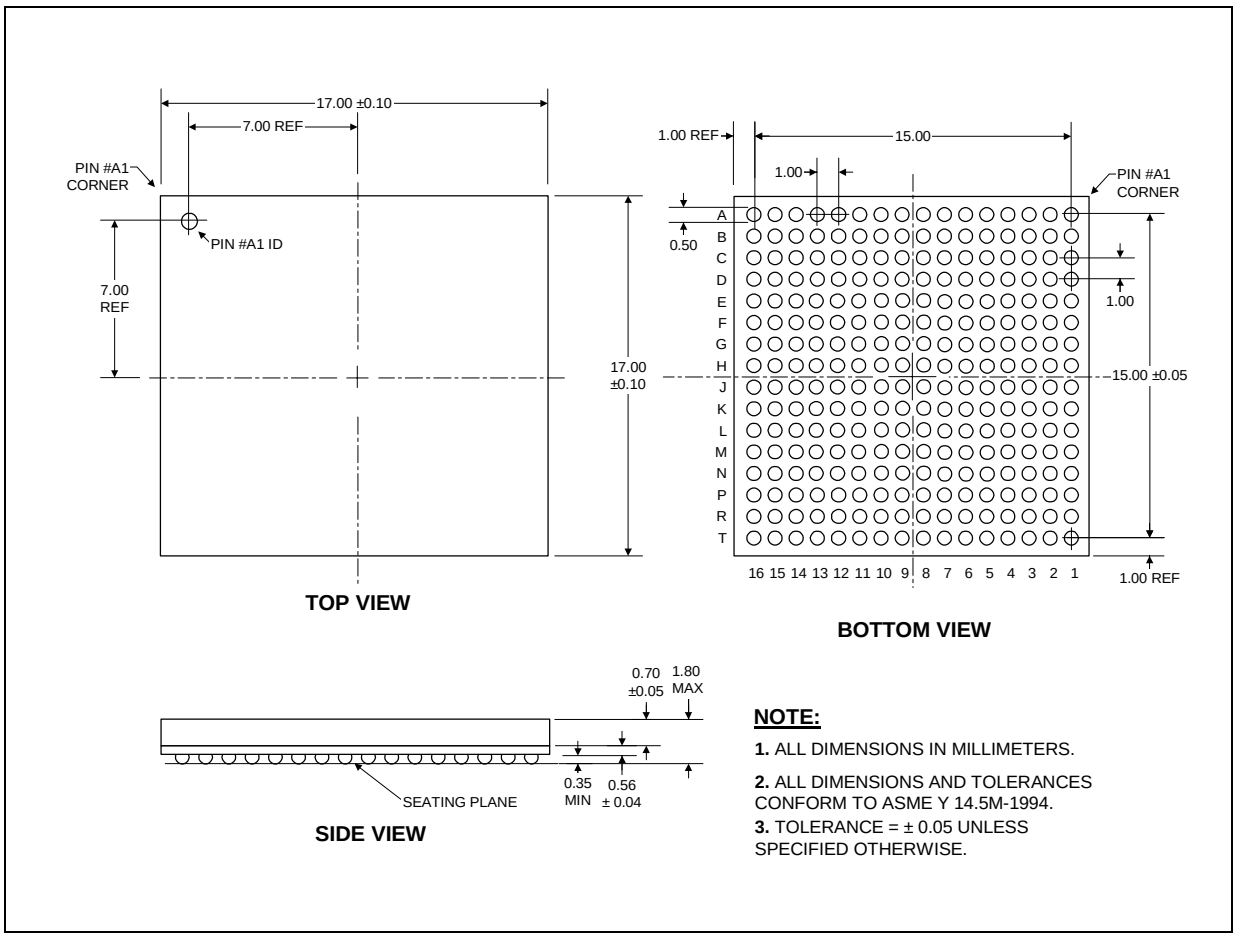
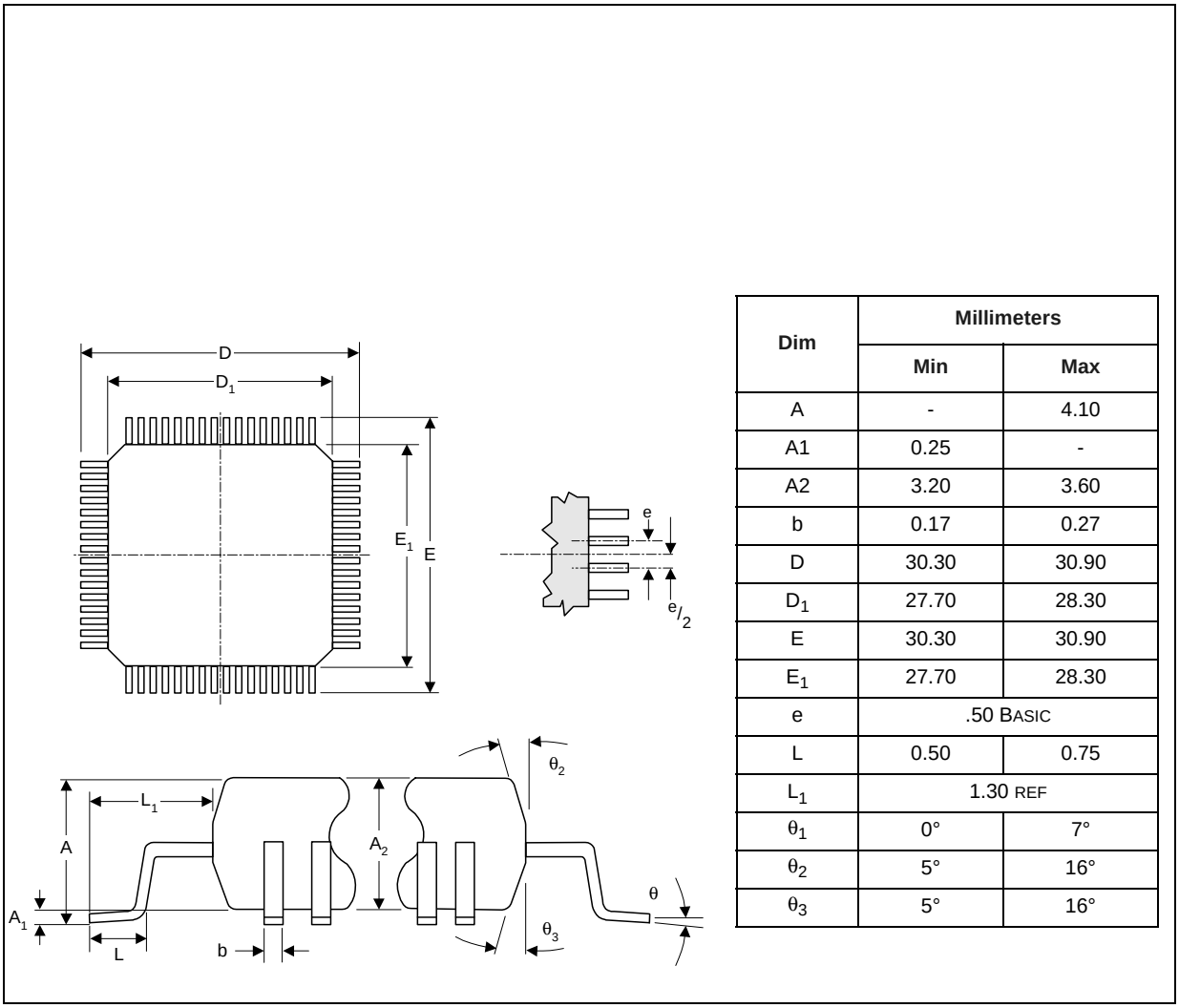


Figure 42. LXT3104HE 208 Pin QFP Mechanical Specifications



Dim	Millimeters	
	Min	Max
A	-	4.10
A1	0.25	-
A2	3.20	3.60
b	0.17	0.27
D	30.30	30.90
D_1	27.70	28.30
E	30.30	30.90
E_1	27.70	28.30
e	.50 BASIC	
L	0.50	0.75
L_1	1.30 REF	
θ_1	0°	7°
θ_2	5°	16°
θ_3	5°	16°

19.0 Glossary

Term Categories

Term	Term definition
ADC	Analog to Digital Converter
AFE	Analog Front End
AGC	Automatic Gain Control
ATWG	Arbitrary Transmit Wave Generation
BPV	Bi-Polar Violation
BSR	Boundary Scan Register
BYR	BYpass Register
CLAD	CLock ADapter
DAC	Digital to Analog Converter
DJA	Digital Jitter Attenuator
DSP	Digital Signal Processor
FIR	Finite Infinite Response
GUI	Graphical User Interface
HPS	Intel® Hitless Protection Switching, Intel® HPS
IADs	Integrated Access Devices
IDR	Device Identification Register
IMAPs	Integrated Multi-service Access Platforms
IR	Instruction Register
JTAG	Joint Test Action Group
LIU	Line Interface Unit
LH	Long Haul
LH/SH	Long Haul/Short Haul
LOS	Loss Of Signal
MQFP	Metric Quad Flat Pack
NRZ	Non-Return-to-Zero
PBGA	Plastic Ball Grid Array
POR	Power On Reset
PPR	Port Page Register
PPRB	Port Page Register Bank
PPS	Port Page Select
PQFP	Plastic Quad Flat Pack
PRM	Intel® On-Chip Performance Report Messaging (Intel® PRM)
PTM	Intel® Pulse Template Matching (Intel® PTM)
QFP	Quad Flat Pack
SH	Short Haul
TBD	To Be Determined
TAOS	Transmit All Ones
UI	Unit Interval