Intel® LXT331 Dual Transceivers with PMC PM4344/6344 Quad Framers

Application Note

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As of January 15, 2001, this document replaces the Level One document known as *AN058*.

Application Note

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1.0 General Description

The LXT331 dual T1/E1 LIU interfaces with PMC-Sierra PM4344/6344 quad framers, providing a very compact and cost-effective four-port solution. This Application Note describes an appropriate configuration of both the LXT331 and the PMC quad framers.

The LXT331 is a high-performance dual T1/E1 line interface unit providing a rich set of features including: data recovery, stand-alone hardware mode or serial host mode, analog loopback and driver performance monitoring. It also features a constant low impedance transmit driver for optimum transmit return loss, and switchable T1/E1 operation without component changes.

The PMC-Sierra PM4344 (T1 framer) and PM6344 (E1 framer) are quad port framers suitable for use in most T1/E1 applications with a minimum of external circuitry. Relevant features include: clock recovery, alarm condition detection (such as loss of signal, loss of framing, and AIS) digital jitter attenuator (configurable for receive or transmit side), HDLC message termination and performance monitoring.

The design shown in Figure 1 uses an octal transformer from HALO Electronics that interfaces directly with the LXT331. As the first surface-mount octal T1/E1 transformer in the industry, this compact device supports all four channels in a quad port design (transmit and receive) and can be used both for T1 and E1 operation.

1.1 Solution Benefits

- T1/E1 operation with single board design
  - Single transformer and LIU for 75/100/120 Ω systems; pin-compatible framers
- No high frequency reference clock required
- Minimal board real estate
- Sophisticated driver monitoring
  - Secondary short detection
  - Driver performance monitoring
  - Tristate capability for 1+1 protection applications
  - Meets BABT 50 mA driver short circuit current limit by design

1.2 Reference Layout

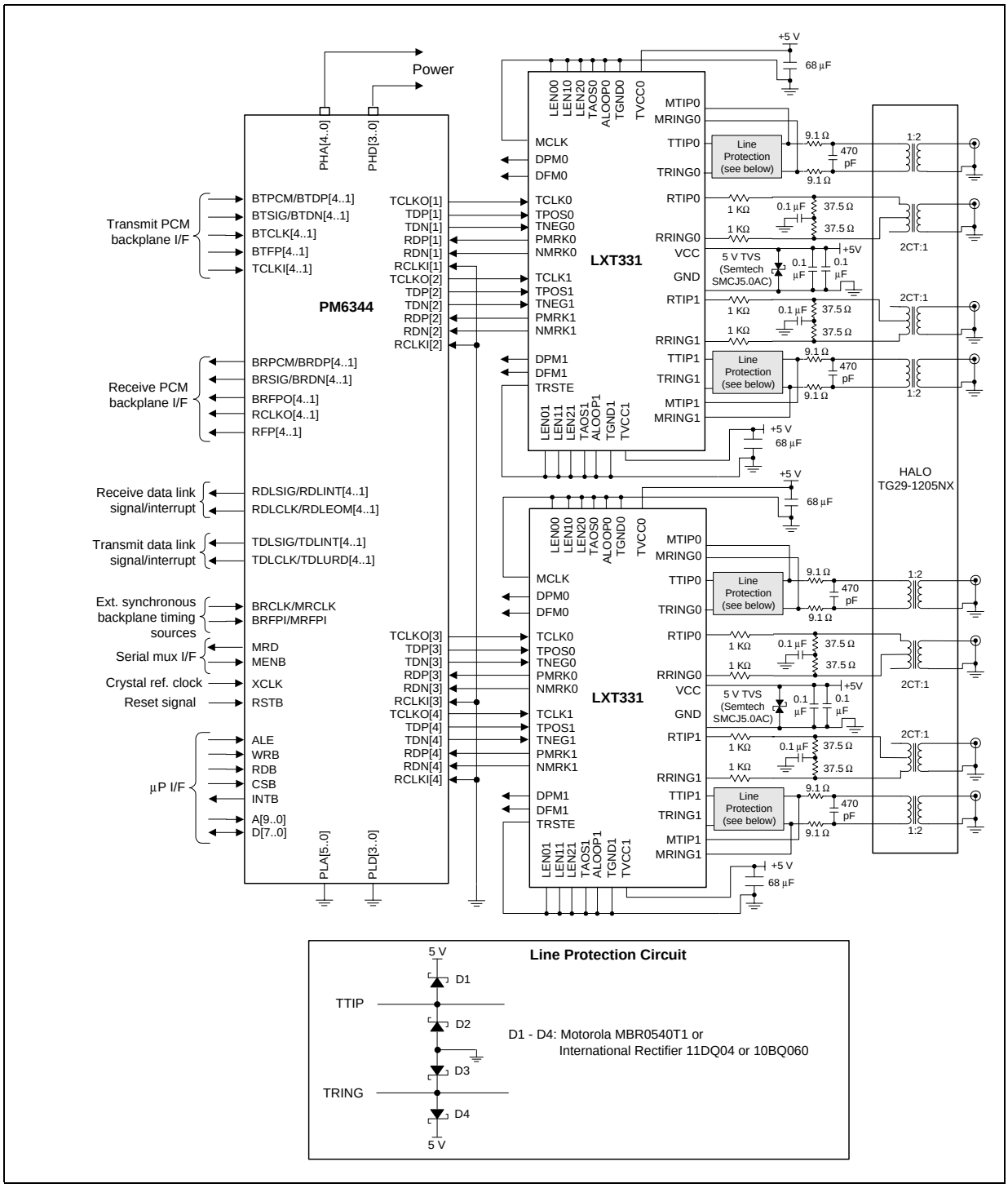
Figure 1 shows a layout diagram of a four port solution that includes two dual transceivers and one quad framer for an E1 75Ω coaxial cable interface. For a T1 solution, the framer would be the PM4344, that is pin compatible with the PM6344 EQUAD. The LXT331 is T1/E1 switchable. For T1 operation, choose the appropriate line length settings LEN<0:2>, and adjust the receive termination to 100Ω. Refer to the LXT331 data sheet for additional details. The octal transformer from HALO can be used for both T1 and E1 applications.

At the network side, the transmit and receive lines interface with the LXT331 LIU through the TG29-1205NX octal transformer. The transmit transformer has a 1:2 turns ratio. The receive transformer is a 1:2 center-tap used at a 1:1 turns ratio. The receive side 37.5Ω resistors provide adequate termination and low common mode impedance for an E1 coaxial cable interface. On the transmit side, the 9.1Ω series resistors between the transformer and the LIU provide excellent transmit return loss (18 dB typical). This provides a good margin for compliance with the latest ETSI standards such as ETS 300 166. Furthermore, the resistors also ensure maximum protection against excessive surge currents and allow compensation for amplitude loss in external protection networks.

In Figure 1, the LXT331 is configured in hardware mode. This mode does not require the allocation of any microprocessor resources. However, if microprocessor control is preferred, the device can be configured for host mode to allow control through a simple, three-wire serial interface. In Figure 1, the line length inputs are set to LEN<0:2>=000 (E1 75Ω operation). If TCLK is provided, the MCLK input can be grounded.

The PM6344 EQUAD is configured for dual rail input (RDP*x*, RDN*x*) and Return-to-Zero (RZ) mode. The clock recovery block inside the framer extracts the clock and the analog LOS information from the RZ pulses provided by the LXT331, using a digital PLL. Digital loss of signal detection, HDB3 decoding and bipolar violation detection are also included in this device.

Figure 1. E1 75Ω Coax Quad Port Layout

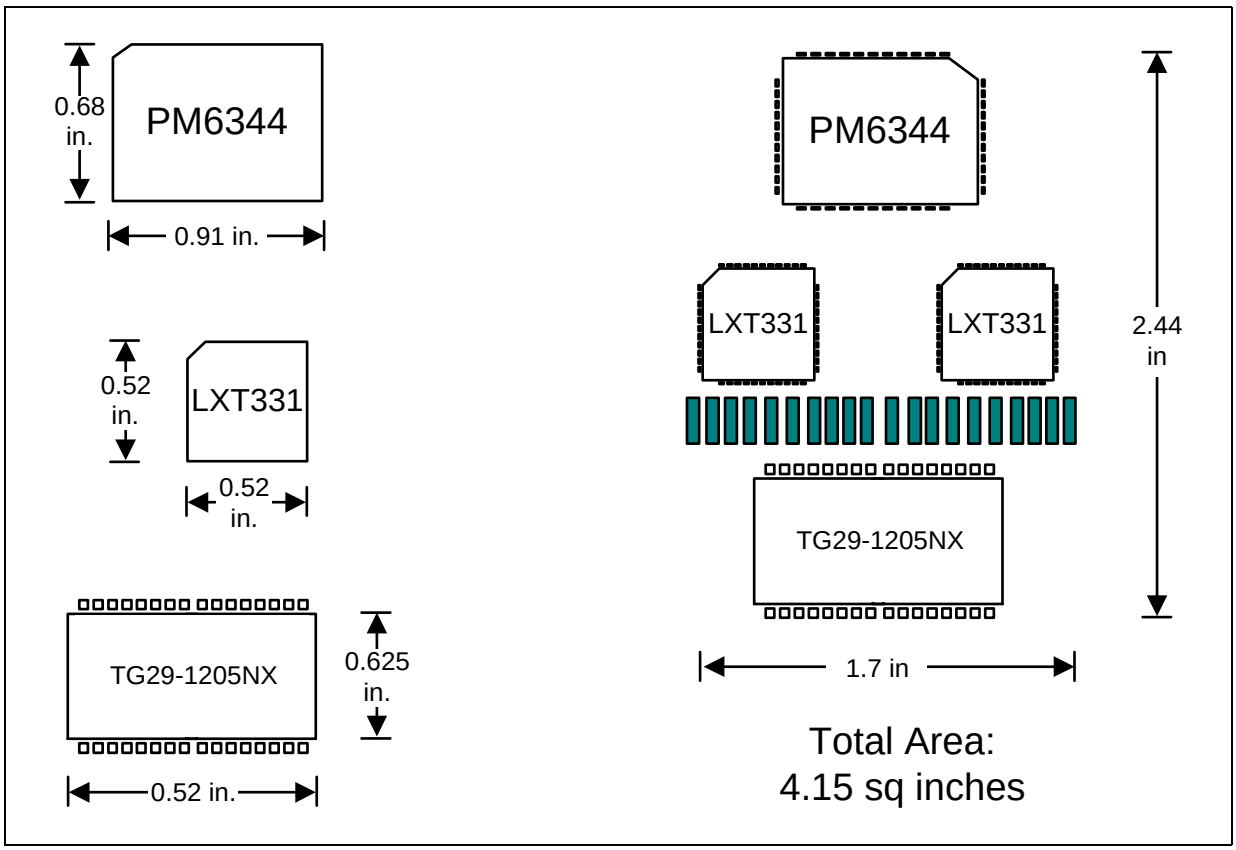


In normal operation, the PM6344 Digital Jitter Attenuator (DJAT) is placed in the transmit direction. The elastic store in the receive side provides adaptation between the recovered line clock and the backplane clock (BRCLK). When the backplane timing is derived from the receive line data (i.e. the RCLKO*x* output is used) the elastic store can be combined with the DJAT digital PLL to provide receive jitter attenuation. This is accomplished by locking the elastic store output clock to the de-jittered recovered clock.

The framer backplane signals are also represented in Figure 1. These signals would be further processed in a real application.

Figure 2 shows an approximate measurement of area for the quad port design described above. Real package sizes were used to make this measurement. A total of only 4.15 sq inches is required for the complete solution. The LXT331 is also available in a very compact QFP package.

Figure 2. Total Component Area



1.3 References

- LXT331, Dual T1/E1 Line Interface Unit Data Sheet, Intel
- Communication ICs Data Book 1996, Intel
- PM6344, Quadruple E1 Framer Data Sheet, PMC-Sierra Inc.
- PM4344, Quadruple T1 Framer Data Sheet, PMC-Sierra Inc.

- PM6344 EQUAD, Answers to Frequently Asked Questions Regarding the EQUAD, PMC-Sierra Inc.
- PM4344 TQUAD, Answers to Frequently Asked Questions Regarding the TQUAD, PMC-Sierra Inc.
- TG29-1205NX Transformer Data Sheet, Halo Electronics Inc.