LXT335

Quad Short-Haul PCM Analog Interface

Datasheet

The LXT335 is a quad, short-haul, PCM analog line interface for 2.048 Mhz transmission systems. It includes four independent data receivers and four independent line drivers in a single, 64-pin QFP package. Its low impedance transmit output drivers provide constant line impedance whether transmitting marks or spaces. The output pulse amplitudes are also constant, and are stabilized against supply voltage variations. The LXT335 is configurable for either balanced 120 Ω or unbalanced 75 Ω systems and exceeds latest ETSI return loss recommendations. All transmitters incorporate a power down mode with output tri-stating.

The LXT335 features a differential receiver architecture with high noise interference margin. It uses peak detection with a variable threshold for reliable data recovery as low as 500 mV (up to 12 dB of cable attenuation). Each receiver incorporates an analog loss of signal (LOS) detector that meets latest ITU standards. The LXT335 features a driver failure monitoring circuit in parallel to TTIP and TRING that reports driver shorts.

Applications

- High-density E1 line interface cards using digital backend ASICS
- Multiplexers, digital crossconnects, SDH systems

Product Features

- Quad E1 short haul PCM analog front-end per ITU G.703
- Single rail supply voltage of 5 V (typical)
- Low power consumption of 410 mW (typical)
- Four independent high-performance line drivers with constant low impedance for typical 20 db return loss
- Voltage stabilized output amplitudes
- Four high performance line receivers with 14 db, single tone interference margin
- Data recovery for cable attenuation of up to 12 db at 1024 khz
- On-chip driver short circuit monitoring function
- Local and remote loopback testing function
- Small footprint 64-pin QFP package

As of January 15, 2001, this document replaces the Level One document *LXT335 — Quad Short-Haul PCM Analog Interface*.

Order Number: 249047-001
January 2001

Datasheet

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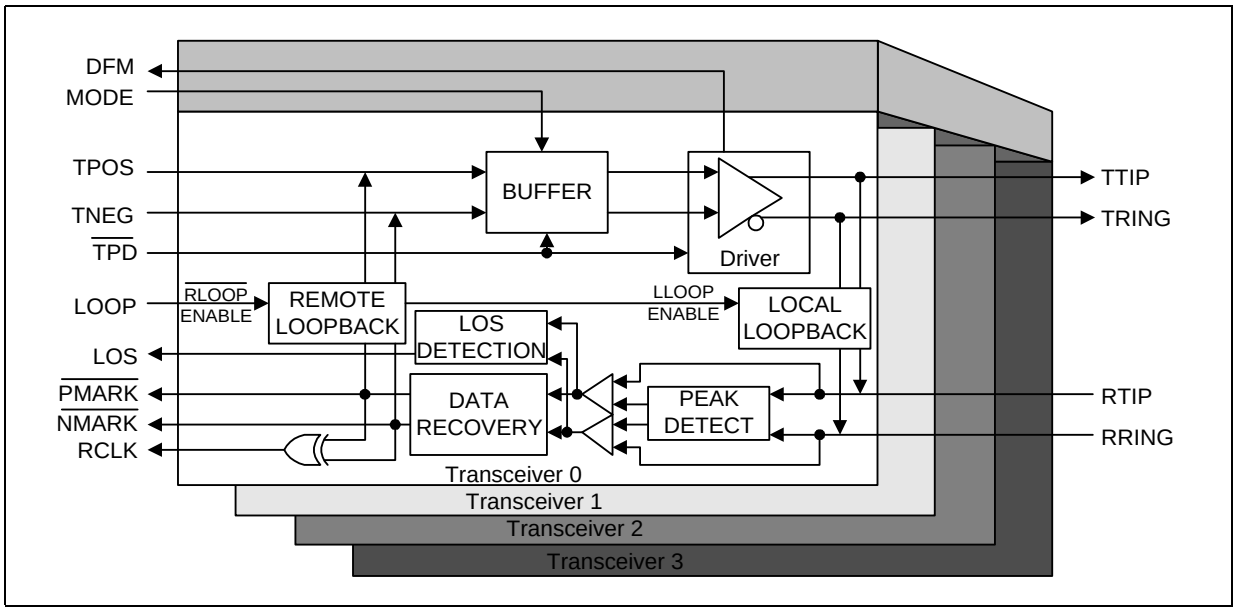
Revision History

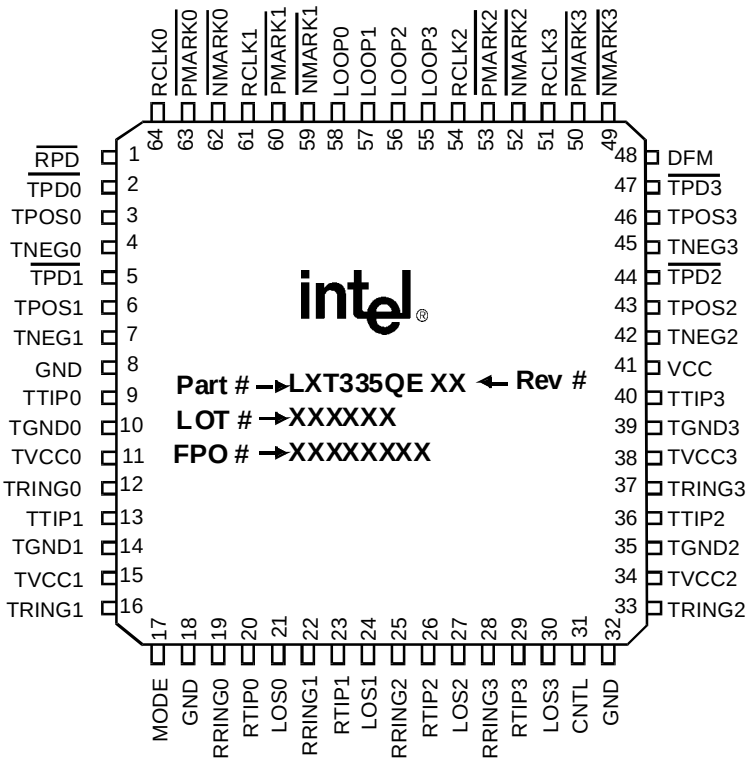
Revision	Date	Description

Figure 1. LXT335 Block Diagram



1.0 Pin Assignments and Signal Descriptions

Figure 2. LXT335 64Pin Assignments and Markings



Package Topside Markings

Marking	Definition
Part #	Unique identifier for this product family.
Rev #	Identifies the particular silicon “stepping” — refer to the specification update for additional stepping information.
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

2.0 Functional Description

Page 1 shows a simplified block diagram of the LXT335. The LXT335 is a quad line interface unit with four on-chip transmit drivers and four data receivers optimized for G.703 2.048 MHz applications. The front end of each line interface interfaces with four lines, one pair for transmit, one pair for receive. These two lines comprise a digital data loop for full duplex transmission. Each line interface also interfaces with back-end processors, through bipolar data I/O channels, and allows control by hardwired pins for stand-alone operation.

2.1 Receiver

The four LXT335 receivers are identical. The following paragraphs describe the operation of a single receiver. LXT335 receives the input signal via a 1:1 transformer. Recovered data is active low and output at $\overline{\text{PMARK}}$ and $\overline{\text{NMARK}}$. Timing information for external clock recovery is output at RCLK.

A peak detector and data slicers process the received signal. The peak detector samples the received signal and determines its maximum value. A percentage of the peak value is provided to the data slicers as a threshold level of 50% to ensure an optimum signal-to-noise ratio.

The receiver is capable of accurately recovering signals with up to 12 dB of cable attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Regardless of received signal level, LXT335 holds its peak detectors above a minimum level of 0.225 V (typical) to provide immunity from impulsive noise.

After the data slicers process, the received signal goes to the data recovery and pulse stretcher section and then to the receive outputs $\overline{\text{PMARK}}$ and $\overline{\text{NMARK}}$.

2.1.1 Loss Of Signal Detector

The Loss of Signal Detector uses an analog detection scheme and complies with the ITU G.775 recommendation. During LOS conditions, received data is output on $\overline{\text{PMARK}}$/$\overline{\text{NMARK}}$. Any signal ~22 dB below the nominal 0 dB signal generates a loss of signal condition. LOS is deactivated again when the signal level rises to more than ~21 dB (typical) below the minimum 0 dB level. The $\overline{\text{PMARK}}$ and $\overline{\text{NMARK}}$ outputs stay active for external digital signal transition detection.

2.2 Transmitter

The four LXT335 low power transmitters are identical. The following paragraphs describe the operation of a single transmitter.

Bipolar transmit data from the digital backend processor is fed into the device at TPOS/TNEG and is passed through “as is”. If $\overline{\text{TPD}}$ is asserted Low the transmitter remains powered down and the TTIP/TRNG outputs are held in a High-Z state. This feature allows use of the LXT335 in fully redundant applications.

Each output driver is supplied by a separate power supply (TVCC0 to TVCC3, TGND0 to TGND3). Current limiters on the output drivers provide short circuit protection and generate a driver failure monitoring signal in case the current limit is exceeded.

The transmitted pulse shape must be generated externally. Pulses are applied to the line drivers for transmission onto the line at TTIP and TRING. The line driver provides a constant low output impedance of < 3 Ω (typical) regardless of whether it is driving marks or spaces or during transitions. LXT335 provides programmable pulse amplitude output voltages.

If MODE is asserted High, the LXT335 is configured for matched line driver applications. In conjunction with external series resistors a well controlled driver output impedance provides excellent transmit return loss exceeding ETSI ETS300166 and Swiss PTT recommendations. If MODE is asserted Low, the LXT335 is configured for unmatched low power line driver applications where it drives a transformer without series resistors.

Asserting CNTL High and MODE Low, configures the LXT335 for 120 Ω loads. Asserting CNTL High and MODE High configures the LXT335 for 75 Ω loads. In transformer coupled applications the LXT335 produces 2.048 MHz pulses for both 75 Ω coaxial (2.37 V) and 120 Ω shielded twisted-pair (3.0 V) lines. Different transformer and resistor combinations are used for optimum transmit return loss performance. Internal circuitry stabilizes the output pulse amplitudes against supply variations and references them to an on-chip bandgap voltage reference.

Certain applications require common 1:2 transformers for the transmitter and receiver and software switchable 75/120 Ω operation while maintaining return loss in compliance with ETS300166. The LXT335 can be used with 25Ω transmit series resistors for both 75Ω and 120Ω operation (Figure 9).

2.2.1 Driver Failure Monitor

All transceiver incorporate internal Driver Failure Monitors (DFM) in parallel with TTIP and TRING. A capacitor, charged via a measure of the driver output current and discharged by a measure of the maximum allowable current, is used to detect driver failures. Shorted lines draw excess current, overcharging the cap. When the capacitor charge deviates outside the nominal charge window for one of the 4 drivers, the common DFM output pin reports a driver short circuit fail. The individual driver failure monitor output takes precedence and overwrites the transceiver specific LOS output. During a long string of spaces, a short-induced overcharge eventually bleeds off, clearing the DFM flag.

2.2.2 Line Protection

In the receive side, the 1 kΩ series resistors protect the receiver against current surges coupled into the device. Due to the high receiver impedance (40 kΩ typ.) the resistors do not affect the receiver sensitivity. In the transmit side, the Schottky diodes D1-D4 protect the output driver. While not mandatory for normal operation, these protection elements are strongly recommended to improve the design robustness.

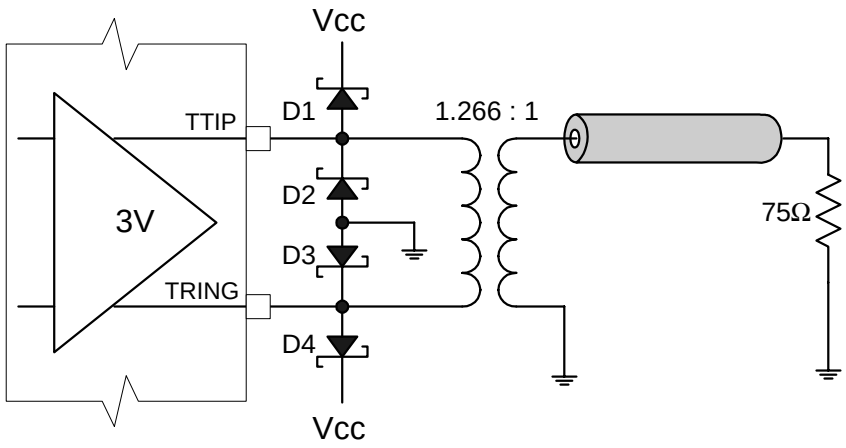
2.3 Diagnostic Mode Of Operation

2.3.1 Loopback

All LOOP*x* pins are identical. If this pin is asserted High, Local Analog Loopback is selected which causes LXT335 to ignore data received on RTIP and RRING and loop data internally from TTIP and TRING back to the receive inputs. If this pin is asserted Low, Remote Loopback is selected which causes LXT335 to ignore data on $\overline{\text{NMARK}}$ and $\overline{\text{PMARK}}$ and to loop internally data received on RTIP and RRING to TTIP and TRING. If this pin is left open or unconnected normal operation mode is selected.

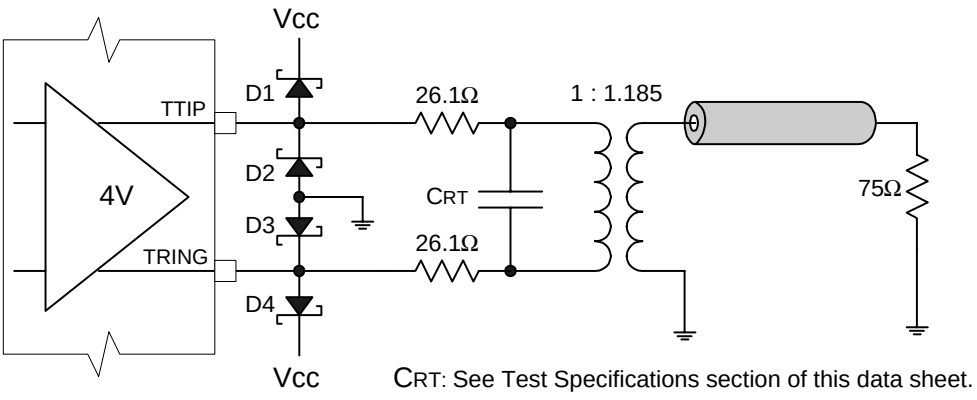
3.0 Application Information

Figure 3. Low Power Transmit Interface for Coax Cables



D1 - D4 = International Rectifier: 11DQ04 or 10BQ060; Motorola: MBR0540T1

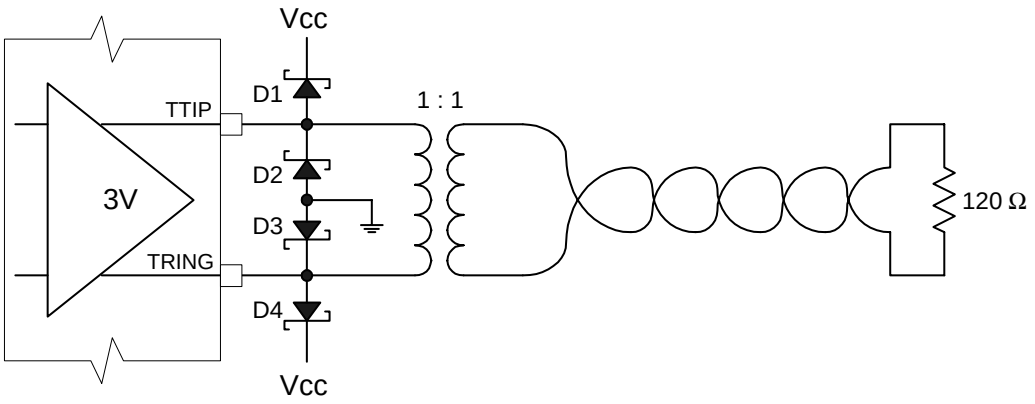
Figure 4. Transmit Interface for Coax Cables



CRT: See Test Specifications section of this data sheet.

D1 - D4 = International Rectifier: 11DQ04 or 10BQ060; Motorola: MBR0540T1.

Figure 5. Low Power Transmit Interface for Twisted Pair Lines



D1 - D4 = International Rectifier: 11DQ04 or 10BQ060; Motorola: MBR0540T1

Figure 6. Transmit Interface for Twisted Pair Lines

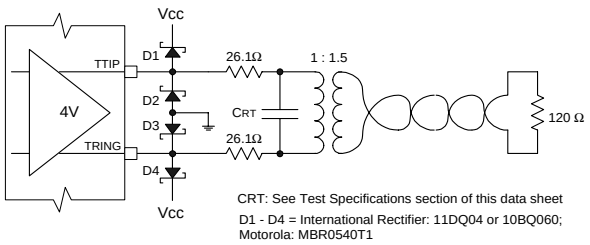


Figure 7. Receive Interface for Twisted Pair Lines

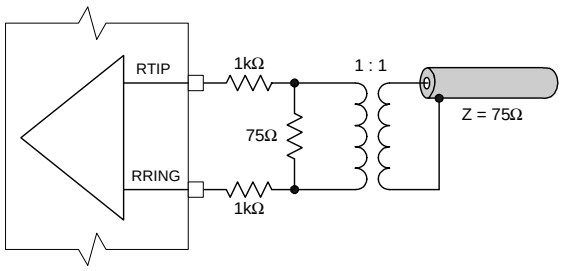


Figure 8. Receive Interface for Twisted-Pair Lines

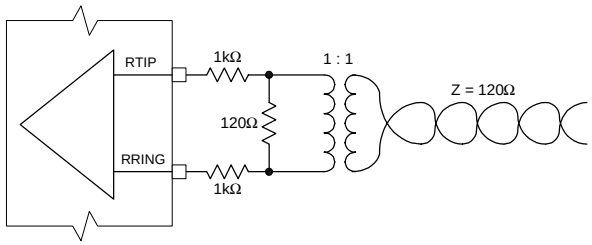


Table 1. Transformer Selection Guide[1]

Manufacturer	Transmit Side		Receive side (1:1 Ratio)
	Part Number	Transformer Turns Ratio	Type
Pulse Engineering	PE-65586	1:1.36	Quad
	PE-65766	1:1.266	Dual
	PE-68789	1:1.5	Dual
	PE-65762	1:1.36	Dual
	PE-65861	1:2	Dual
	PE-65861	1:1	Dual
	PE-68789	1:1.185	Single
	PE-65389	1.266:1	Single
HALO	TG27-1505NX	1:1.36	Octal
	TD64-1205D	1:1.26	Dual
	TG29-1205NX	1:2	Octal
Bel-Fuse	0553-0013	1:1.36	Dual
	5006-1C	1:2	Dual
Schott Corp	67129300	1:2	Single
Valor	ST 5078	1:1.36	Dual
	ST 5028	1:2	Dual

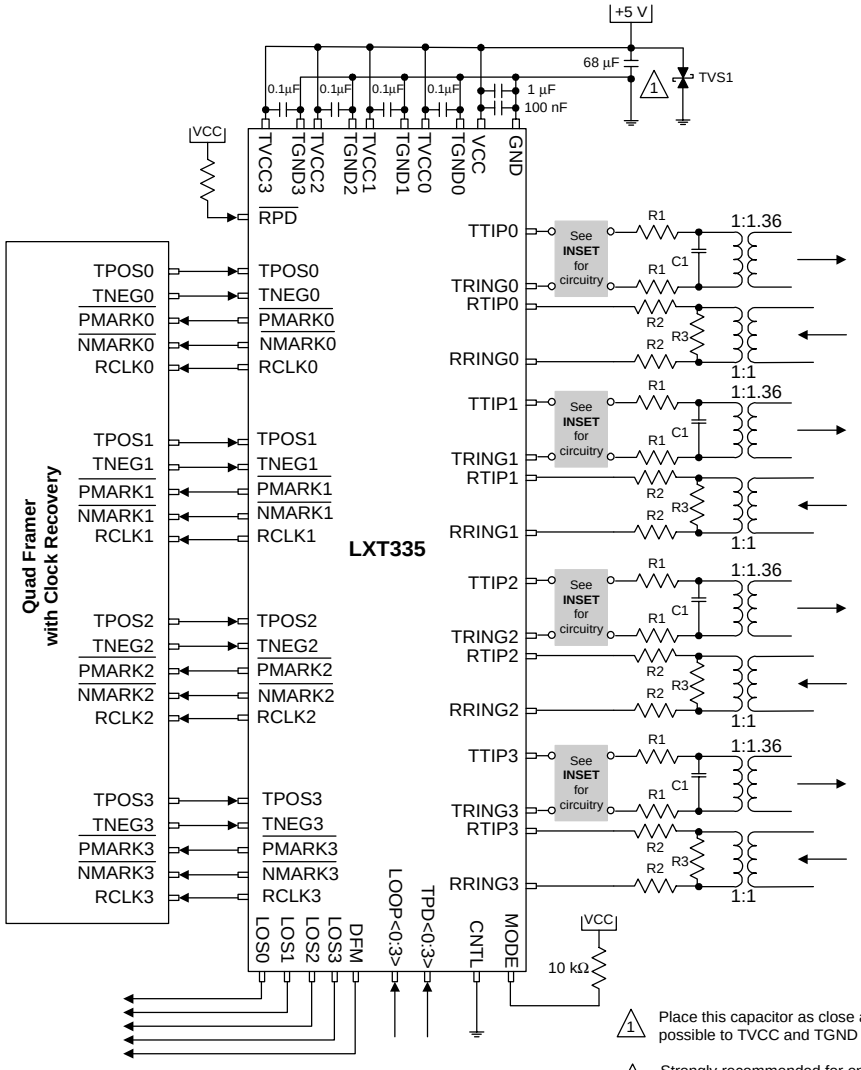
1. As of the publication date, Intel has tested the transformers listed in this table. However, part numbers and specifications change without notice. Design engineers should validate components before committing to their use.

Table 2. Transmit Transformer and Resistor Combinations

Transformer	Resistor	Return Loss[1]	CNTL1	MODE1	Impedance
1.266:1	0 Ω	< 1 dB	Low	Low	75 Ω
1:1	0 Ω	< 1 dB	Low	Low	120 Ω
1:1.185	26.1 Ω	20 dB	Low	High	75 Ω
1:1.5	26.1 Ω	20 dB	Low	High	120 Ω
1:1.36	25 Ω	18 dB	Low	High	75 Ω
1:1.36	25 Ω	18 dB	Low	High	120 Ω
1:2	15 Ω	≥ 8 dB	High	High	75 Ω
1:2	15 Ω	≥ 8 dB	High	Low	120 Ω

1. Typical values 51 kHz - 3.078 MHz

Figure 9. E1 120 Ω and 75 Ω Matched Line Applications



Component	Application	
	120 Ω	75 Ω
R1. Transmit resistor	25 Ω	25 Ω
R2. Receive resistor	1 kΩ	1 kΩ
R3. Receive terminating resistor	120 Ω	75 Ω
C1. Transmit capacitor (typical)	180 pF	180 pF
D1 - D4. Protection diodes (Schottky)	International Rectifier: 11DQ04 or 10BQ060 Motorola: MBR0540T1	
TVS1. Transient Voltage Suppressor	Semtech: SMCJ5.0AC or equivalent	

4.0 Test Specifications

Note: The minimum and maximum values in Table 3 through Table 8 and Figure 10 and Figure 11 are performance specifications of the LXT335 and are guaranteed by test except, where noted, by design.

Table 3. Absolute Maximum Ratings

Parameter	Sym	Min.	Max.	Unit
DC supply voltage	VCC, GND	-0.3	6.0	V
Input voltage on any pin [1]	VIN	GND-0.3	RVCC + 0.3	V
Input voltage on RTIP, RRING	VIN	-6	RVCC + 0.3	V
Transient latchup current on any pin[2]	IIN	–	100	mA
Input current on any digital pin[3]	IIN	-10	10	mA
DC input current on TTIP, TRING[3]	IIN	–	±100	mA
DC input current on RTIP, RRING[3]	Iin	–	±20	mA
Storage temperature	TSTOR	-65	+150	° C
Total package power dissipation	–	–	1	W

Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum ratings conditions for external periods may affect device reliability.

1. Reference to ground.
2. Exceeding these values will cause SCR latchup.
3. Constant input current.

Table 4. Recommended Operating Conditions

Parameter	Sym	Min	Typ	Max	Units	Test Condition
DC supply voltage [1]	VCC	4.75	5.0	5.25	V	
Ambient operating temperature	TA	-40	+25	+85	° C	

1. TVCC must not exceed RVCC BY 0.3 V

Table 5. DC Characteristics (over recommended range)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Digital I/O pins	High-level input voltage	VIH	2.0	–	–	V	
	Low-level input voltage	VIL	—	–	0.8	V	
	High-level output voltage[2]	VOH	3.5	–	–	V	IOUT= -400µA
	Low-level output voltage[2]	VOL	—	–	0.4	V	IOUT= 1.6 mA
Input leakage current (digital input pins)		IIL	-10	–	+10	µA	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Output Drivers will output CMOS logic levels into CMOS loads.
3. 100% 1s density. Power dissipation including device load while driving a matched line over the operating temperature range. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50 pF load.
4. 50% 1s density. Power dissipation including device load while driving a line without matching resistors over the operating temperature range. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50 pF load.
5. Applies to the following pins: 9, 12, 13, 16, 33, 36, 37, 40, 49-54, 59-64.

Table 5. DC Characteristics (over recommended range) (Continued)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Tristate leakage current[5]		IHZ	-10		+10	µA	
Driver short circuit current		–	–	–	50	mA	See Figure 4 and Figure 6
MODE input pins	Low-level input voltage	VINL	–	–	1.5	V	pins 17, 55, 56, 57, 58
	High-level input voltage	VINH	3.5	–	–	V	
	Mid-range input voltage	VINM	2.3	2.5	2.7	V	
	Low-level input current	IINL	–	–	50	µA	
	High-level input current	IINH	–	–	50	µA	
Total power dissipation [3]	75 Ω system (MODE=H)	PD	–	660	750	mW	Figure 4
	120 Ω system (MODE=H)	PD	–	660	750	mW	Figure 6
Total power dissipation[4]	75 Ω system (MODE=L)	PD	–	410	470	mW	Figure 3
	120 Ω system (MODE=L)	PD	–	410	470	mW	Figure 5
Power down current		ICCO	–	–	10	mA	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Output Drivers will output CMOS logic levels into CMOS loads.
3. 100% 1s density. Power dissipation including device load while driving a matched line over the operating temperature range. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50 pF load.
4. 50% 1s density. Power dissipation including device load while driving a line without matching resistors over the operating temperature range. Digital inputs are within 10% of the supply rails and digital outputs are driving a 50 pF load.
5. Applies to the following pins: 9, 12, 13, 16, 33, 36, 37, 40, 49-54, 59-64.

Table 6. Receive Characteristics

Parameter		Sym	Min	Typ	Max	Units	Test Condition
Permissible cable attenuation		–	500	–	–	mV	
		–	–	–	12	dB	@1024 kHz
Receiver dynamic range		DR	0.5	–	4.2	VP	
Signal to noise interference margin[1]		S/I	-15	–	–	dB	per G.703, O.151
Signal to single tone interference margin		S/X	-14	–	–	dB	O.151
$\overline{\text{PMARK}}$ / $\overline{\text{NMARK}}$ output Jitter		–	–	0.01	–	U.I.	peak to peak
Slicer ratio		SRE	43	50	57	%	rel. to peak input voltage
Analog loss of signal threshold		–	22	–	–	dB	
Loss of signal threshold		–	–	1	–	dB	
Receiver input impedance		–	–	40	–	kΩ	@ 1.024 kHz, RTIP to RRING
Input return loss[2]	51 kHz – 102 kHz	–	20	–	–	dB	measured against nominal impedance, Figure 7, Figure 8.
	102 – 2048 kHz	–	20	–	–	dB	
	2048 kHz – 3072 kHz	–	20	–	–	dB	

1. No errors shall occur when the combined signal attenuated by the maximum specified interconnting cable loss is applied to the input port. See ITU O.151 recommendation for further details.
2. Guaranteed by design and other correlation factors.

Table 7. Transmit Timing Characteristics

Parameter	Sym	Min	Typ	Max	Unit	Test Condition
Transmit data rate	–	–	2.048	–	Mbps	
Transmit data tolerance	–	-50	–	50	ppm	
Output pulse width	t_{PW}	–	244	–	ns	

Table 8. Receive Timing Characteristics (See Figure 10)

Parameter	Sym	Min	Typ	Max	Units	Test Condition
$\overline{\text{PMARK}}$/$\overline{\text{NMARK}}$ pulse width	t_{MPW}	200	244	300	ns	
Receiver throughput delay	t_{RXD}	–	65	–	ns	
Receive data rate tolerance	–	–	±80	–	ppm	
Receive data to receive clock delay time	–	–	5	–	ns	

Figure 10. Receive Timing Specifications

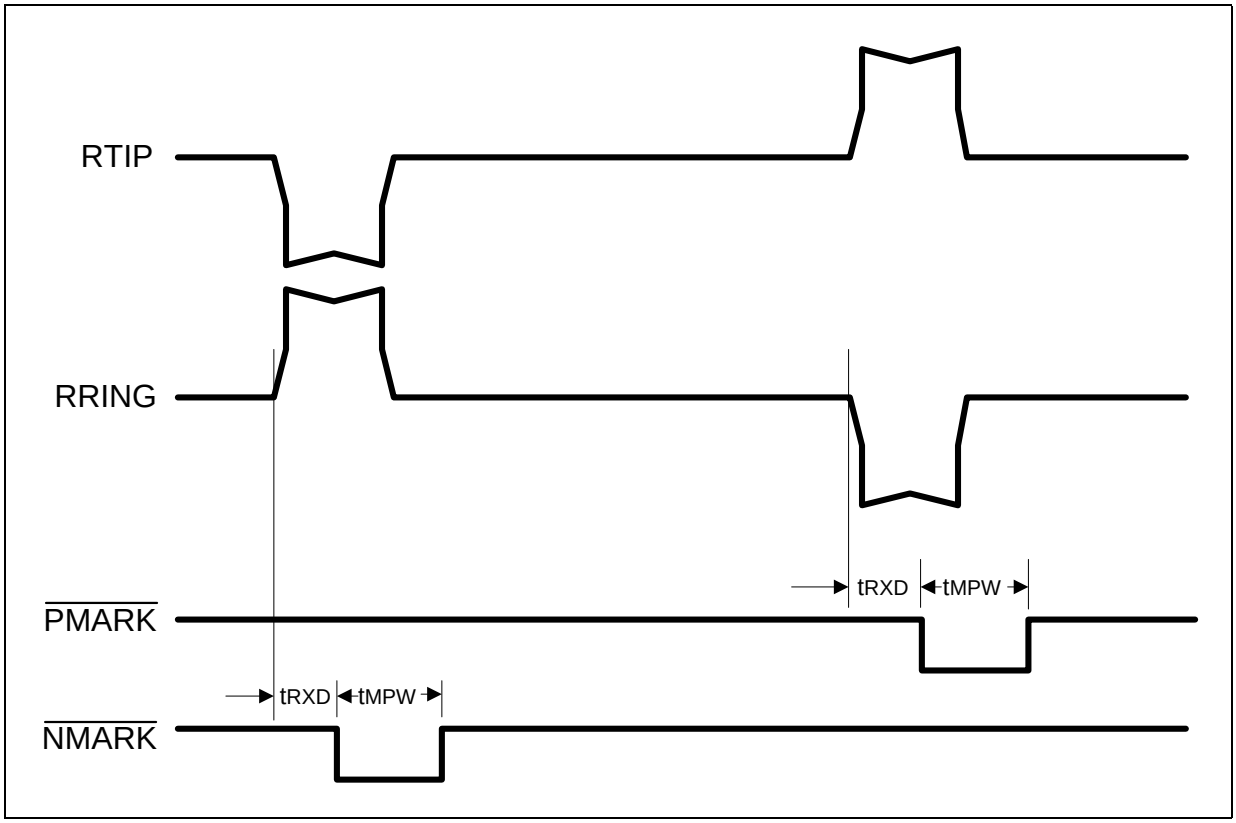
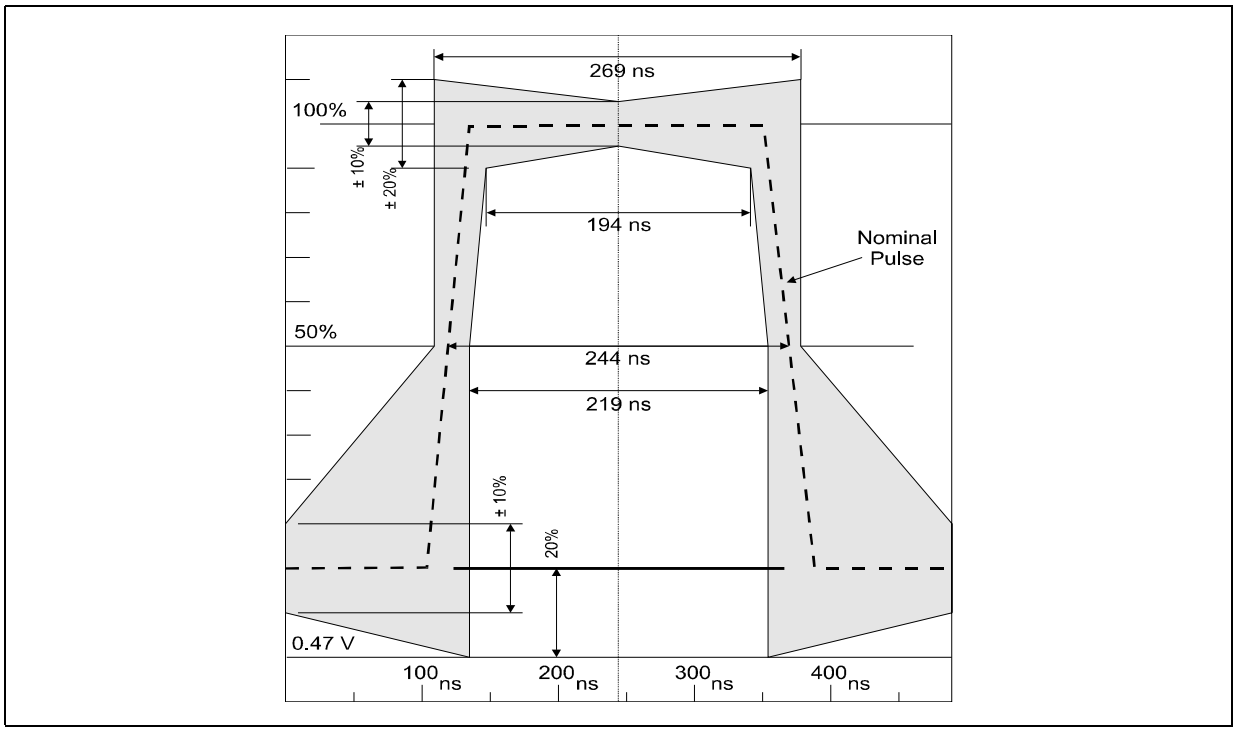
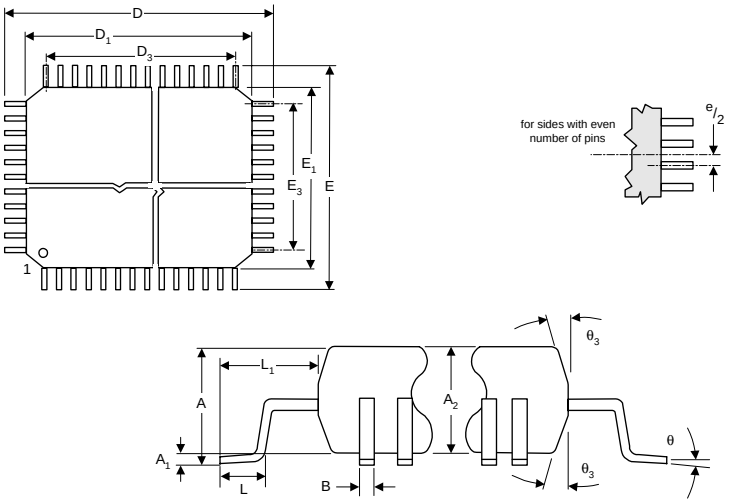


Figure 11. 2.048 MHz Pulse Mask G.703



5.0 Mechanical Specifications

Figure 12. Package Specifications



Ordering Information

- Part Number: LXT335QE
- 64-pin Quad Flat Pack
- Extended Temperature Range -40°C - +85°C

Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	–	0.130	–	3.30
A_1	0.000	0.010	0.00	0.25
A_2	0.100	0.120	2.55	3.05
b	0.012	0.018	0.30	0.45
D	0.695	0.715	17.65	18.15
D_1	0.549	0.553	13.95	14.05
D_3	0.472 REF		12.00 REF	
E	0.695	0.715	17.65	18.15
E_1	0.549	0.553	13.95	14.05
E_3	0.472 REF		12.00 REF	
e	0.031 BSC		0.80 BSC	
L	0.029	0.041	0.73	1.03
L_1	0.077 REF		1.95 REF	
θ_3	5 °	16 °	5 °	16 °
θ	0 °	7 °	0 °	7 °