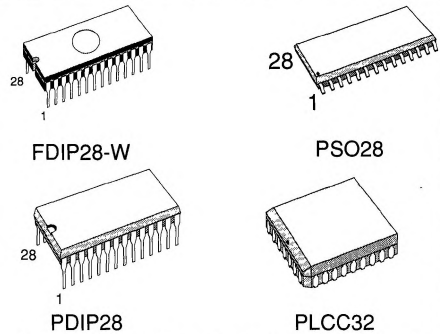
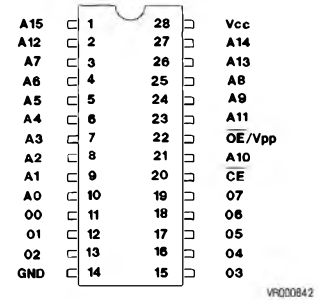
512K CMOS UV EPROM - OTP ROM

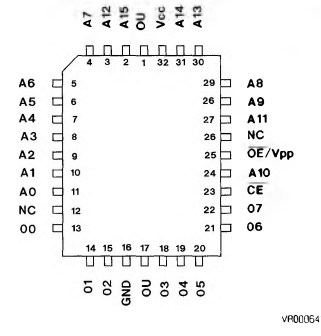
- VERY FAST ACCESS TIME : 100 ns.
- COMPATIBLE WITH HIGH SPEED MICROPROCESSORS, ZERO WAIT STATE.
- LOW POWER "CMOS" CONSUMPTION :
  - Operating current 30mA
  - Stand by current 200µA.
- PROGRAMMING VOLTAGE 12.75V.
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING.
- PROGRAMMING TIMES OF AROUND 6 SECONDS (PRESTO IIB ALGORITHM).



(Ordering information at the end of the datasheet)

Figure 1 : Pin Connection





DESCRIPTION

The M27C512 is a high speed 524,288 bit ultraviolet erasable and reprogrammable EPROM ideally suited for applications where fast turnaround and pattern experimentation are important requirements.

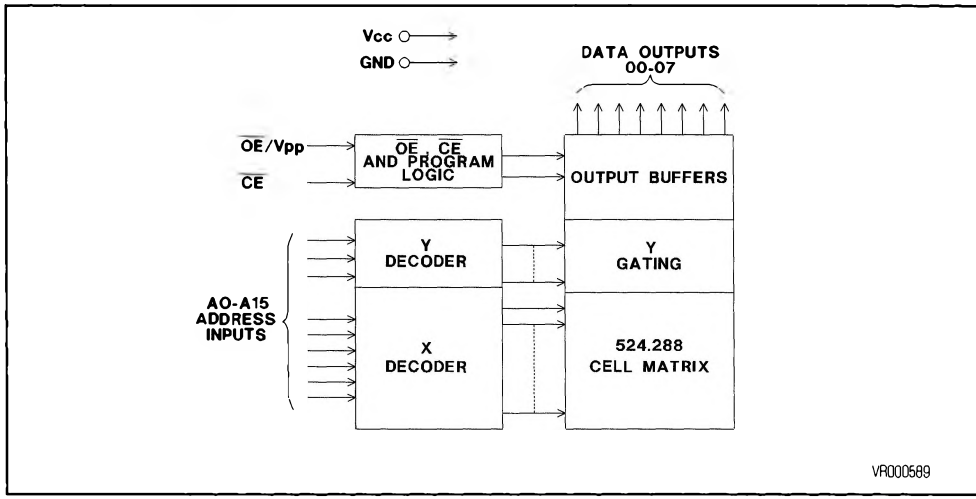
It is housed in a 28 pin Ceramic Frit Seal Window package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

In order to meet production requirements (cost effective solution or SMD), this product is also offered in plastic packages, either Plastic DIP, SO or PLCC, for One Time Programming only.

PIN FUNCTIONS

A0-A15	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$ / V_{PP}	OUTPUT ENABLE / V_{PP}
O0-O7	DATA INPUT/OUTPUT
V_{CC}	+ 5V POWER SUPPLY
GND	GROUND
DU	DON'T USE
NC	NO CONNECTION

Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Input or Output voltages with respect to ground	-0.6 to +7.0	V
V_{PP}	Supply voltage with respect to ground	-0.6 to +14.0	V
V_{A9}	Voltage on A9 with respect to ground	-0.6 to +13.5	V
V_{CC}	Supply voltage with respect to ground	-0.6 to +7.0	V
T_{bias}	Temperature range under bias	-50 to +125	°C
T_{stg}	Storage temperature range	-65 to +150	°C

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE	$\overline{CE}$	$\overline{OE}$ / V_{PP}	A9	OUTPUT
READ	L	L	X	D_{OUT}
OUTPUT DISABLE	L	H	X	HIGH Z
STANDBY	H	X	X	HIGH Z
PROGRAM	L	V_{PP}	X	DIN
PROGRAM INHIBIT	H	V_{PP}	X	HIGH Z
ELECTRONIC SIGNATURE	L	L	V_H	CODE

NOTE : X = Don't care ; V_H = 12V ± 0.5V ; H = High ; L = Low.

READ OPERATION

DC AND AC CONDITIONS

SELECTION CODE	F1	F6	F7	F3
Operating Temperature Range	0 to 70°C	-40 to 85°C	-40 to 105°C	-40 to 125°C
SELECTION CODE (Example for 0°C to 70°C Oper. Temp. Range)	**-10XF1, 12XF1, 15XF1, 20XF1, 25XF1**		**12F1,15F1,20F1, 25F1**	
V_{CC} Power Supply	5V ± 5%		5V ± 10%	

DC AND OPERATIONG CHARACTERISTICS (F1 AND F6 DEVICES)

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}	-10	10	µA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL} I_{OUT}= 0 mA (F = 5MHz)		30	mA
I_{CC2}	V_{CC} Standby Current - TTL	$\overline{CE}$ = V_{IH}		1	mA
I_{CC3} (4)	V_{CC} Standby Current - CMOS	$\overline{CE}$ > V_{CC} - 0.2V		200	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input Low Voltage		-0.3	+0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+1.0	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA I_{OH} = -100 µA	2.4 V_{CC}-0.7		V

AC CHARACTERISTICS

Symbol	Parameter	Test Condition	27C512										Unit
			-10		-12		-15		-20		-25		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		100		120		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		100		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		40		50		60		70		100	ns
t_{DF} (2)	$\overline{OE}$ High to Output Float	$\overline{CE}$ = V_{IL}	0	30	0	40	0	50	0	60	0	60	ns
t_{OH}	Output Hold from Address	$\overline{CE}$= $\overline{OE}$=V_{IL}	0		0		0		0		0		ns

CAPACITANCE(3)

(T_A = 25°C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	12	pF

NOTES : 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100 % tested. Output Float is defined as the point where data is no longer driven (see timing diagram).
3. This parameter is only sampled and not 100 % tested.
4. From date code 9112.

AC TEST CONDITIONS

Input Rise and Fall Times	:	≤ 20 ns	Timing Measurement Reference Levels :	
Input Pulse Levels	:	0.45 to 2.4V	Inputs : 0.8 and 2V - Outputs : 0.8 and 2V	

Figure 3 : AC Testing Input/Output Waveform

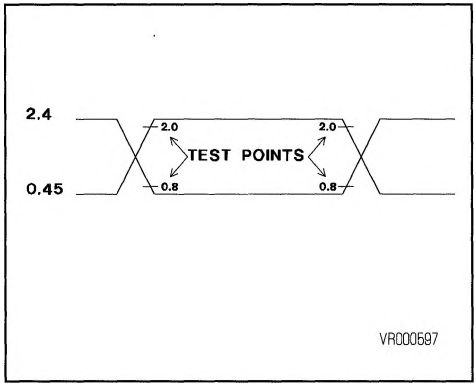


Figure 4 : AC Testing Load Circuit

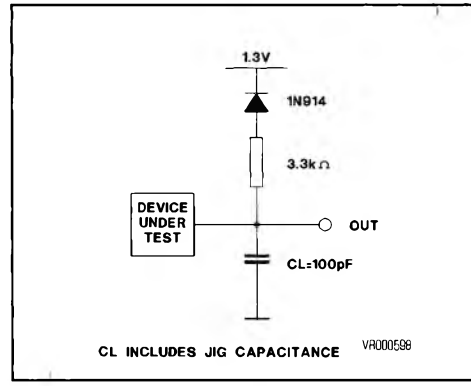
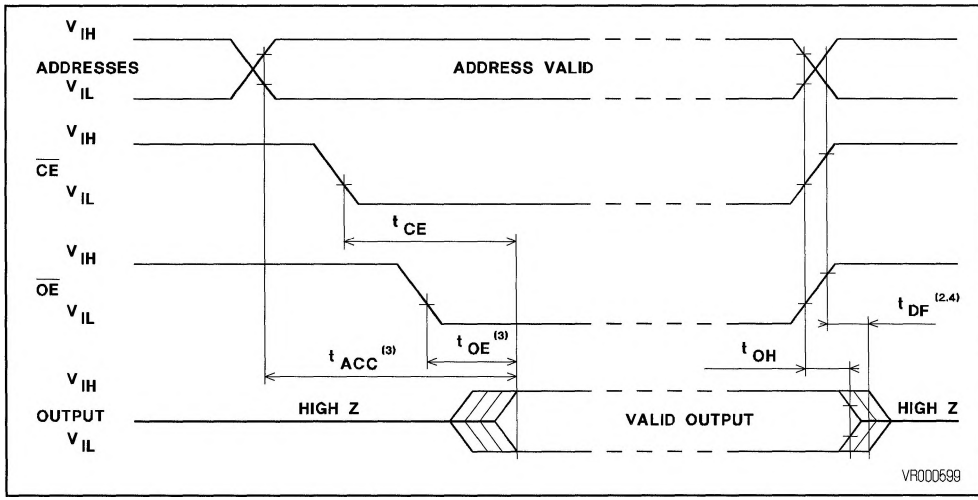


Figure 5 : AC Waveforms



NOTES : 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100 % tested.
3. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The modes of operations of the M27C512 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for OE/V_{PP} and 12V on A9 for Electronic Signature.

READ MODE

The M27C512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and the addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27C512 has a standby mode which reduces the active current from 30mA to 0.2mA (from date code 9104). The M27C512 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}/V_{PP}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of CMOS-E4 EPROMs require careful decoupling of the devices. The supply current, Icc, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1µF ceramic capacitor be used on every device between Vcc and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between Vcc and GND for every eight devices. The bulk capacitor should be located near the power supplyconnection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution : exceeding 14V on OE/Vpp pin will permanently damage the M27C512.

When delivered (and after each erasure for UV EPROM), all bits of the M27C512 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The M27C512 is in the programming mode when V_{PP} input is at 12.75V and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. The M27C512 can use PRESTO IIB Programming Algorithm that drastically reduces the programming time (typically less than 6 seconds). Nevertheless to achieve compatibility with all programming equipments, PRESTO Programming Algorithm can be used as well.

PRESTO IIB PROGRAMMING ALGORITHM

PRESTO IIB Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of less than 6 seconds. This can be achieved with SGS-THOMSON M27C512 due to several design innovations described in the M27C512 datasheet to improve programming efficiency and to provide adequate margin for reliability. Before starting the programming the internal MARGIN MODE circuit is set in order to guarantee that each cell is pro-

grammed with enough margin. Then a sequence of 100 microsecond program pulses are applied to each byte until a correct verify occurs. No overprogram pulses are applied since the verify in MARGIN MODE provides the necessary margin.

PROGRAM INHIBIT

Programming of multiple M27C512s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs including $\overline{OE}/V_{PP}$ of the parallel M27C512 may be common. A TTL low level pulse applied to a M27C512's $\overline{CE}$ input, with $\overline{OE}/V_{PP}$ at 12.75V, will program that M27C512. A high level $\overline{CE}$ input inhibits the other M27C512s from being programmed. V_{CC} is specified to be 6.25V ± 0.25V.

PROGRAM VERIFY

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ at V_{IL}. Data should be verified with t_{DV} after the following edge of $\overline{CE}$.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C512. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C512. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) the device identifier code. For the SGS-THOMSON M27C512, these two identifier bytes are given here below, and can be read-out on outputs O0 to O7.

ERASURE OPERATION (applies for UV EPROM)

The erasure characteristics of the M27C512 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C512 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C512 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C512 window to prevent unintentional erasure. The recommended erasure procedure for the M27C512 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27C512 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

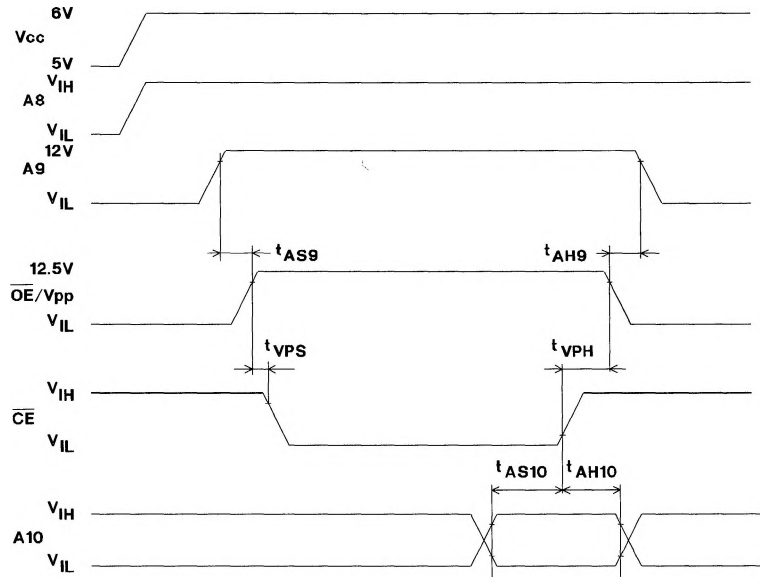
ELECTRONIC SIGNATURE MODE

IDENTIFIER	PINS									
	A0	O7	O6	O5	O4	O3	O2	01	O0	Hex
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	0	0	1	1	1	1	0	1	3D

NOTE : A9 = 12V ± 0.5V ; $\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL} ; A1 to A8 = A10 to A15 = V_{IL}

DEVICE OPERATION (Continued)

Figure 6 : MARGIN MODE Set and Reset Waveforms



NOTES: 1. Other addresses are don't care.
2. Set MARGIN MODE A10 = V_{IH}, Reset MARGIN MODE A10 = V_{IL}.

MARGIN MODE AC CHARACTERISTICS

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
t_{AS10}	A10 Setup Time		1		µs
t_{AH10}	A10 Hold Time		1		µs
t_{VPH}	V_{PP} Hold Time		2		µs
t_{VPS}	V_{PP} Setup Time		2		µs
t_{AS9}	A9 Setup Time		2		µs
t_{AH9}	A9 Hold Time		2		µs

PROGRAMMING OPERATION

(T_A = 25°C ± 5°C, V_{CC} [1] = 6.25V ± 0.25V, V_{PP} [1] = 12.75V ± 0.25V)

DC AND OPERATING CHARACTERISTICS

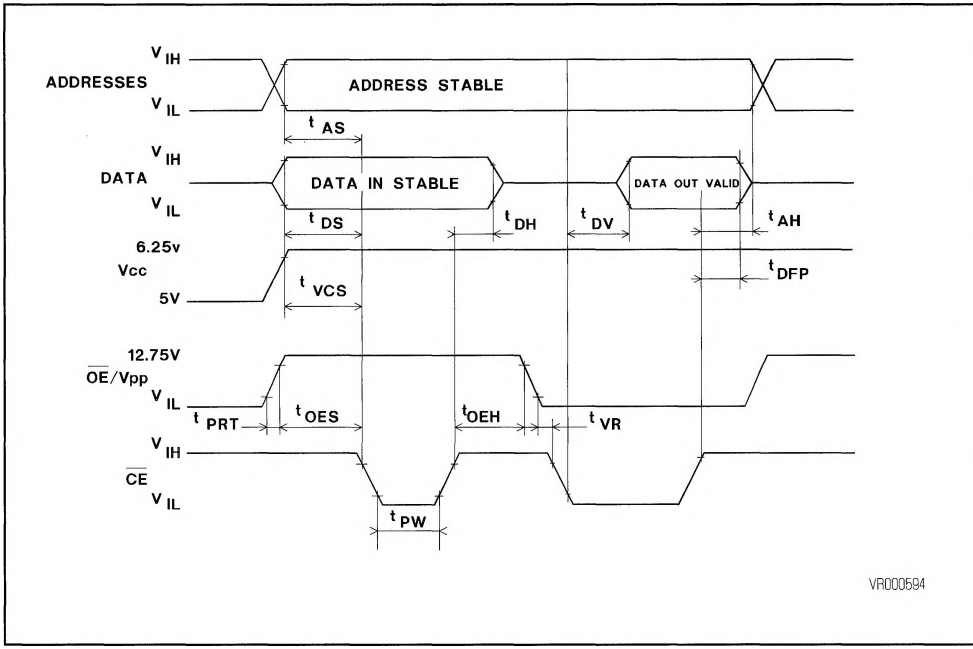
Symbol	Parameter	Test Condition (see Note 1)	Values		Unit
			Min	Max.	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10	µA
V_{IL}	Input Low Level (All Inputs)		-0.1	0.8	V
V_{IH}	Input High Level		2.4	V_{CC}+0.5	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = - 400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current			50	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$		50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5	12.5	V

AC CHARACTERISTICS

Symbol	Parameter	Test Condition (see Note 1)	Values		Unit
			Min	Max	
t_{AS}	Address Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP} [2]	Chip Enable Output Float Delay		0	130	ns
t_{VCS}	V_{CC} Setup Time		0		µs
t_{PW}	$\overline{CE}$ Initial Program Pulse Width		95	105	µs
t_{DV}	Data Valid from $\overline{CE}$			1	ns
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2		µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

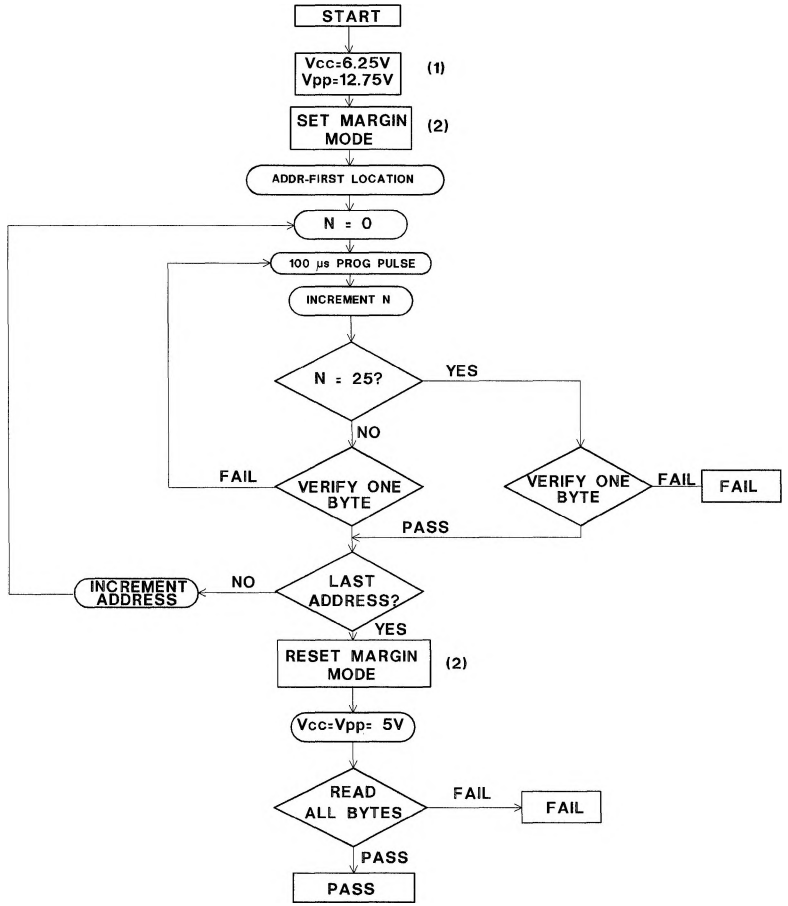
NOTES : 1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and not 100 % tested.
Output Float is defined as the point where data is no longer driven (see timing diagram).

Figure 7 : Programming Waveforms



NOTES : 1. The input timing reference level is 0.8V for a V_{IL} and 2V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

Figure 8 : PRESTO IIB Programming Algorithm Flow Chart



VR000465

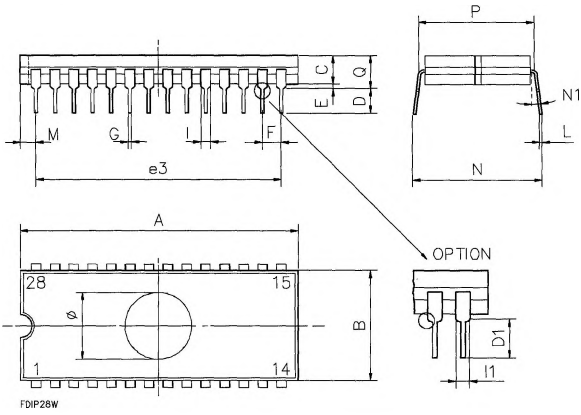
ORDERING INFORMATION (UV EPROM)

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27C512-10XF1	100 ns	5V ± 5%	0°C to +70°C	FDIP28-W
M27C512-12XF1	120 ns	5V ± 5%	0°C to +70°C	FDIP28-W
M27C512-15XF1	150 ns	5V ± 5%	0°C to +70°C	FDIP28-W
M27C512-20XF1	200 ns	5V ± 5%	0°C to +70°C	FDIP28-W
M27C512-25XF1	250 ns	5V ± 5%	0°C to +70°C	FDIP28-W
M27C512-12F1	120 ns	5V ± 10%	0°C to +70°C	FDIP28-W
M27C512-15F1	150 ns	5V ± 10%	0°C to +70°C	FDIP28-W
M27C512-20F1	200 ns	5V ± 10%	0°C to +70°C	FDIP28-W
M27C512-25F1	250 ns	5V ± 10%	0°C to +70°C	FDIP28-W
M27C512-15XF6	150 ns	5V ± 5%	-40°C to +85°C	FDIP28-W
M27C512-15XF7	150 ns	5V ± 5%	-40°C to +105°C	FDIP28-W
M27C512-15XF3	150 ns	5V ± 5%	-40°C to +125°C	FDIP28-W

NOTE : Consult your nearest SGS-THOMSON sales office for availability of other combinations.

PACKAGE MECHANICAL DATA - UV EPROM

Figure 9 : 28-PIN WINDOW CERAMIC DUAL IN LINE FRIT-SEAL



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			38.10			1.500
B	13.05		13.36	0.514		0.526
C	3.90		5.08	0.154		0.199
D	3.00			0.118		
E	0.50		1.78	0.020		0.070
e 3		33.02			1.300	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.027
I	1.17		1.42	0.046		0.056
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N						
N1	0°		10°	0°		10°
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	7.35		7.90	0.290		0.311

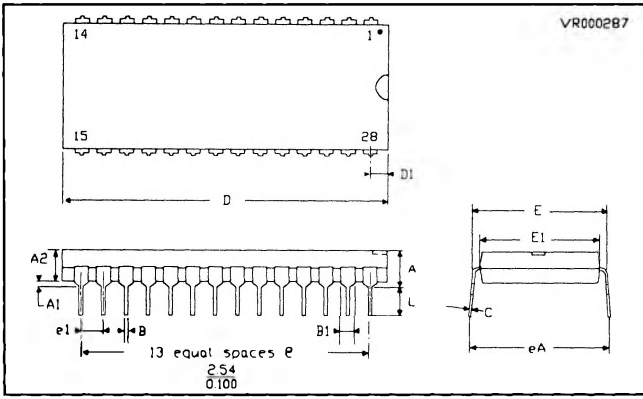
ORDERING INFORMATION (OTP ROM)

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27C512-15XB1	150 ns	5V ± 5%	0°C to +70°C	PDIP28
M27C512-20B1	200 ns	5V ± 10%	0°C to +70°C	PDIP28
M27C512-15XB6	150 ns	5V ± 5%	-40°C to +85°C	PDIP28
M27C512-15XC1	150 ns	5V ± 5%	0°C to +70°C	PLCC32
M27C512-20C1	200 ns	5V ± 10%	0°C to +70°C	PLCC32
M27C512-15XC6	150 ns	5V ± 5%	-40°C to +85°C	PLCC32
M27C512-15XM1	150 ns	5V ± 5%	0°C to +70°C	SO28
M27C512-20M1	200 ns	5V ± 10%	0°C to +70°C	SO28

NOTE : Consult your nearest SGS-THOMSON sales office for availability of other combinations.

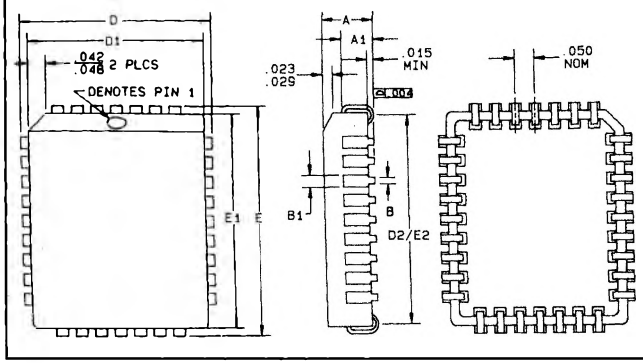
PACKAGE MECHANICAL DATA - OTP ROM

Figure 10 : 28-PIN PLASTIC DIP



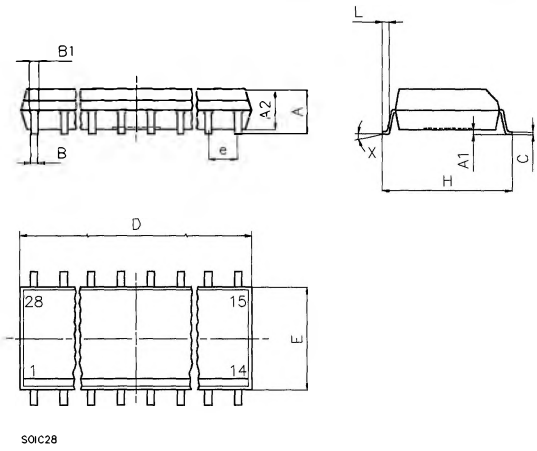
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1		0.63			.025	
B		0.45			.018	
b1	0.23		0.31	.009		.012
b2		1.27			.050	
C						
D			37.34			1.470
E	15.20		16.68	.598		.657
e		2.54			.100	
e 3		33.02			1.300	
e 4						
F			14.10			.555
I		4.45			.175	
L		3.30			.130	
K1						
K2						

Figure 11 : 32-LEAD PLASTIC LEADED CHIP CARRIER



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	3.04	3.55	3.55	.120	.120	.140
A1	1.96	2.41	2.41	.078	.078	.095
B	0.33	0.53	0.53	.013	.013	.021
B1	0.66	0.81	0.81	.026	.026	.032
D	12.31	12.57	12.57	.485	.485	.495
D1	11.35	11.50	11.50	.447	.447	.453
D2	9.90	10.92	10.92	.390	.390	.430
E	14.85	15.11	15.11	.585	.585	.595
E1	13.89	14.04	14.04	.547	.547	.553
E2	12.44	13.46	13.46	.490	.490	.530

Figure 12 : SOIC28-28-LEAD SMALL OUTLINE PACKAGE



SOIC28

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.05			.120
A1	0.05		0.35	.002		.013
A2	2.34		2.69	.092		.105
B	0.35		0.51	.013		.020
B1	0.35		0.61	.013		.024
C	0.15		0.32	.006		.012
D	17.71		18.49	.697		.727
E	8.23		8.89	.324		.350
e		1.27			.050	
H	11.51		12.70	.453		.500
L	0.41		1.27	.016		.050
X		8°				8°