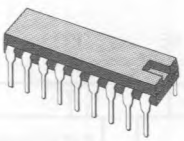
# PULSE DIALER

- OPERATION FROM 1.5V TO 5.5 SUPPLY
- STATIC STANDBY OPERATION DOWN TO 1V
- LOW CURRENT CONSUMPTION : 100uA, 1.5V
- LOW STATIC STANDBY CURRENT : MAX 500nA
- LAST NUMBER REDIAL FUNCTION
- 32 DIGIT CAPACITY, INCLUDING ACCESS PAUSES
- ON-CHIP RC OSCILLATOR USING THREE EXTERNAL COMPONENTS
- DIALING RATE CAN BE VARIED BY CHANGING THE DIAL RATE OSCILLATOR FREQUENCY
- DIALING PULSE MARK/SPACE RATIO SELECTABLE : 1.5 : 1 OR 2 : 1
- CIRCUIT RESET FOR LINE POWER BREAKS > 220ms
- ACCESS PAUSE GENERATION VIA THE KEYBOARD
- ACCESS PAUSE RESET VIA THE KEYBOARD



**DIP18**
(0,25mm)

**ORDER CODE :** M3561B

**PIN CONNECTION**


M89M3561-01

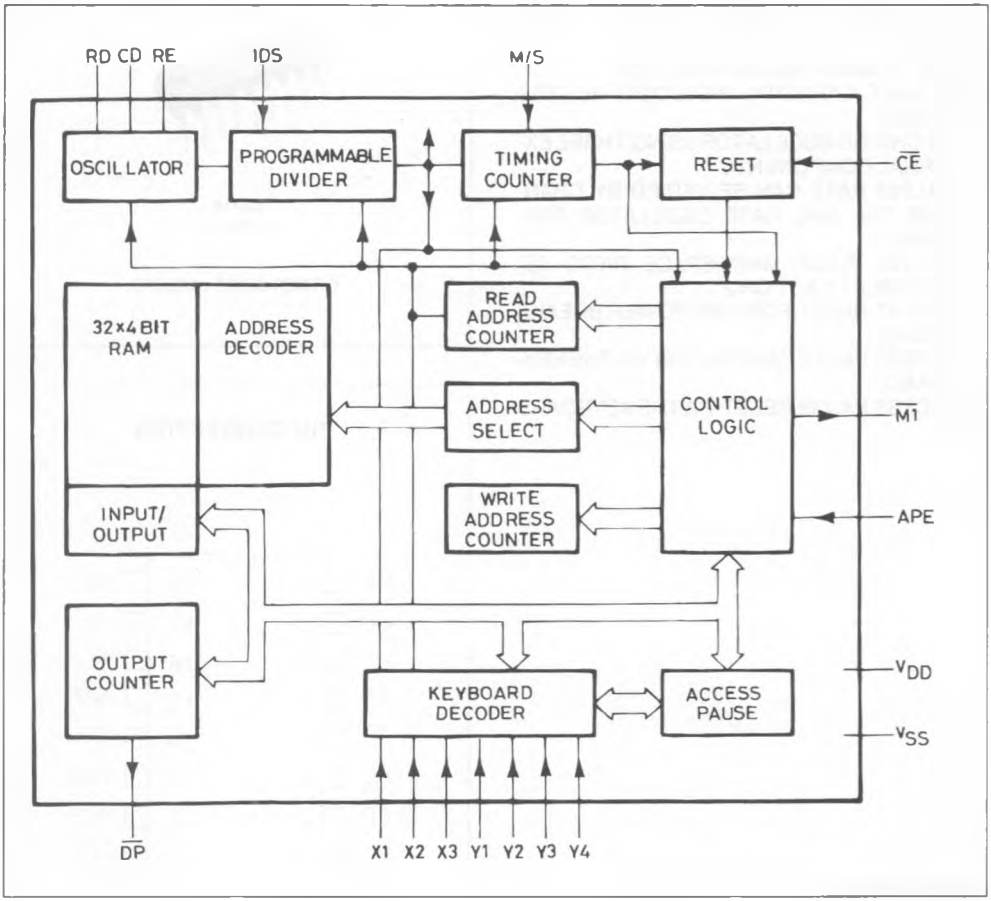
## DESCRIPTION

The M3561 is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert push button keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 push button matrix. Numbers with up to 32 digits can be retained in a RAM for redial. Access pause can be stored via the keyboard.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage | + 7 | V |
| $V_{IN}$ | Voltage on any Pin | ($V_{SS}$ – 0.3) to ($V_{DD}$ + 0.3) | V |
| $T_{OP}$ | Operating Temperature | (– 25 to + 70) | °C |
| $T_{ST}$ | Storage Temperature | (– 65 to + 150) | °C |

## BLOCK DIAGRAM



## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = 2.5V ; $V_{SS}$ = 0V ; $f_{OSC}$ = 2.4KHz ; $T_{amb}$ = – 25°C to + 70°C, unless otherwise specified)

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{DD}$ | Operating Supply Voltage | | 1.5 | | 5.5 | V |
| $V_{DR}$ | Data Retention Voltage | $\overline{CE} = V_{DD}$ | 1 | | | V |
| $I_{DD}$ | Operating Supply Current | $\overline{CE} = V_{SS}$ ; $V_{DD}$ = 1.5 V<br>$\overline{CE} = V_{SS}$ ; $V_{DD}$ = 5.5 V<br>$T_{amb}$ = 25 °C | | | 100<br>500 | µA<br>µA |
| $I_{DDO}$ | Standby Supply Current | $\overline{CE} = V_{DD}$ ; $V_{DD}$ = 1.5 V<br>M/S = $V_{DD}$ ;<br>IDS = APE = $V_{SS}$ | | | 500 | nA |
| $V_{IL}$ | Input Voltage Low | 1.5 V ≤ $V_{DD}$ ≤ 5.5 V | $V_{SS}$ – 0.3 V | | 20 % of $V_{DD}$ | |
| $V_{IH}$ | Input Voltage High | 1.5 V ≤ $V_{DD}$ ≤ 5.5 V | 80 % of $V_{DD}$ | | $V_{DD}$ + 0.3 V | |
| – $I_{IL}$<br>$I_{IH}$ | Input Leakage Current $\overline{CE}$ Low<br>$\overline{CE}$ High | $\overline{CE} = V_{SS}$<br>$\overline{CE} = V_{DD}$ | | | 100<br>100 | nA<br>nA |
| – $I_{IL}$ | Pull-up Input Current M/S | $V_I = V_{SS}$ | 0.4 | | 4 | µA |
| $R_{KON}$ | Keyboard "ON" Resistance | Contact ON | | | 1 | kΩ |
| $R_{KOFF}$ | Keyboard "OFF" Resistance | Contact OFF | 1 | | | MΩ |
| $I_{IH}$ | Input Current for Xn, "ON" | $V_I = V_{DD}$ | | | 30 | µA |
| $I_{IH}$ | Input Current for Yn, "ON" | $V_I = V_{DD}$ | | | 30 | µA |
| – $I_{IL}$ | Input Current for Xn "OFF" | $V_I = V_{SS}$ | | | 220 | µA |
| – $I_{IL}$ | Input Current for Yn "OFF" | $V_I = V_{SS}$ | | | 220 | µA |
| $I_{OL}$ | Outputs $\overline{M1}$, $\overline{DP}$ : Sink Current | $V_{OL}$ = 0.5 V | 1 | 6 | | mA |
| – $I_{OH}$ | Source Current | $V_{OH}$ = 2.0 V | 1 | 6 | | mA |
| f | Oscillator Frequency | $V_{DD}$ = 1.5 V | | | 10 | KHz |
| Δf | Frequency Deviation (%)<br>$\Delta f = \frac{\lvert f(1.5\ V) - f(3.5\ V)\rvert}{f(2.5\ V)}$ | 1.5 V ≤ $V_{DD}$ ≤ 3.5 V<br>fixed $R_C$ Oscillator<br>Components :<br>$R_d$ = 715 kΩ<br>$R_e$ = 750 kΩ<br>C1 = 270 pF<br>$T_{amb}$ – 25 °C | | | 4 | % |

## TIMING CHARACTERISTICS

($V_{DD}$ = 1.5 to 5.5V ; $V_{SS}$ = 0 ; fosc = 2.4KHz ; $T_{amb}$ = 25°C)

| Symbol | Parameter | | Test Conditions | Value | Unit |
|---|---|---|---|---|---|
| $f_{CL}$ | Clock Pulse Frequency | 30 x $f_{DP}$ | | 300 | Hz |
| $f_{DP}$ | Dialing Pulse Frequency | $1/T_{DP}$ | IDS = $V_{SS}$ | 10 | Hz |
| $t_m$<br>$t_m$ | Make Time | 2/5 x $T_{DP}$<br>1/3 x $T_{DP}$ | M/S = $V_{DD}$<br>M/S = $V_{SS}$ | 40<br>33.3 | ms<br>ms |
| $t_b$<br>$t_b$ | Break Time | 3/5 x $T_{DP}$<br>2/3 x $T_{DP}$ | M/S = $V_{DD}$<br>M/S = $V_{SS}$ | 60<br>66.6 | ms<br>ms |
| $t_{id}$ | Inter Digit Pause | 8 x $T_{DP}$ | IDS = $V_{SS}$ | 800 | ms |
| $t_{pd}$ | Pre Digit Pause | 8.4 x $T_{DP}$ | IDS = $V_{SS}$ | 840 | ms |
| $t_{rd}$ | Reset Delay Time | | | 223 | ms |
| $t_{e\ min}$<br>$t_{e\ max}$ | Debounce Time | Min.<br>Max. | | 13.3<br>16.7 | ms<br>ms |
| $t_{en\ max}$ | Clock Enable Time | | | 1 | ms |
| $t_{ON\ max}$ | Clock Start-up Time | | | 1 | ms |
| $t_{i\ typ}$ | Initial Data Entry Time | $t_{ON} + t_e$ | | 16 | ms |

## GENERAL DESCRIPTION

### 1. Pin Description

Y4 ; Y3 ; Y2 ; Y1 (pins 1 through 4)

Row keyboard input pins

$\overline{CE}$ (pin 5)

Chip Enable input pin. It is used to initialize the system, to select between the operational mode and the static standby mode, to handle line power breaks.

RE ; CD ; RD (pins 6 through 8)

Oscillator pins. These pins are used to connect external resistors RD, RE and capacitor CD to form a R-C oscillator that generates the time base for the Key Pulser. The output dialing rate and IDP are derived from this time base.

$\overline{DP}$ (pin 9)

Dial Pulse output pin. This signal is provided to drive the external line switching transistor or relay. The output will be "low" during "space" and "high" otherwise.

VSS (pin 10)

Negative supply input pin.

$\overline{M1}$ (pin 11)

Mute output pin. This signal can be used to mute the receiver during the dialling sequence.

M/S (pin 12)

Mark/Space selection input pin. This pin controls the mark to space ratio of the line pulses :

M/S = VSS (33.3/66.6) ; M/S = VDD (40/60).

M/S has an internal pull-up resistor.

VDD (pin 13)

Positive Supply input pin.

IDS (pin 14)

This pin must be connected to Vss.

APE (pin 15)

This pin must be connected to Vss.

X1 ; X2 ; X3 (pins 16 through 18)

Column keyboard input pins.

**Table1 :** Table for selecting oscillator component values for desired dialing rates and inter-digit pauses.

| Osci. Freq. [KHz] | RD kΩ | RE kΩ | CD [pF] | Dial Rate (pps) IDS = $V_{SS}$ | IDP (ms) IDS = $V_{SS}$ |
|---|---|---|---|---|---|
| 1.32 | Select component in the ranges indicated in table of electrical specificatiion | | | 5.5 | 1454 |
| 1.44 | | | | 6 | 1334 |
| 1.56 | | | | 6.5 | 1230 |
| 1.68 | | | | 7 | 1142 |
| 1.80 | | | | 7.5 | 1066 |
| 1.92 | | | | 8 | 1000 |
| 2.04 | | | | 8.5 | 942 |
| 2.16 | | | | 9 | 888 |
| 2.28 | | | | 9.5 | 842 |
| 2.40 | 715 | 750 | 270 | 10 | 800 |
| f | | | | f/0.24 | 1920/f |

**Table 2 :** Input Pin Selection.

| Function | Pin | Input Level | Selection |
|---|---|---|---|
| Mark/space Ratio | M/S | $V_{SS}$<br>$V_{DD}$ | 1 : 2<br>1 : 1.5 |
| Chip Enable | $\overline{CE}$ | $V_{SS}$<br>$V_{DD}$ | Off-hook<br>On-hook |

### 2. Clock Oscillator

This device contains an oscillator circuit that requires three external components : two resistors (RD and RE) and one capacitor (CD). All internal timing is derived from this master time base. To eliminate clock interference in the talk state, the oscillator is only enabled during key closures and during the dialing state. It is disabled at all other times, including the "on hook" condition. For a dialing rate of 10 pps, the oscillator should be adjusted to 2400Hz. Typical values of external components for this are RD = 715Kohm and RE = 750Kohm and CD = 270pF.

It is recommended that the tolerance of resistors be 1%, and that of the capacitor be 5%, to insure a ± 10% tolerance of the dialing rate in the system.

### 3. Chip Enable ($\overline{CE}$)

The $\overline{CE}$ input is used to initialize the chip system.

$\overline{CE}$ = High provides the static standby condition. In this mode, the clock oscillator is off, and internal registers are clamped in reset, with the exception of WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When $\overline{CE}$ = Low, the clock oscillator is again off but the internal registers are enabled and data can be entered from the keyboard. After the first keyboard entry the clock oscillator starts.

If the $\overline{CE}$ input is taken to a High level for more than the time trd (see figures 3 and 4 and timing data), an internal reset pulse will be generated at the end of the trd period. The system is then is the static standby mode.

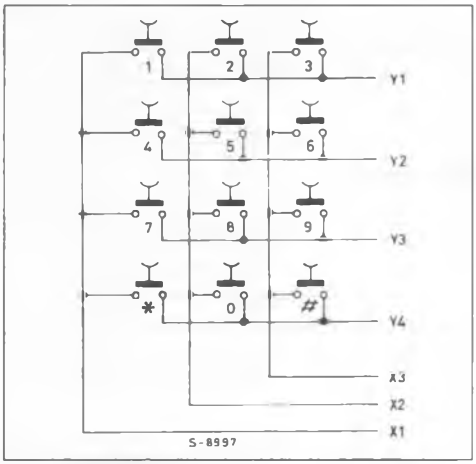
Short $\overline{CE}$ pulses of < trd will not affect the operation of the circuit. No reset pulses are then produced.

### 4. Debouncing Keyboard Entries

The column keyboard inputs to the integrated circuit (Xn) and the row keyboard inputs (Yn) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact), as shown in fig. 1, or to a double contact keyboard with a common connected to VDD (see figure 2). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input, or when one column input and one row input are set High. Any other input combinations will be judged to not be valid and will not be accepted.

Valid inputs are debounced on to the leading and trailing edges, as shown in figure 3 : Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for four or five clock pulse periods (entry period te). The next keyboard entry will not be accepted until the previously closed contact has been open for three or four clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the trailing edge of the first clock pulse after the entry.

**Figure 1 :** Single Contact Keyboard.




# Key : Redial or Set/Reset Access Pause.

**Figure 2 :** Double Contact Keyboard.
(1) common (connected to VDD).

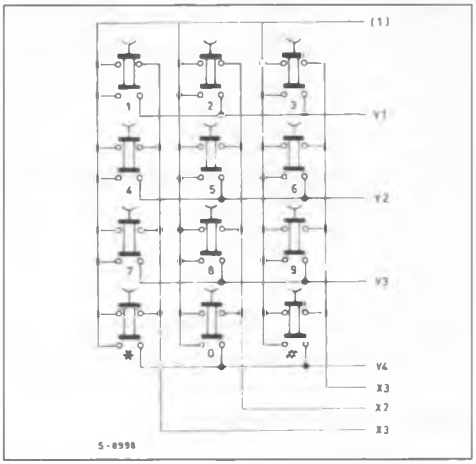
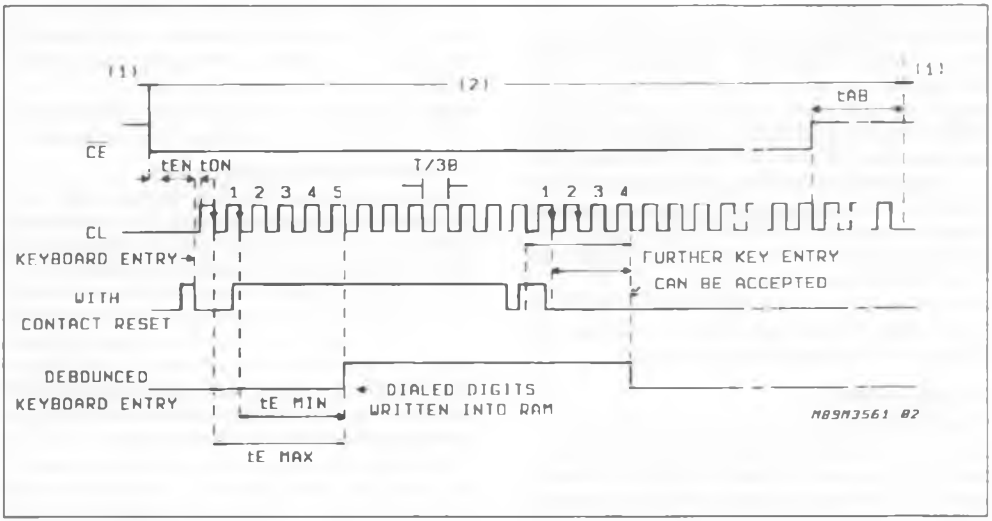



**Figure 3.**

Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply. to $\overline{CE}$ during the transmission of dialing pulses.




(1) Static Standby Mode.
(2) Dialing Mode.

### 5. Data Storage and Data Retrieval

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM, but not yet converted into line pulses.

If more than 32 keycodes are written into the RAM, memory overflow results and the excess keycodes replace the data in the lower-numbered RAM locations. In this event, since an erroneous number is stored, automatic redialing is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first push button to be pressed is not redial (#), the WAC is reset during entry time te, the corresponding keycode is written into the first RAM location and the WAC is then incremented by one to select the next RAM location. Consequently, if the first push button pressed is not redial, the data stored previously in the RAM cannot be redialed anymore.

If the first push button is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialing pulses at output DP. If the redial push button (#) is operated again during the redialling sequence, it will be decoded as an Access Pause Reset. This function will be described later during the description of the access pause system of the M3561. During and after redial, new keyboard entries will be accepted, and converted into correctly timed dialing pulses. These new keyboard are not stored in RAM.

### 6. Dialing Sequence

The dialing sequence can be initiated under the following conditions :

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry) ; see fig. 4.

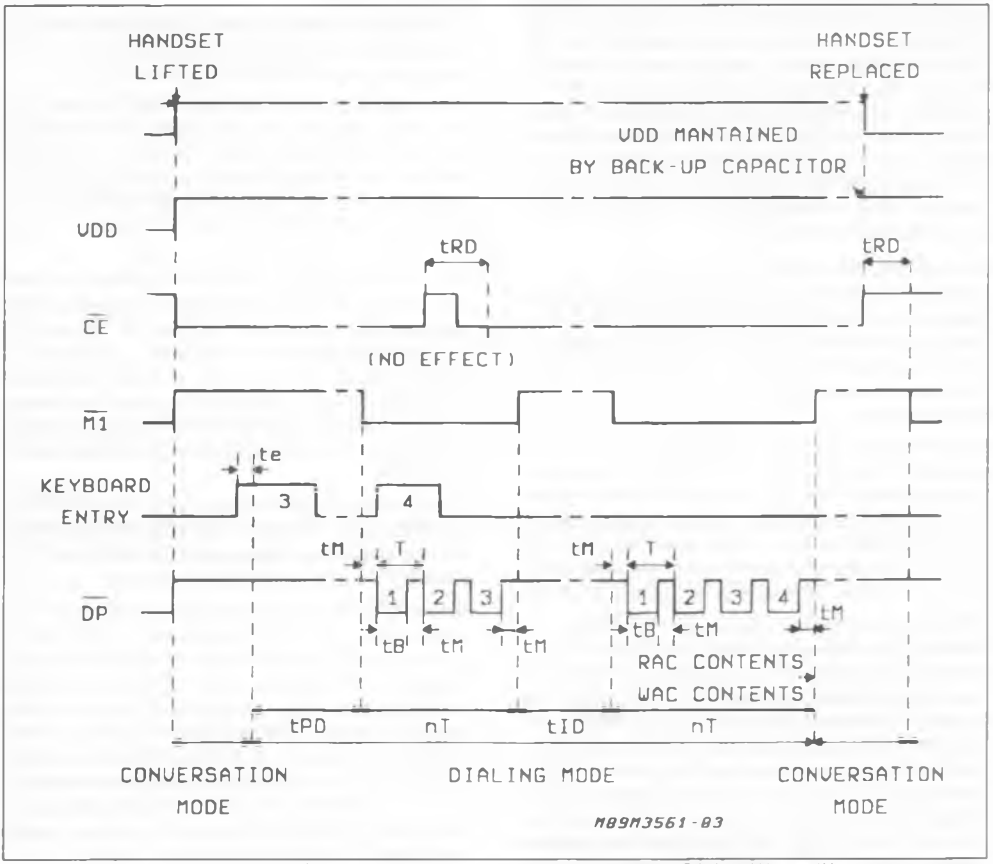
Then, approximately 1ms (ten) after $\overline{CE}$ goes Low, the clock pulse generator is enable, and the circuit is in the conversation mode, while the subscriver waits for the dialing tone. When the first digit of the required number is entered at the keyboard, the clock oscillator starts and data entry period te begins.

The further dialing sequence will be described with the aid of fig. 4. When the keyboard entry has been decoded and written into the RAM, $\overline{M1}$ goes LOW to mute the telephone with a delay of about one Inter Digit Pause time (1.1 *tid), the RAC addresses the RAM and the first keycode is loaded into the register of the output counter, which generates the appropriate number of correctly timed dialing pulses at output DP.

When the digit has been pulsed out, $\overline{M1}$ goes HIGH, at least for one IDP, the RAC is incremented by one, and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out).

When $\overline{M1}$ is High, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if $\overline{CE}$ goes High for more than the reset delay time (trd) at any time during the conversation or dialing mode (e.g., because the handset is replaced). $\overline{CE}$ remains High although VDD is maintained by a backup supply (e.g., because an external diode isolates $\overline{CE}$ from the back-up supply connected to VDD). The RAM retains its contents for subsequent automatic redialing as long as the back-up supply maintains VDD above VDR = 1V.

**Figure 4.**
Timing diagram of dialing sequence with $V_{DD}$ and $\overline{CE}$ Low before keyboard entry (e.g., supply via the cradle contacts).




(1) Oscillator off. All registers except WAC reset. Keyboard input inhibited. Number stored in RAM until $V_{DD}$ >= 1V.

**7. Storage and Regeneration of Access Pauses**

A dial sequence may require an extended Inter Digit Pause if it is necessary to wait for the dial tone. During the keyboard entry, whenever an access pause is needed, a pause code can be stored in the RAM, via the keyboard (# key) for a later redial sequence. When an access pause is regenerated during redialing, it can be terminated via keyboard ( # key).

A pause code takes one position in the RAM like a digit. The number of digits plus the number of access pauses cna therefor bu up to 32.

7.1. MANUAL PAUSE. Access pause codes can be stored in the RAM at appropriate positions by pressing the access pause key (# key). A manual pause code can be stored after any digit. The maximum number of manual pause codes is not limited. Consecutive manual pause codes will generate a single pause during redial.

During the redial sequence the manually stored codes will automatically generate pauses. The duration of the manual pause is unlimited. Whenever a manual pause code is read from the RAM, the normal Inter Digit Pause is extended until it is terminated manually by presssing key #.

### 8. Summary of Special Keyboard Functions

Key # : Inserts a manual pause code, if activated after a number key, or terminates a manual pause, if activated during the pause.

Key # : Starts the redial sequence, if activated as first key after off-hook.

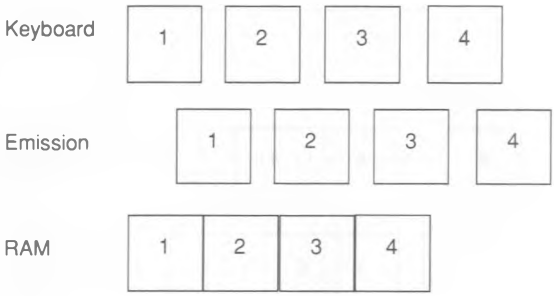
### 9. Statc Standby Operation

$\overline{CE}$ : HIGH turns off the oscillator and resets all internal registers, with the exception of the WRITE ADDRESS COUNTER and the RAM. All input pull-up and pull-down devices are switched off. The current consumption is reduced in this condition such that the supply voltage required to hold the data stored in the RAM can be provided by a capacitor.

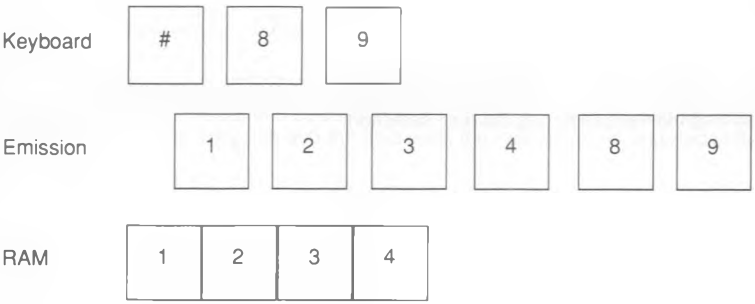
### 10. Selection of Extra Digits During or After Redial

Case 1

1th selection



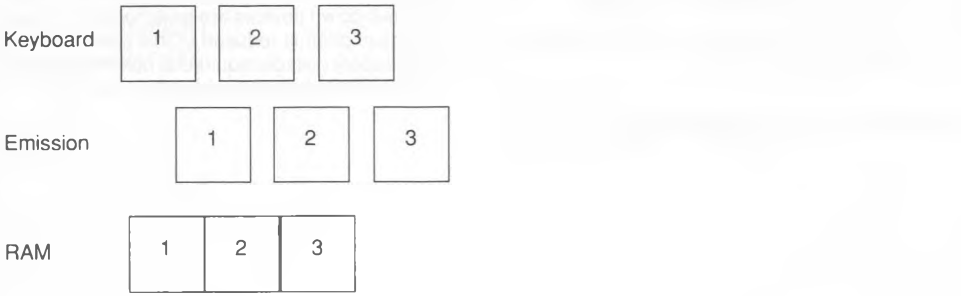

Redial



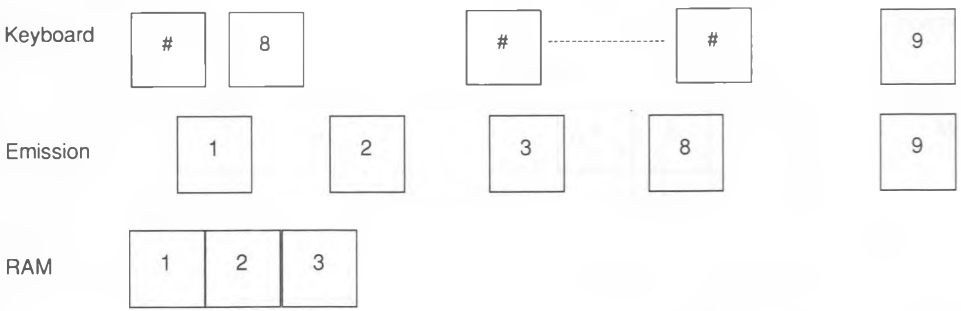

Comment : The key entries 8 and 9 after "Redial" are dialed buty not memorized.

Case 2

1st selection



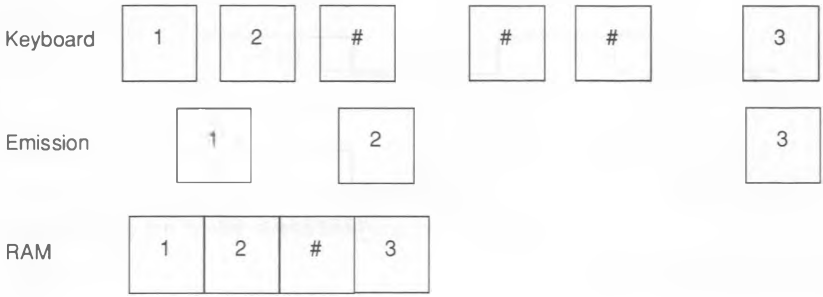

Redial



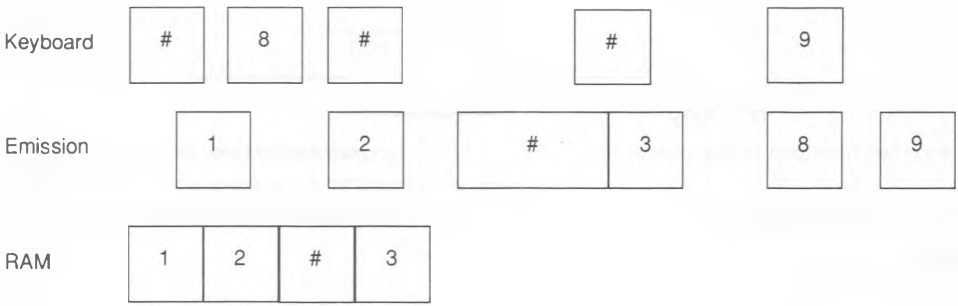

Comment : The first key [#] is used as "Redial", the other keys [#] are ignored because no manual pause was memorized during the first selection.

Case 3

1st selection




Redial

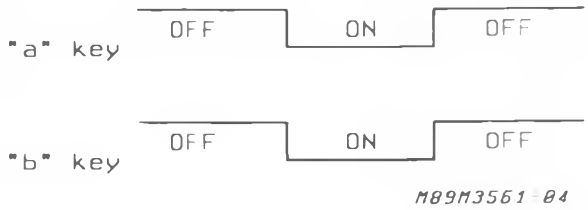



Comment : during the first selection if many keys [#] are pressed consecutively only one is memorized in the RAM. In the second selection the first [#] key is used as Redial, the second is ignored since the emission is still going and the third ends the manual pause inserted in the first selection.

### 11. Multiple Key Pressing

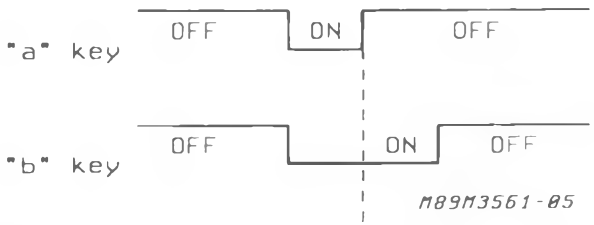
If two keys are pressed at the same time, the following operation will take place.

Case 1




These key inputs will be completely ignored.

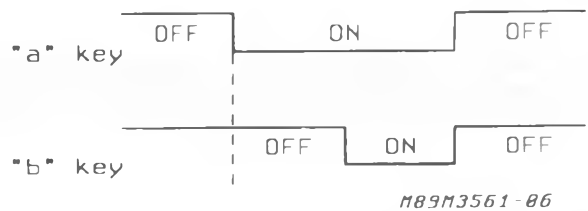
Case 2




The "a" key input wil be ignored.

The "b" key input will be read from this point ( ¦ )

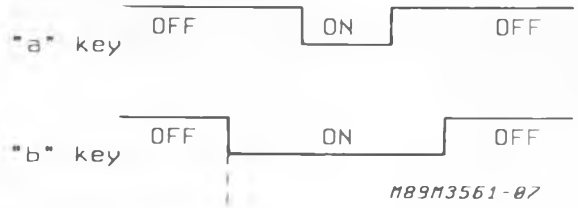
Case 3




The "a" key input will be read from this point ( ¦ )

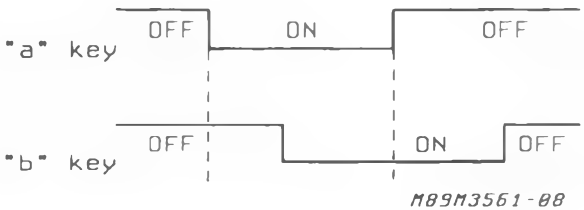
The "b" key input will be ignored.

Case 4




The "b" key input will be read from this point ( | ).
Consequently the "b" key is read once and the "a" key is ignored.

Case 5




The "a" key input wil be read from 1st point ( | ). The "b" key input will be read from 2nd point ( | ).
Consequently the "a" key and the "b" key are read once each.-