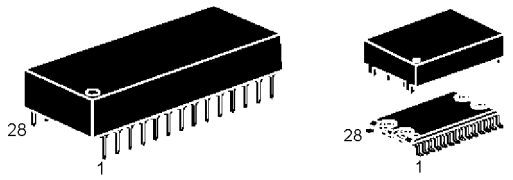
SGS-THOMSON MICROELECTRONICS

M48Z08
M48Z18

CMOS 8K x 8 ZEROPOWER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- UNLIMITED WRITE CYCLES
- READ CYCLE TIME EQUALS WRITE CYCLE TIME
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z08: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48Z18: 4.2V ≤ V_{PFD} ≤ 4.5V
- SELF CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY
- SNAPHAT HOUSING (BATTERY) REPLACEABLE
- 11 YEARS of DATA RETENTION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with the MK48Z08, 18 and JEDEC STANDARD 8K x 8 SRAMs



PCDIP28 (PC)
Battery CAPHAT

SOH28 (MH)
Battery SNAPHAT

DESCRIPTION

The M48Z08,18 ZEOPOWER® RAM is an 8K x 8 non-volatile static RAM which is pin and functional compatible with the MK48Z08,18. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory solution.

Table 1. Signal Names

A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

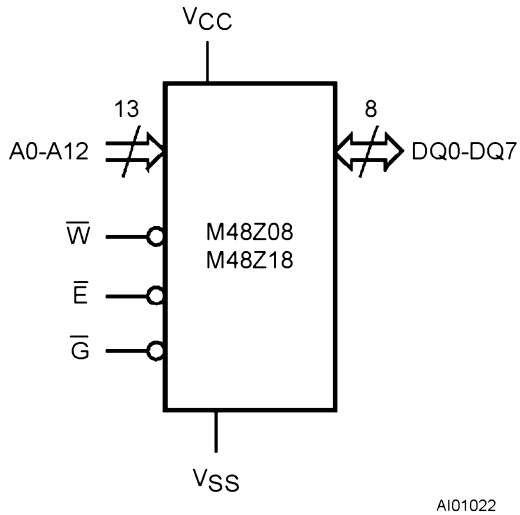
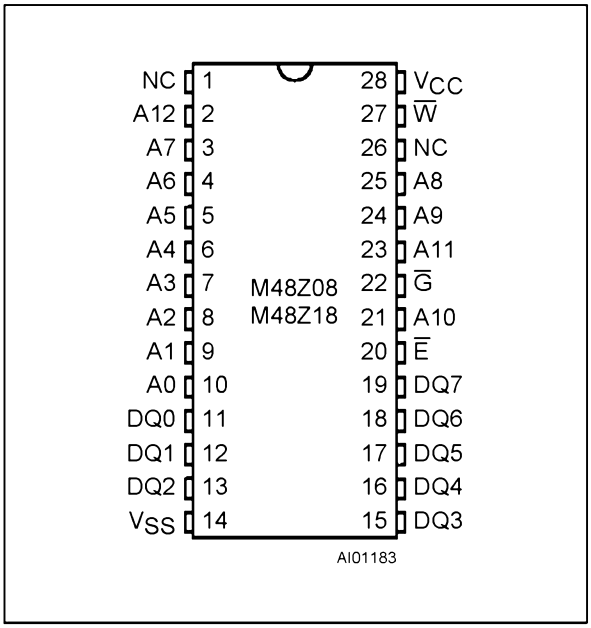
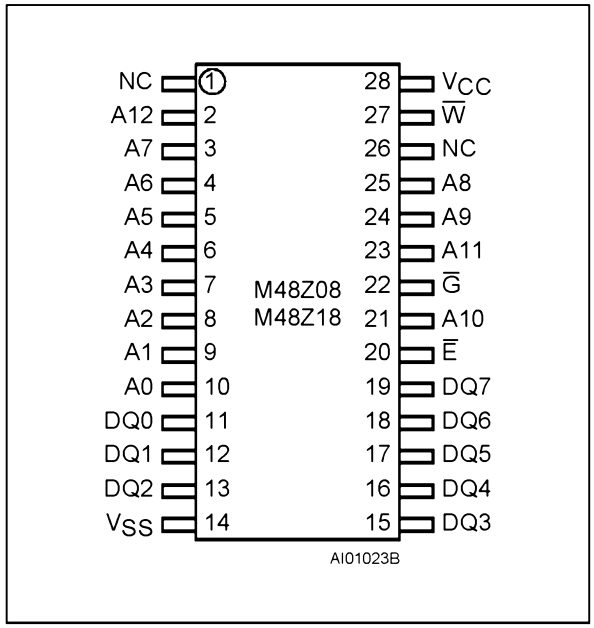


Figure 2A. DIP Pin Connections



Warning: NC = Not Connected

Figure 2B. SO Pin Connections



Warning: NC = Not Connected

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature (V_{CC} Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

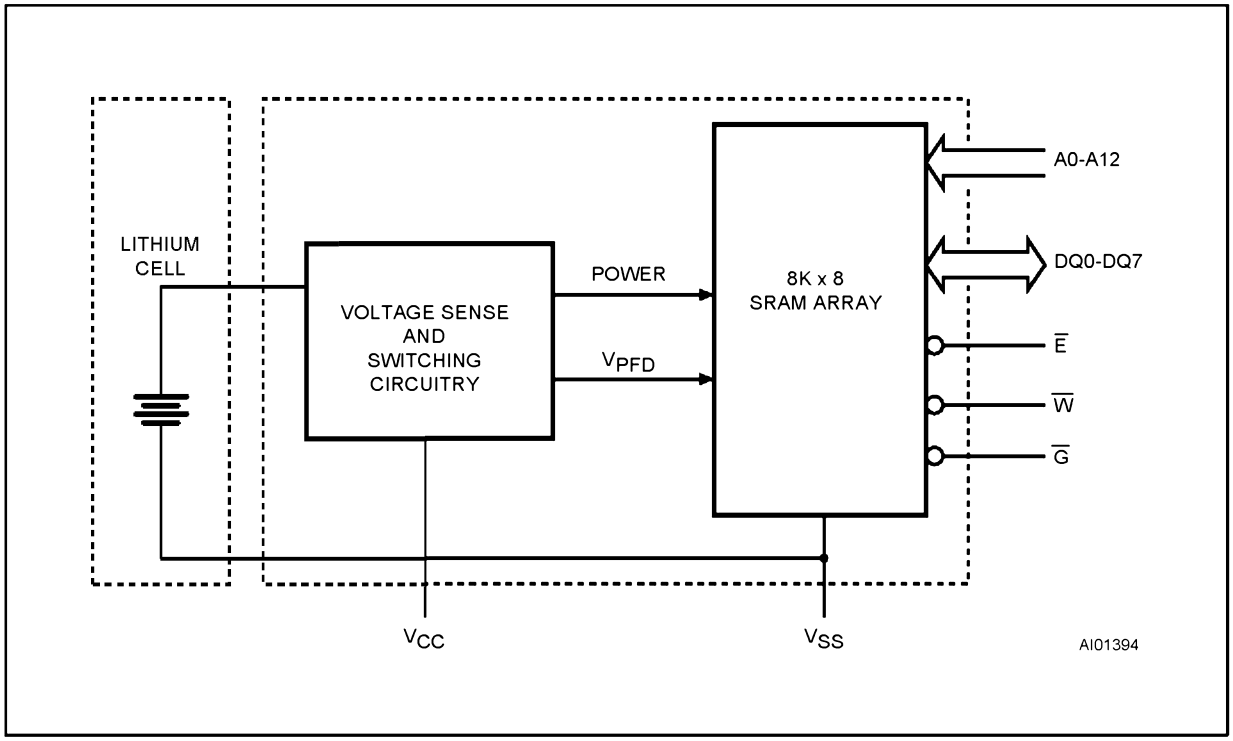
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	High Z	CMOS Standby
Deselect	≤ V_{SO}	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 3. Block Diagram



DESCRIPTION (cont'd)

The M48Z08,18 is a non-volatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The 28 pin 600mil DIP CAPHAT™ houses the M48Z08,18 silicon with a long life lithium button cell in a single package.

The 28 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery. The unique design allows the SNAPHAT battery package to be mounted on top of the SO package after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

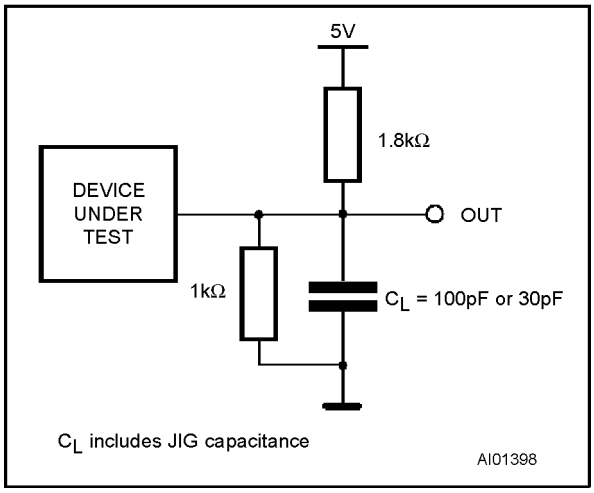


Table 4. Capacitance (1) (T_A = 25 °C)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} (2)	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance calculated from the equation C = IΔt/ΔV with ΔV = 3V and power supply at 5V.
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC}	Supply Current	Outputs open		80	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ = V_{CC} – 0.2V		3	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Table 6. Power Down/Up Trip Points DC Characteristics (1) (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48Z08)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48Z18)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR}	Expected Data Retention Time	11			YEARS

Note: 1. All voltages referenced to V_{SS}.

DESCRIPTION (cont'd)

For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4Z28-BR00SH1".

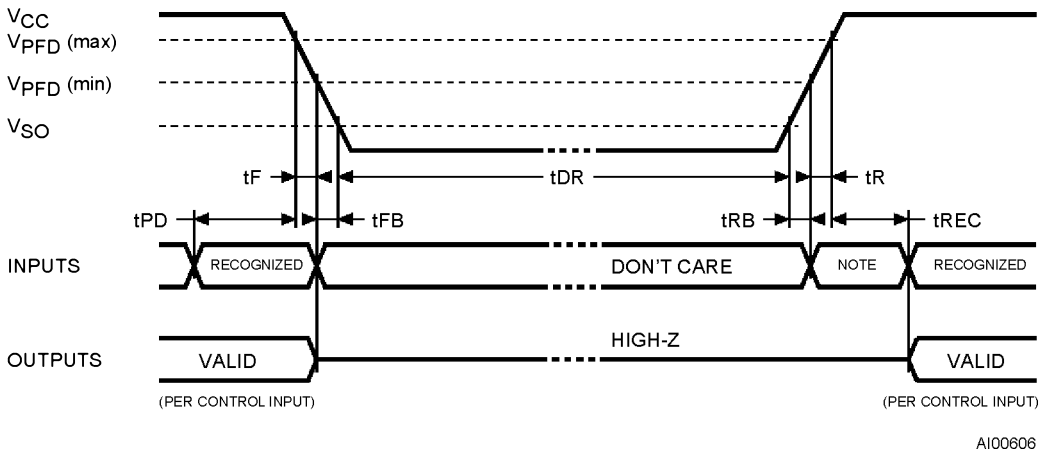
The M48Z08,18 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data until valid power returns.

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	1		ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms



Note: Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E}$ high as V_{CC} rises past V_{PFD}(min). Some systems may performs inadvertent write cycles after V_{CC} rises above V_{PFD}(min) but before normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

Table 8. Read Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z08 / 18 -100		Unit
		Min	Max	
t_{AVAV}	Read Cycle Time	100		ns
t_{AVQV} (1)	Address Valid to Output Valid		100	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		100	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		50	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	10		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	5		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		50	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		40	ns
t_{AXQX} (1)	Address Transition to Output Transition	5		ns

Notes: 1. C_L = 100pF (see Figure 4).
2. C_L = 30pF (see Figure 4).

Figure 6. Read Mode AC Waveforms

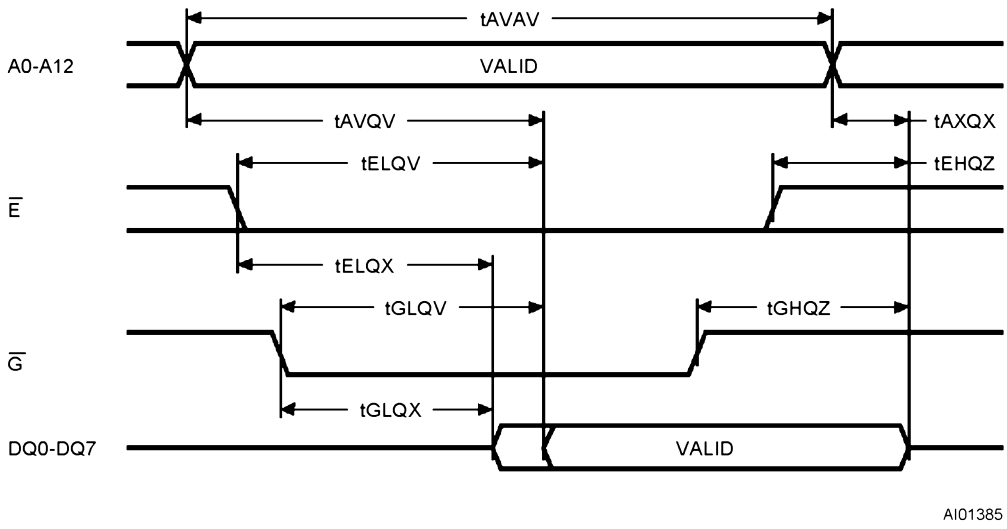


Table 9. Write Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z08 / 18 -100		Unit
		Min	Max	
t_{AVAV}	Write Cycle Time	100		ns
t_{AVWL}	Address Valid to Write Enable Low	0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		ns
t_{WLWH}	Write Enable Pulse Width	80		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	80		ns
t_{WHAX}	Write Enable High to Address Transition	10		ns
t_{EHAX}	Chip Enable High to Address Transition	10		ns
t_{DVWH}	Input Valid to Write Enable High	50		ns
t_{DVEH}	Input Valid to Chip Enable High	30		ns
t_{WHDX}	Write Enable High to Input Transition	5		ns
t_{E1HDX}	Chip Enable High to Input Transition	5		ns
t_{WLQZ} (1, 2)	Write Enable Low to Output Hi-Z		50	ns
t_{AVWH}	Address Valid to Write Enable High	80		ns
t_{AVEH}	Address Valid to Chip Enable High	80		ns
t_{WHQX} (1, 2)	Write Enable High to Output Transition	10		ns

Notes: 1. C_L= 30pF (see Figure 4).
2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

READ MODE

The M48Z08,18 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple- through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 Address Inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48Z08,18 is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$.

A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high of t_{EHAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 7. Write Enable Controlled, Write AC Waveforms

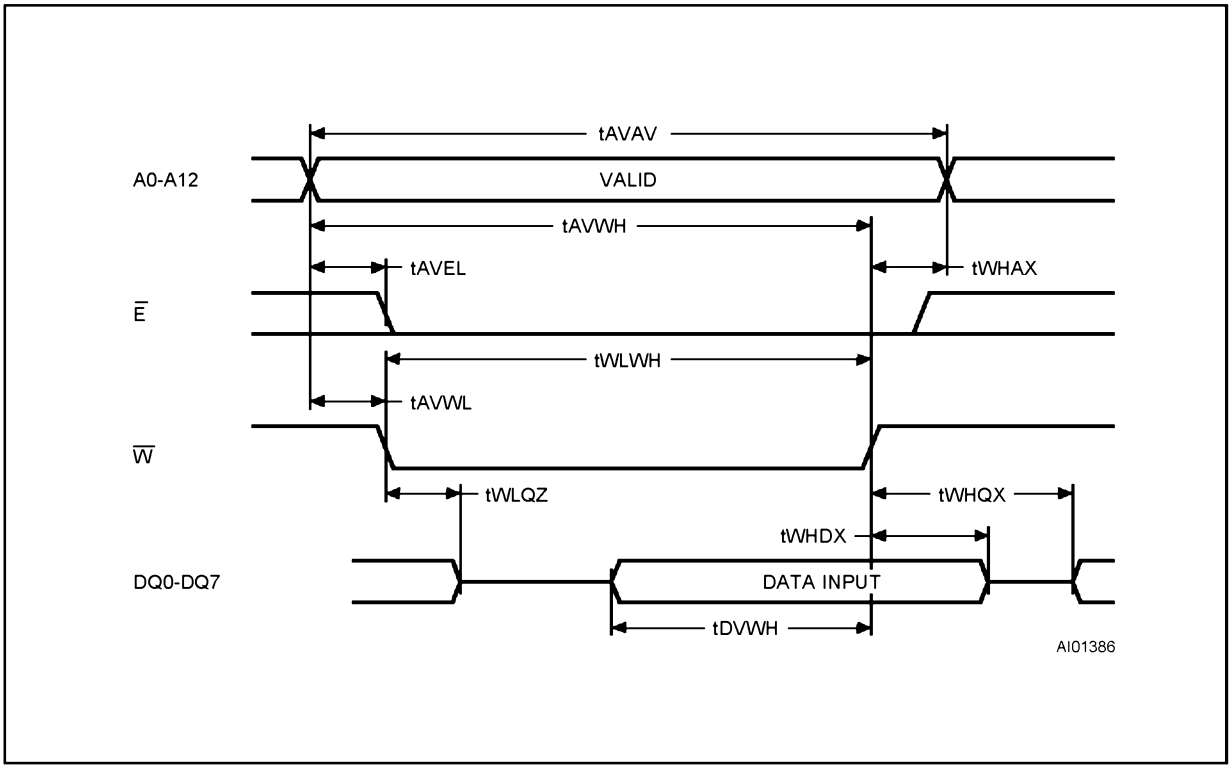
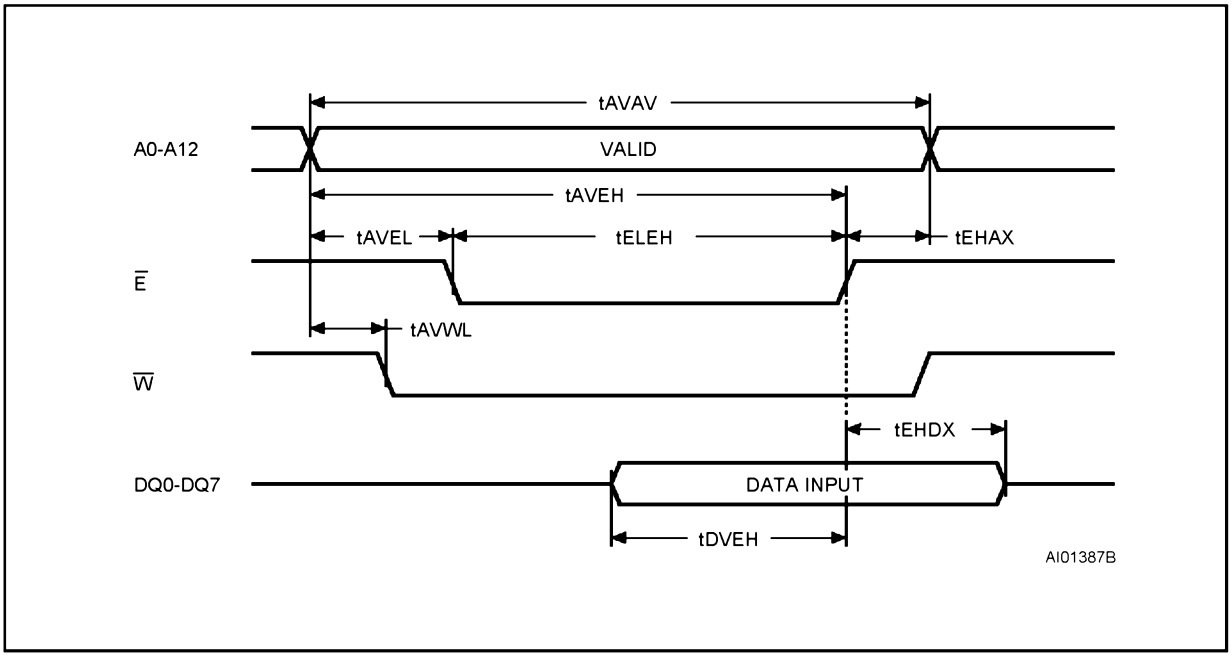


Figure 8. Chip Enable Controlled, Write AC Waveforms



DATA RETENTION MODE

With valid V_{CC} applied, the M48Z08,18 operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

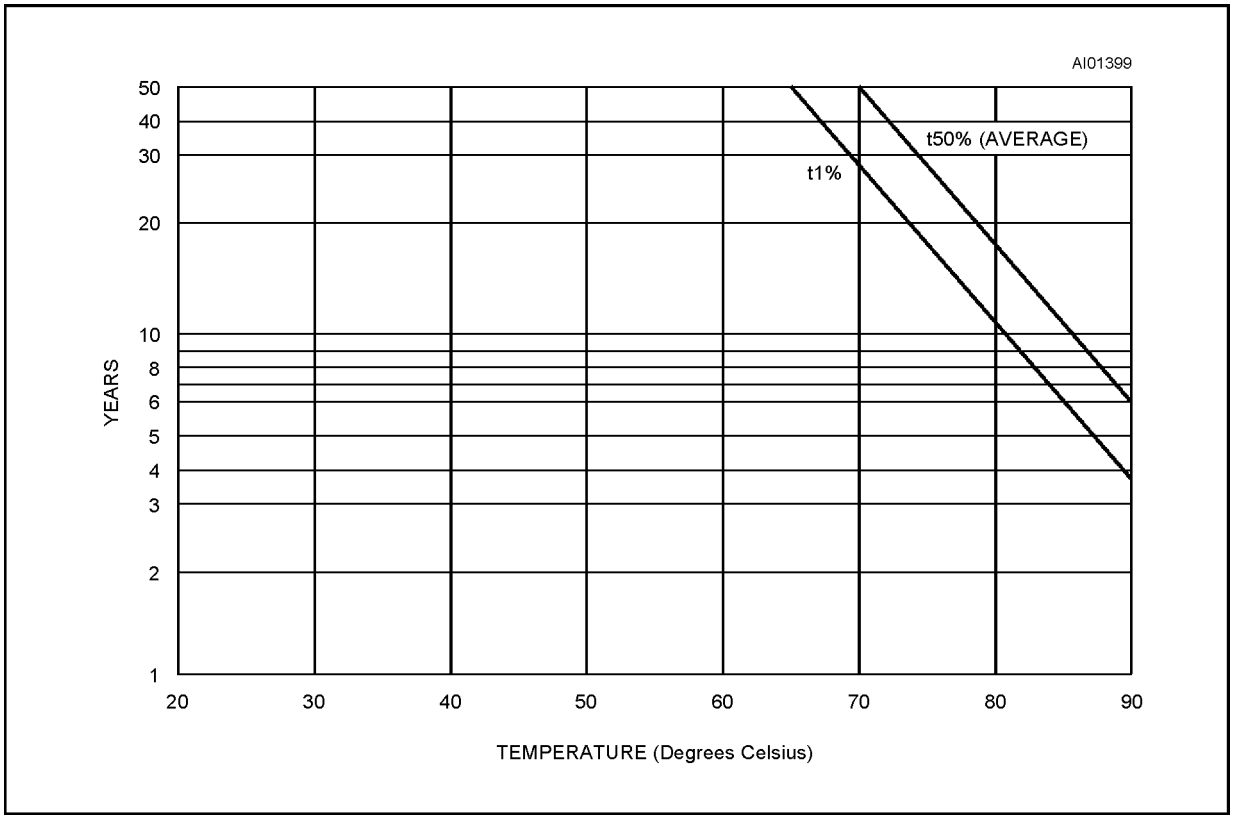
Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48Z08,18 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48Z08,18 for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues until V_{CC} reaches V_{PFD}(min). $\overline{E}$ should be kept high as V_{CC} rises past V_{PFD}(min) to prevent inadvertent write cycles prior to processor stabilization. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max).

SYSTEM BATTERY LIFE

The useful life of the battery in the M48Z08,18 is expected to ultimately come to an end for one of two reasons: either because it has been discharged while providing current to the RAM in the battery back-up mode, or because the effects of aging render the cell useless before it can actually be completely discharged. The two effects are virtually unrelated allowing discharge, or Capacity Consumption, and the effects of aging, or Storage Life, to be treated as two independent but simultaneous mechanisms. The earlier occurring failure mechanism defines the battery system life of the M48Z08,18.

Figure 9. Predicted Battery Storage Life versus Temperature



Cell Storage Life

Storage life is primarily a function of temperature. Figure 9 illustrates the approximate storage life of the M48Z08,18 battery over temperature. The results in Figure 9 are derived from temperature accelerated life test studies performed at SGS-THOMSON. For the purpose of the testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4V closed circuit voltage across a 250 kΩ load resistor. The two lines, $t_{1\%}$ and $t_{50\%}$, represent different failure rate distributions for the cell's storage life. At 70°C, for example, the $t_{1\%}$ line indicates that an M48Z08,18 has a 1% chance of having a battery failure 28 years into its life while the $t_{50\%}$ shows the part has a 50% chance of failure at the 50 year mark. The $t_{1\%}$ line represents the practical onset of wear out and can be considered the worst case Storage Life for the cell. The $t_{50\%}$ can be considered the normal or average life.

Calculating Storage Life

The following formula can be used to predict storage life:

$$\frac{1}{\{[(TA1/TT)/SL1]+[(TA2/TT)/SL2]+...+[(TAN/TT)/SLN]\}}$$

where,

- TA1, TA2, TAN = time at ambient temperature 1, 2, etc.
- TT = total time = TA1+TA2+...+TAN
- SL1, SL2, SLN = storage life at temperature 1, 2, etc.

For example an M48Z08,18 is exposed to temperatures of 55°C or less for 8322 hrs/yr, and temperatures greater than 60°C but less than 70°C for the remaining 438 hrs/yr. Reading predicted $t_{1\%}$ values from Figure 9,

- SL1 ≅ 200 yrs, SL2 = 28 yrs
- TT = 8760 hrs/yr
- TA1 = 8322 hrs/yr, TA2 = 438 hrs/yr

Predicted storage life ≥

$$\frac{1}{\{[(8322/8760)/200]+[(431/8760)/28]\}}$$

or 154 years.

As can been seen from these calculations and the results, the expected lifetime of the M48Z08, 18 should exced most system requirements.

Estimated System Life

Since either storage life or capacity consumption can end the battery's life, the system life is marked by which ever occurs first.

Reference for System Life

Each M48Z08,18 is marked with a nine digit manufacturing date code in the form of H99XXYYZZ. For example, H995B9431 is:

H = fabricated in Carrollton, TX

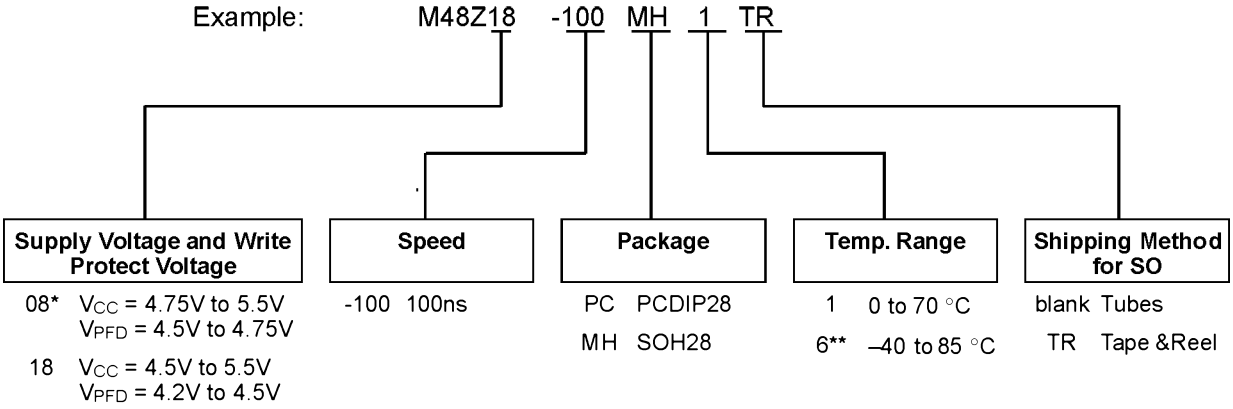
9 = assembled in Muar, Malaysia,

9 = tested in Muar, Malaysia,

5B = lot designator,

9431 = assembled in the year 1994, work week 31.

ORDERING INFORMATION SCHEME



Notes: 08* CAPHAT package only.
6** Temperature range available for M48Z18 product only.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the M48T18 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4Z28-BR00SH1".

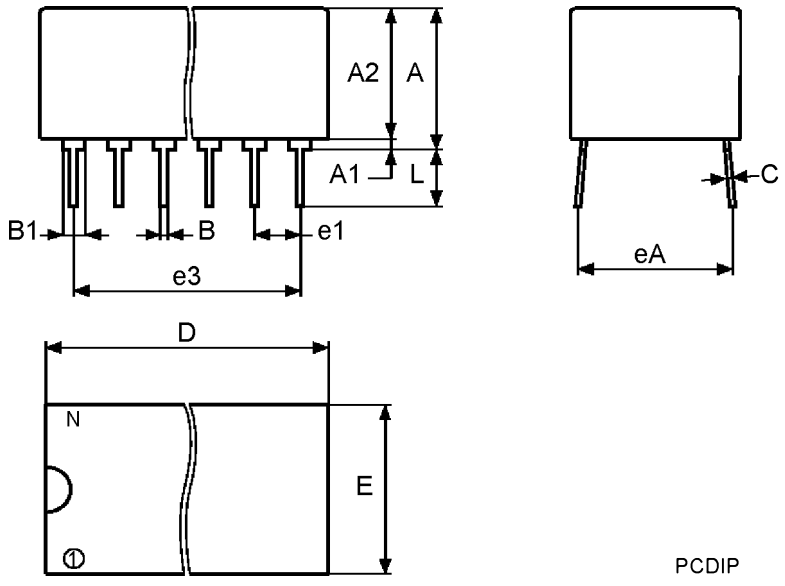
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PCDIP28 - 28 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	28			28		

PCDIP28



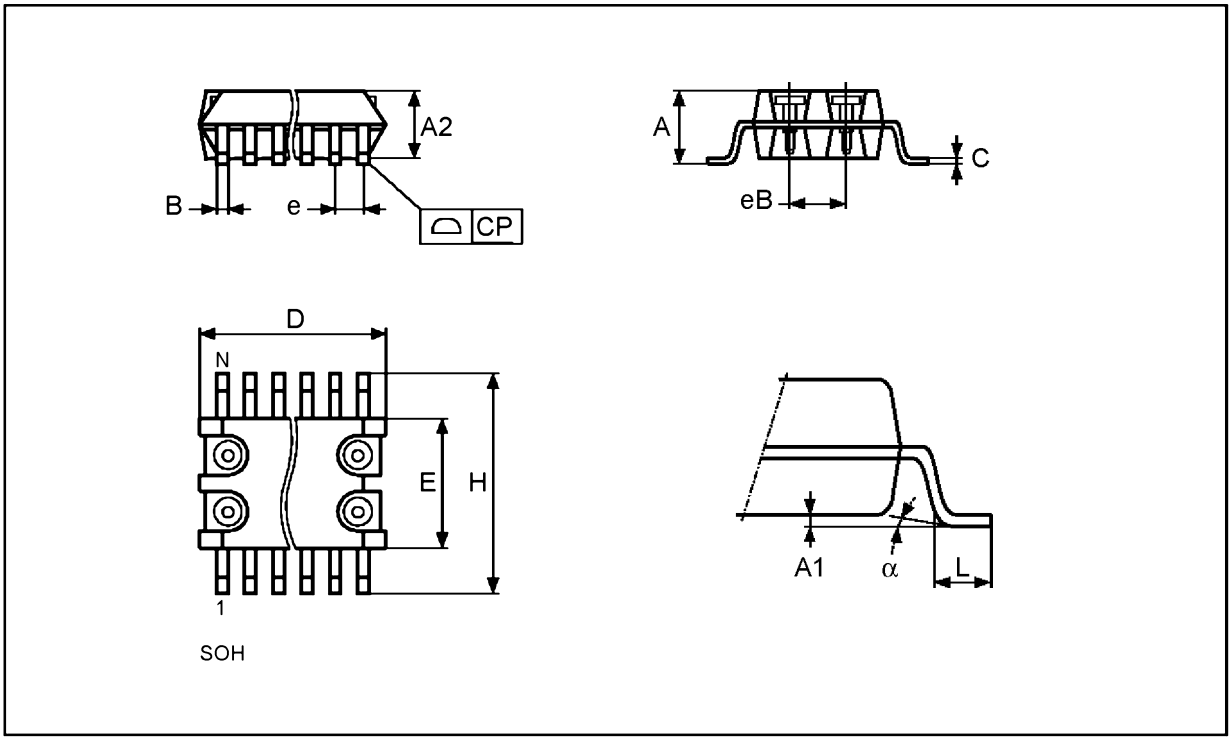
PCDIP

Drawing is not to scale

SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

SOH28



SOH

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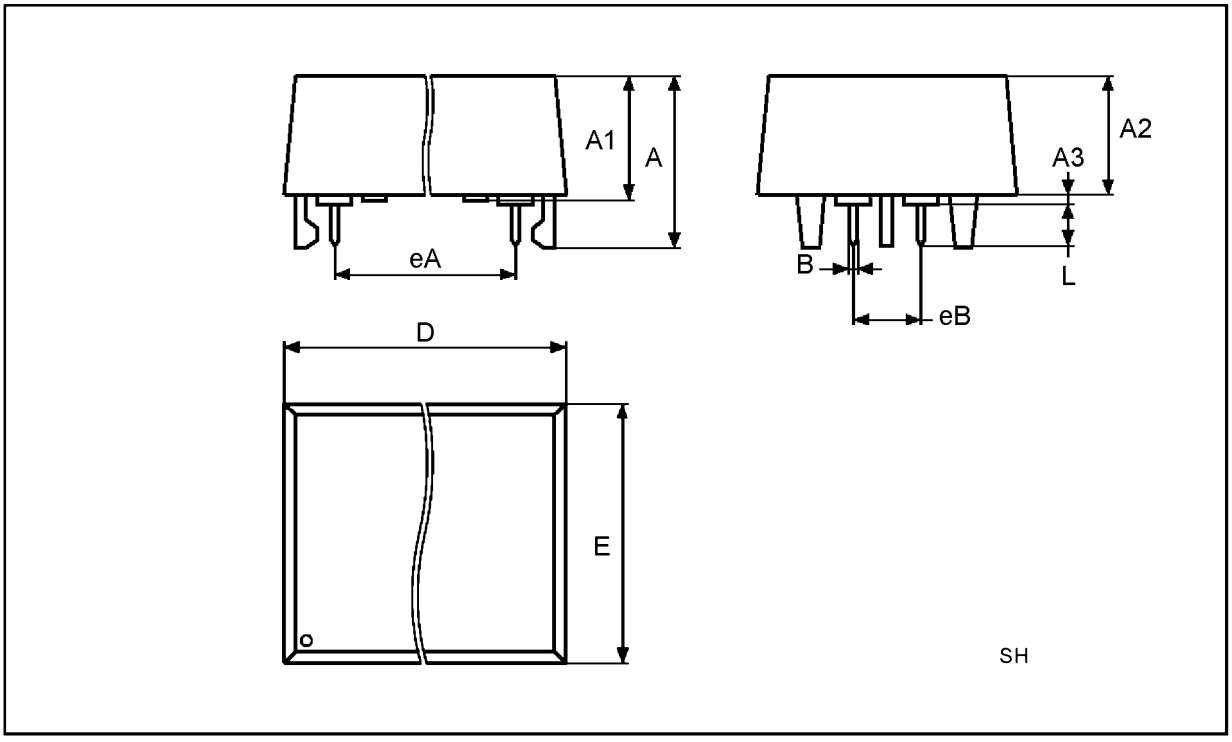
SH28 - SNAPHAT Housing for 28 lead Plastic Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

SH28



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