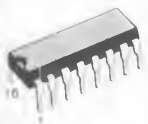
SGS-THOMSON MICROELECTRONICS

M54HC390
M74HC390

DUAL DECADE COUNTER

- HIGH SPEED
  t_{PD} = 13 ns (Typ) at V_{CC} = 5V
- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS390



B1N
Plastic Package

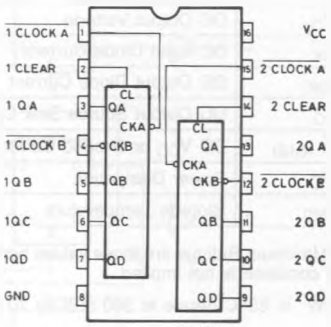
F1
Ceramic Frit Seal Package

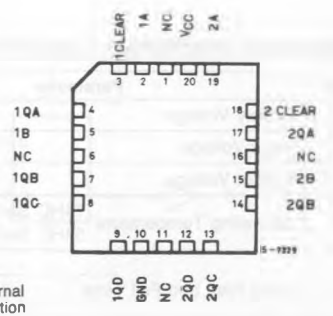
M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC390 F1
M74HC390 B1N
M74HC390 F1
M74HC390 C1
M74HC390 M1

PIN CONNECTION (top view)





NC = No Internal Connection

DESCRIPTION

The M54/74HC390 is a high speed CMOS DUAL DECADE COUNTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

This dual decade counter contains two independent ripple carry counters. Each counter is composed of a divide-by-two and divide-by-five counter. The divide-by-two and divide-by-five counters can be cascaded to form dual decade, dual biquinary, or various combinations up to a single divide-by-100 counter.

Each 4-bit counter is incremented on the high to low transition (negative edge) of the clock input, and each has an independent clear input. When clear is set low all four bits of each counter are set to low. This enables count truncation and allows the implementation of divide-by-N counter configurations.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

COUNT	OUTPUTS							
	BCD COUNT *				BI-QUINARY **			
	QD	QC	QB	QA	QA	QD	QC	QB
0	L	L	L	L	L	L	L	L
1	L	L	L	H	L	L	L	H
2	L	L	H	L	L	L	H	L
3	L	L	H	H	L	L	H	H
4	L	H	L	L	L	H	L	L
5	L	H	L	H	H	L	L	L
6	L	H	H	L	H	L	L	H
7	L	H	H	H	H	L	H	L
8	H	L	L	L	H	L	H	H
9	H	L	L	H	H	H	L	L

INPUTS			OUTPUTS			
$\overline{\text{CLOCK A}}$	$\overline{\text{CLOCK B}}$	CLEAR	QA	QB	QC	QD
X	X	H	L	L	L	L
↓	X	L	BINARY COUNT UP			
X	↓	L	QUINARY COUNT UP			

Note: * Output QA is connected to input $\overline{\text{CLOCK B}}$ for BCD count.
** Output QD is connected to input $\overline{\text{CLOCK A}}$ for bi-quinary count.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

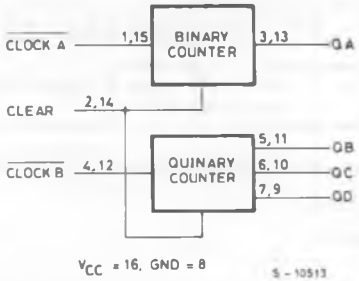
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

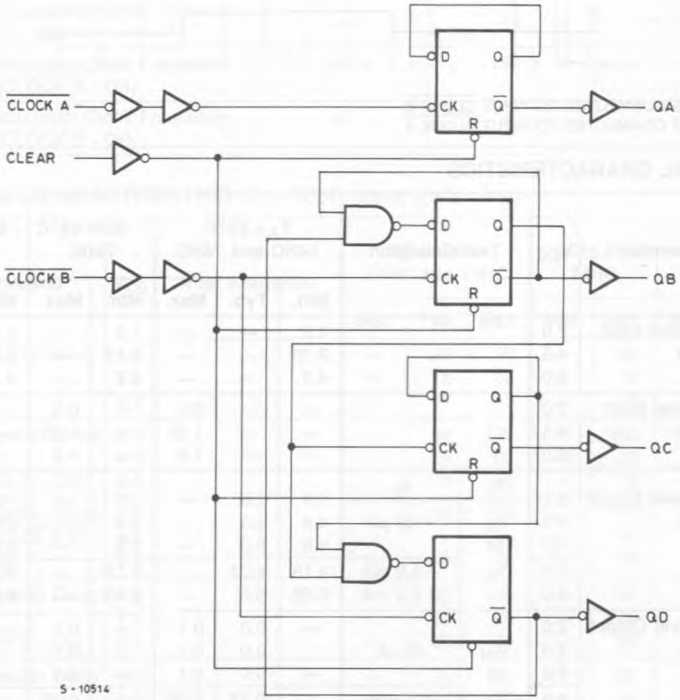
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

BLOCK DIAGRAM

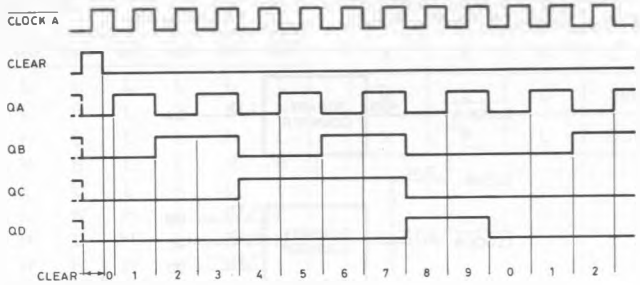


LOGIC DIAGRAM

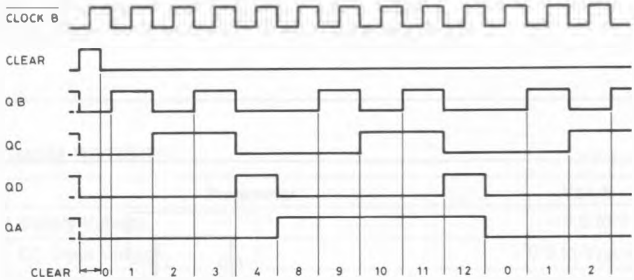


TIMING CHART

(1) BCD COUNT SEQUENCE*



(2) BI-QUINARY COUNT SEQUENCE**



* OUTPUT QA IS CONNECTED TO INPUT $\overline{\text{CLOCK B}}$
** OUTPUT QD IS CONNECTED TO INPUT $\overline{\text{CLOCK A}}$

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			− 40 to 85°C 74HC		− 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND	—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND	—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time	—	4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$ - QA)	—	13	21	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{B}$ - QB, QD)	—	14	23	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{B}$ - QC)	—	21	33	ns
t_{PHL}	Propagation Delay Time (CL - Q)	—	16	26	ns
f_{MAX}	Maximum Clock Frequency ($\overline{CLOCK\ A}$ - QA)	35	64	—	MHz
f_{MAX}	Maximum Clock Frequency ($\overline{CLOCK\ B}$ - QB)	30	45	—	MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			− 40 to 85°C 74HC		− 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK\ A}$ - QA)	2.0		—	64	130	—	165		195	ns
		4.5		—	16	26	—	33		39	
		6.0		—	14	22	—	28		33	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK\ B}$ (Q_B, Q_N)	2.0		—	68	135	—	170		205	ns
		4.5		—	17	27	—	34		41	
		6.0		—	14	23	—	29		35	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLOCK\ B}$ - Q_C)	2.0		—	96	185	—	230		280	ns
		4.5		—	24	37	—	46		56	
		6.0		—	20	31	—	39		48	
t_{PHL}	Propagation Delay Time (CLEAR - Qn)	2.0		—	76	150	—	190		225	ns
		4.5		—	19	30	—	38		45	
		6.0		—	16	26	—	33		38	

AC ELECTRICAL CHARACTERISTICS (Continued)

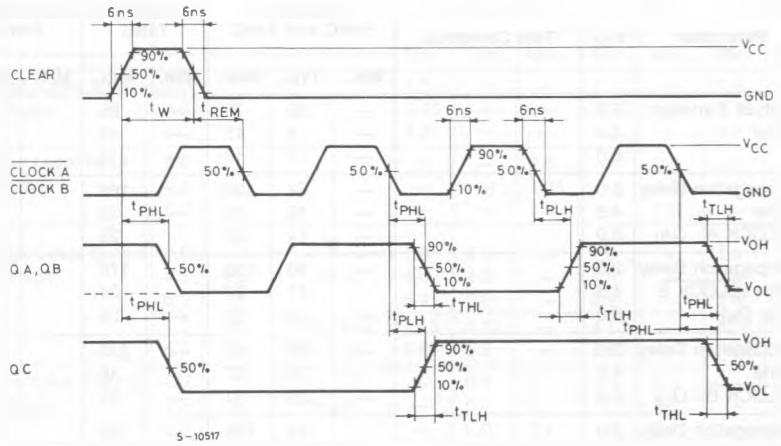
Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency ($\overline{CLOCK}$ A - QA	2.0 4.5 6.0		6.4 32 28	15 58 68	— — —	5.2 26 31	— — —	4.2 21 25	— — —	MHz
f_{MAX}	Maximum Clock Frequency ($\overline{CLOCK}$ B - QB)	2.0 4.5 6.0		5.4 27 32	10 41 48	— — —	4.4 22 26	— — —	3.8 19 22	— — —	MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width ($\overline{CLOCK}$)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
$t_{W(L)}$	Minimum Pulse Width (CLEAR)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t_{REM}	Minimum Removal Time	2.0 4.5 6.0		— — —	5 0 0	25 5 5	— — —	30 6 6	— — —	40 8 7	ns
C_{IN}	Input Capacitance			—	5	10	—	10		10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	44	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

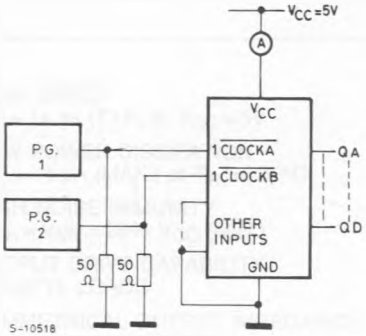
Average operating current can be obtained by the following equation:

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

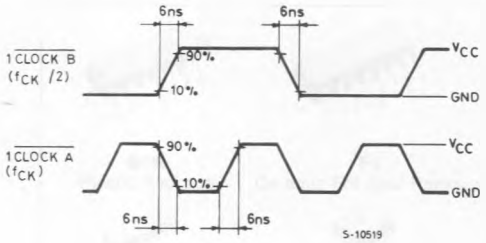
SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



INPUT WAVEFORM



WHEN THE OUTPUTS DRIVE CAPACITIVE LOAD, TOTAL CURRENT CONSUMPTION IS TO BE A SUM OF THE VALUE CALCULATED FROM C_{PD} AND ΔI_{CC} OBTAINED FROM THE FOLLOWING FORMULA.

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \cdot \frac{Ca}{2} + \frac{fCK}{2} \cdot V_{CC} \left(\frac{2Cb}{5} + \frac{Cc}{5} + \frac{Cd}{5}\right)$$

Ca – Cd ARE THE CAPACITANCE AT QA – QD OUTPUT.