

## HC692 DECADE COUNTER/REGISTER (3-STATE) HC693 4 BIT BINARY COUNTER/REGISTER (3-STATE)

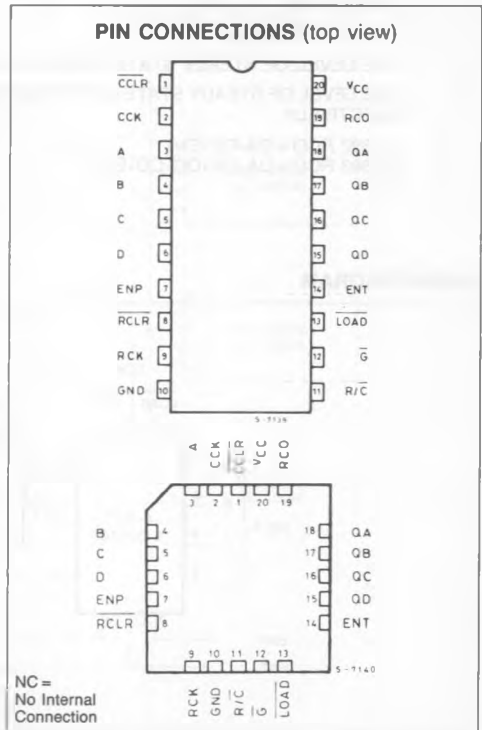
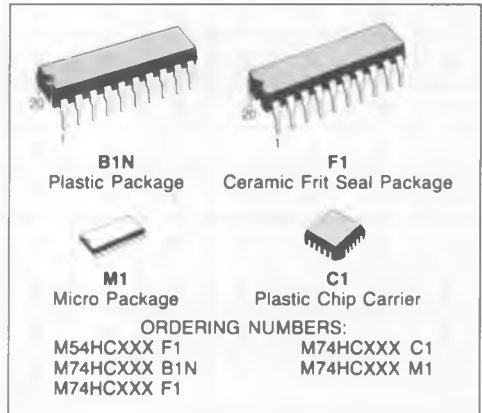
- **HIGH SPEED**  
 $f_{MAX} = 33\text{MHz}$  (TYP.) at  $V_{CC} = 5\text{V}$
- **LOW POWER DISSIPATION**  
 $I_{CC} = 4\ \mu\text{A}$  (MAX.) at  $T_A = 25^\circ\text{C}$
- **HIGH NOISE IMMUNITY**  
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (MIN.)
- **OUTPUT DRIVE CAPABILITY**  
 15 LSTTL LOADS (FOR  $Q_A$  to  $Q_D$ )  
 10 LSTTL LOADS (FOR RCO)
- **SYMMETRICAL OUTPUT IMPEDANCE**  
 $|I_{OH}| = |I_{OL}| = 6\ \text{mA}$  (MIN.) FOR  $Q_A$  to  $Q_D$   
**OUTPUT**  
 $|I_{OH}| = |I_{OL}| = 4\ \text{mA}$  (MIN.) FOR RCO OUTPUT
- **BALANCED PROPAGATION DELAYS**  
 $t_{PLH} = t_{PHL}$
- **WIDE OPERATING VOLTAGE RANGE**  
 $V_{CC}(\text{OPR}) = 2\text{V}$  to  $6\text{V}$
- **PIN AND FUNCTION COMPATIBLE**  
 WITH LSTTL 54/74LS692/693

### DESCRIPTION

The HC692/693 are high speed CMOS COUNTER/REGISTER fabricated with silicon gate C<sup>2</sup>MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. HC692 is BCD DECADE COUNTER, HC693 is 4-BIT BINARY COUNTER, these devices also have registers. If the LOAD input (LOAD) is held "L", DATA input (A-D) are loaded in to the internal counter at positive edge of counter clock input (CCK). In the counter mode, internal counter counts up at the positive of the counter clock. If the counter clear input (CCLR) is held "L", the internal counter is cleared synchronously to the counter clock.

The internal counter's outputs are stored in the output register at the positive edge of the register clock (RCK). If the register clear input (RCLR) is held "L", the register is cleared synchronously to register clock. At this point, the internal counter outputs do not change. The outputs ( $Q_A$ - $Q_D$ ) select internal counter outputs or register outputs respectively with the output select input (R/C).

Two enable inputs (ENT and ENP) and carry output (RCO) are provided to enable easy cascading of the counters, which facilitates easy implementation of N-bit counters without using external gates. All inputs are equipped with protection circuits against static discharge and transient excess voltage.



TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
$\overline{\text{CCLR}}$	$\overline{\text{LOAD}}$	ENP	ENT	CCK	$\overline{\text{RCLR}}$	RCK	R/C	$\overline{\text{G}}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X		X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X		X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	L	X		X	X	L	L	NO CHANGE				NO COUNT
H	H	X	L		X	X	L	L	NO CHANGE				NO COUNT
H	H	H	H		X	X	L	L	COUNT UP				COUNT UP
X	X	X	X		X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	L		H	L	L	L	L	L	CLEAR REGISTER
X	X	X	X	X	H		H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X		H	L	NO CHANGE				NO LOAD

X : DON'T CARE

Z : HIGH IMPEDANCE

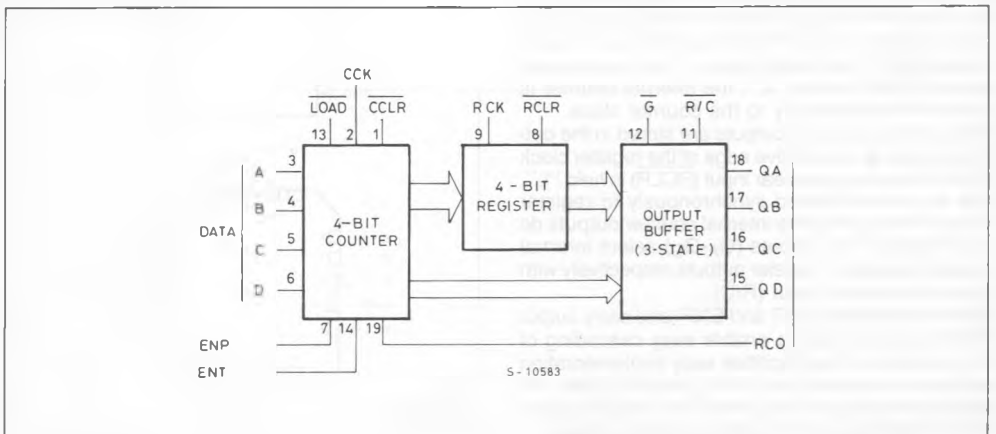
a-d : THE LEVEL OF STEADY STATE INPUTS AT INPUTS A THROUGH D RESPECTIVELY.

a'-d' : THE LEVEL OF STEADY STATE OUTPUTS AT INTERNAL COUNTER OUTPUTS QA' THROUGH QD' RESPECTIVELY.

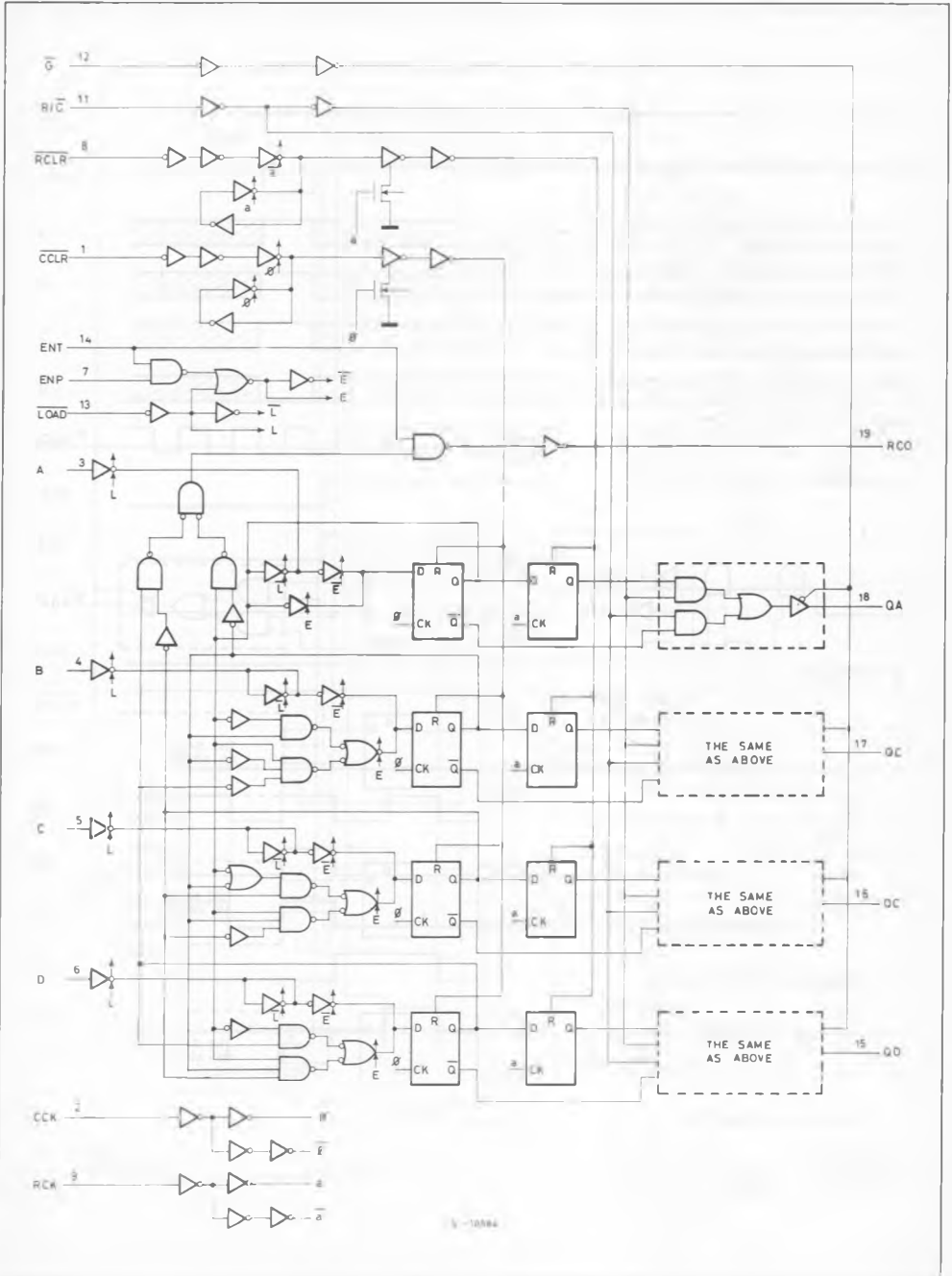
HC692 RCO = QA·QD·ENT

HC693 RCO = QA·QB·QC·QD·ENT

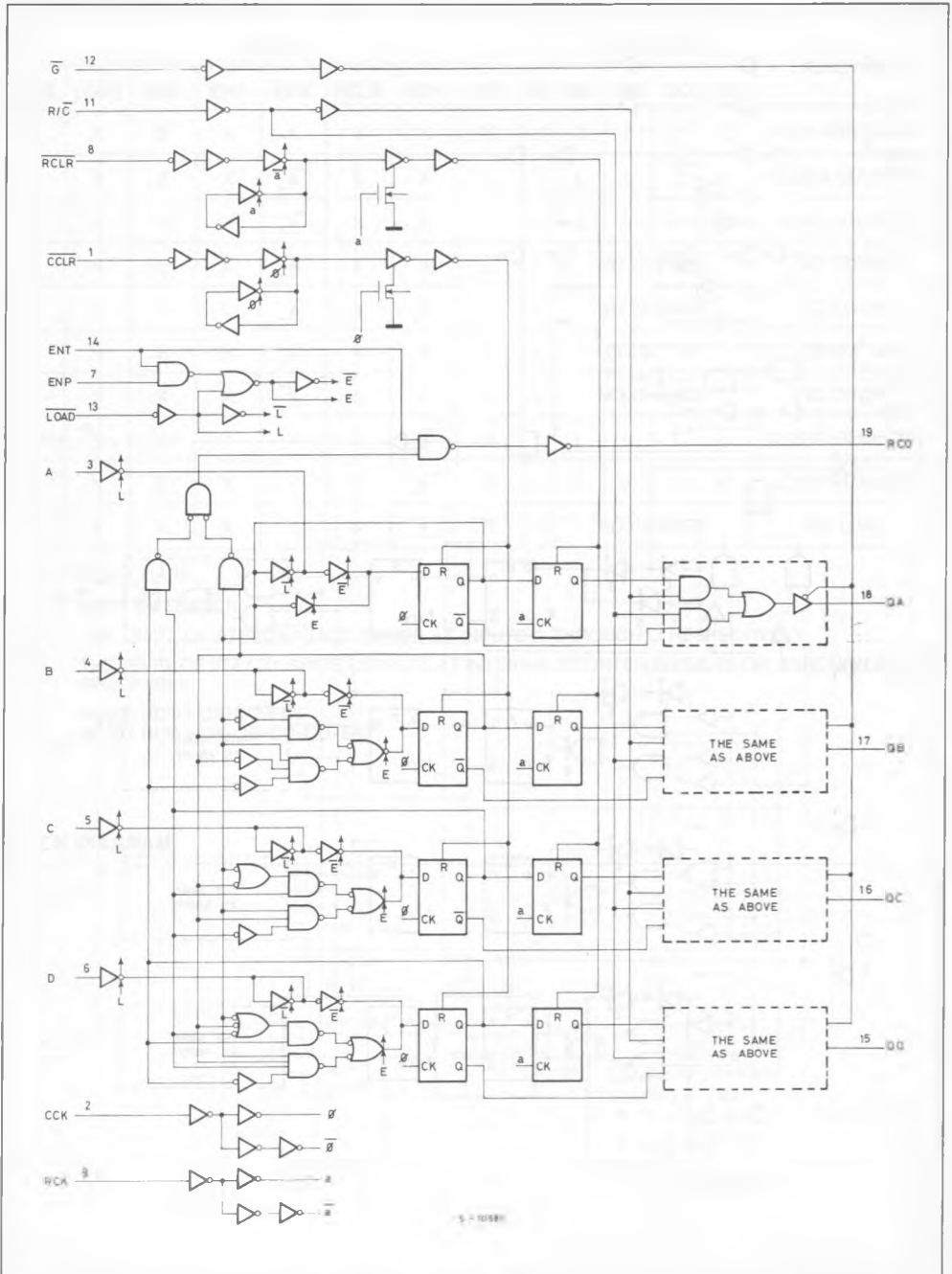
BLOCK DIAGRAM



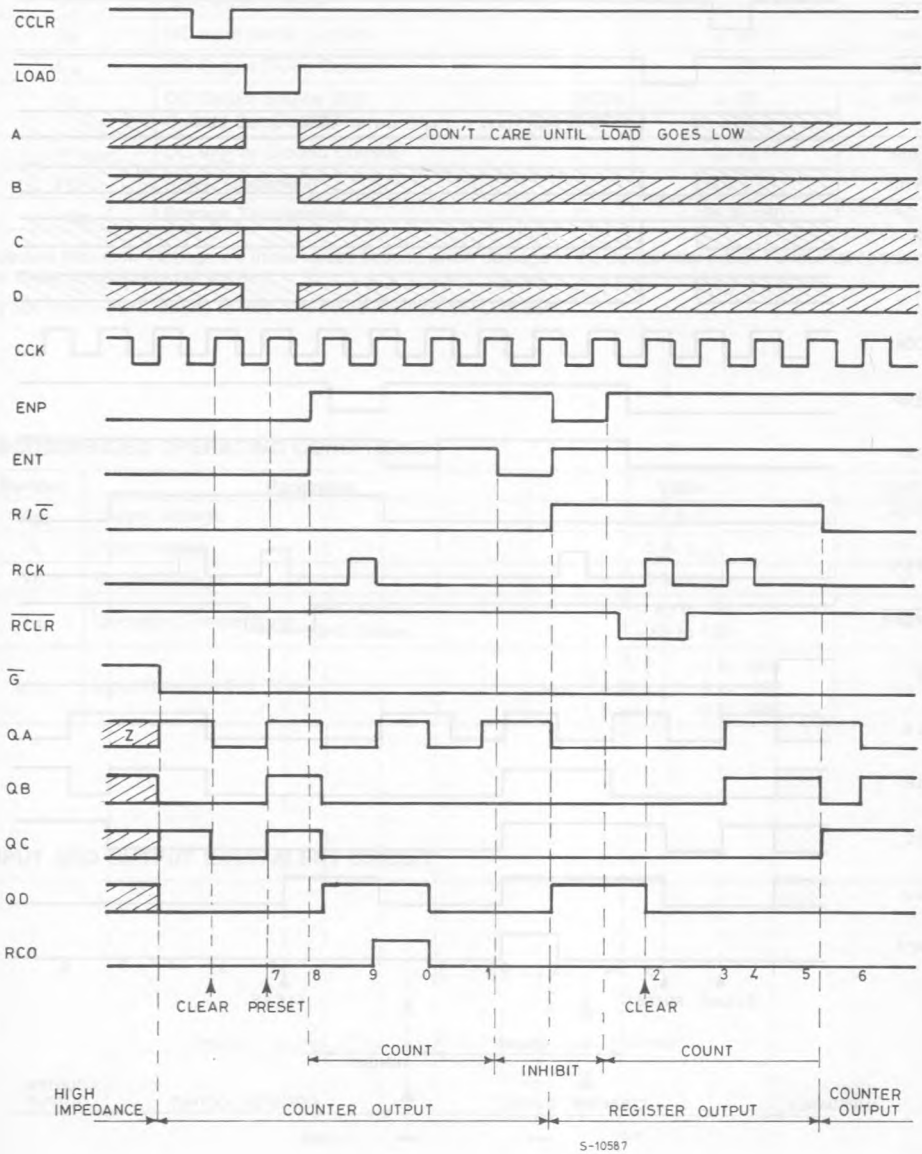
LOGIC DIAGRAM (HC692)



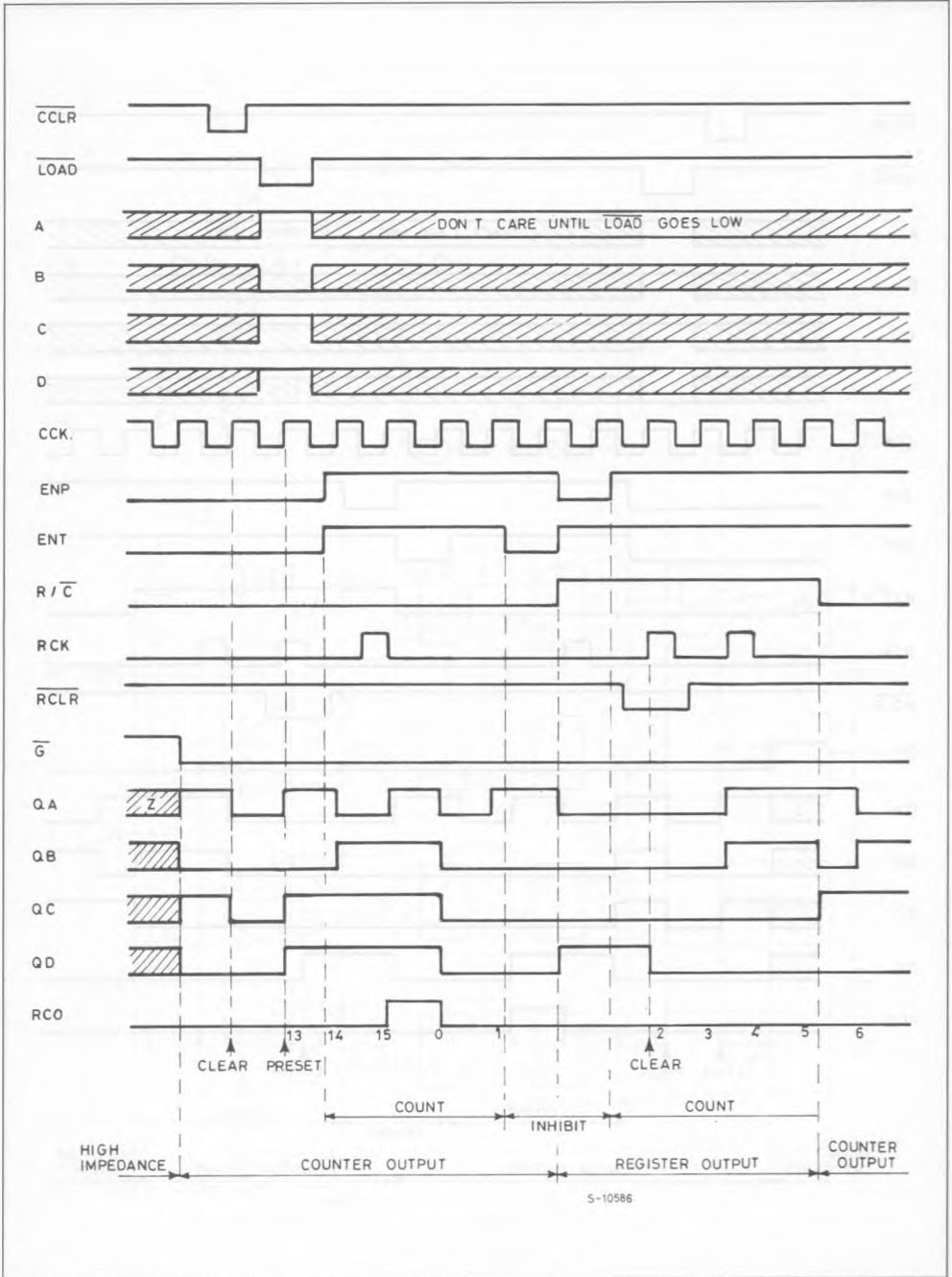
LOGIC DIAGRAM (HC693)



## TIMING CHART (HC692)



TIMING CHART (HC693)



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	- 0.5 to 7	V
$V_I$	DC Input Voltage	- 0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	- 0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Source Sink Current Per Output Pin (RCO) (QA to QD)	$\pm 25$ $\pm 35$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 70$	mA
$P_D$	Power Dissipation	500 (*)	mW
$T_{stg}$	Storage Temperature	- 65 to 150	$^{\circ}C$

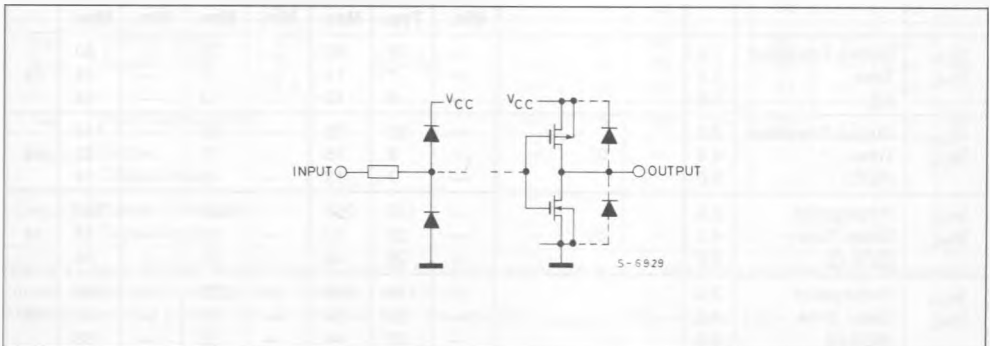
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(\*) 500 mW:  $\cong 65^{\circ}C$  derate to 300 mW by 10 mW/ $^{\circ}C$ :  $65^{\circ}C$  to  $85^{\circ}C$

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	2 to 6	V
$V_I$	Input Voltage	0 to $V_{CC}$	V
$V_O$	Output Voltage	0 to $V_{CC}$	V
$T_A$	Operating Temperature 74HC Series 54HC Series	- 40 to 85 - 55 to 125	$^{\circ}C$
$t_r, t_f$	Input Rise and Fall Time	$V_{CC}$ $\left\{ \begin{array}{l} 2 \text{ V} \\ 4.5 \text{ V} \\ 6 \text{ V} \end{array} \right. \begin{array}{l} 0 \text{ to } 1000 \\ 0 \text{ to } 500 \\ 0 \text{ to } 400 \end{array}$	ns

## INPUT AND OUTPUT EQUIVALENT CIRCUIT



## DC SPECIFICATIONS

Symbol	Parameter	V <sub>CC</sub>	Test Condition	T <sub>A</sub> = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit	
				Min	Typ	Max	Min	Max	Min	Max		
V <sub>IH</sub>	High Level Input Voltage	2.0		1.5	—	—	1.5	—	1.5	—	V	
		4.5		3.15	—	—	3.15	—	3.15	—		
		6.0		4.2	—	—	4.2	—	4.2	—		
V <sub>IL</sub>	Low Level Input Voltage	2.0		—	—	0.5	—	0.5	—	0.5	V	
		4.5		—	—	1.35	—	1.35	—	1.35		
		6.0		—	—	1.8	—	1.8	—	1.8		
V <sub>OH</sub>	High Level Output Voltage	2.0	V <sub>IN</sub>	I <sub>OH</sub>	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V <sub>IH</sub>	- 20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0	or V <sub>IL</sub>		5.9	6.0	—	5.9	—	5.9	—	
		4.5	Q <sub>A</sub> -Q <sub>D</sub>	- 6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		- 7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
4.5	RCO	- 4.0 mA	4.18	4.31	—	4.13	—	4.10	—	V		
6.0		- 5.2 mA	5.68	5.8	—	5.63	—	5.60	—			
V <sub>OL</sub>	Low Level Output Voltage	2.0	V <sub>IN</sub>	I <sub>OL</sub>	—	0	0.1	—	0.1	—	0.1	V
		4.5	V <sub>IH</sub>	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0	or V <sub>IL</sub>		—	0	0.1	—	0.1	—	0.1	
		4.5	Q <sub>A</sub> -Q <sub>D</sub>	6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
4.5	RCO	4.0 mA	—	0.17	0.26	—	0.33	—	0.40	V		
6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40			
I <sub>OZ</sub>	3-State Off Leak Current	6.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND		—	—	±0.5	—	±0.5	—	±10	μA
I <sub>IN</sub>	Input Leakage Current	6.0	V <sub>IN</sub> = V <sub>CC</sub> or GND		—	—	±0.1	—	±1.0	—	±1.0	
I <sub>CC</sub>	Quiescent Supply Current	6.0	V <sub>IN</sub> = V <sub>CC</sub> or GND		—	—	4.0	—	40.0	—	80.0	

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50pF, Input t<sub>r</sub> = t<sub>f</sub> = 6ns)

Symbol	Parameter	V <sub>CC</sub>	Test Condition	T <sub>A</sub> = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t <sub>TLH</sub> t <sub>THL</sub>	Output Transition Time (Q)	2.0		—	25	60	—	75	—	90	ns
		4.5		—	7	12	—	15	—	18	
		6.0		—	6	10	—	13	—	15	
t <sub>TLH</sub> t <sub>THL</sub>	Output Transition Time (RCO)	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (CCK-Q)	2.0		—	132	260	—	325	—	390	ns
		4.5		—	33	52	—	65	—	78	
		6.0		—	28	44	—	55	—	66	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (RCK-Q)	2.0		—	136	260	—	325	—	390	ns
		4.5		—	34	52	—	65	—	78	
		6.0		—	29	44	—	55	—	66	



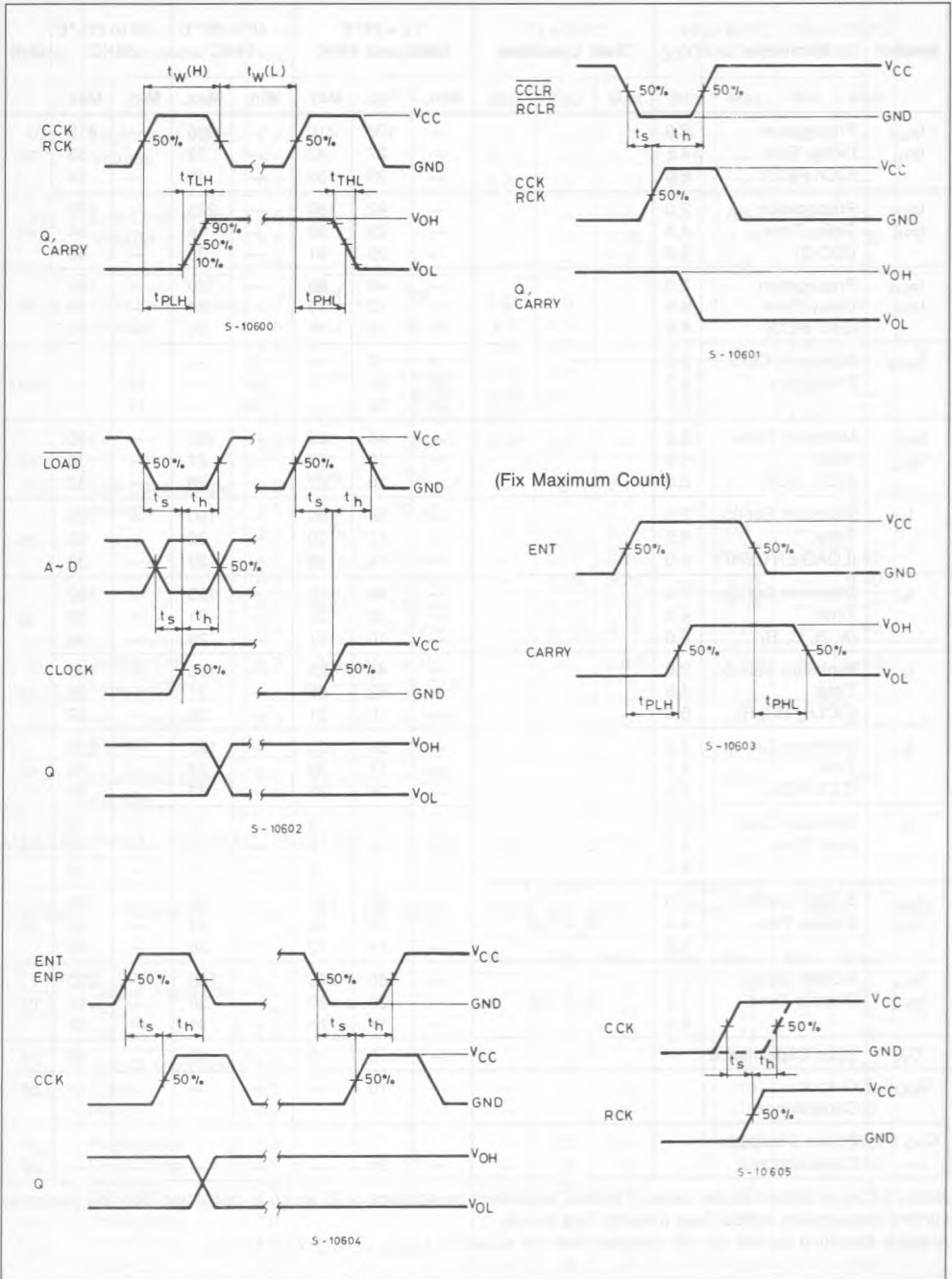
## AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V <sub>CC</sub>	Test Condition	T <sub>A</sub> = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (CCK-RCO)	2.0 4.5 6.0		— — —	108 27 23	210 42 36	— — —	265 53 45	— — —	315 63 54	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (R/C-Q)	2.0 4.5 6.0		— — —	92 23 20	180 36 31	— — —	225 45 38	— — —	270 54 46	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (ENT-RCO)	2.0 4.5 6.0		— — —	48 12 10	95 19 16	— — —	120 24 20	— — —	145 29 25	ns
f <sub>MAX</sub>	Maximum Clock Frequency	2.0 4.5 6.0		4 20 24	8 30 35	— — —	3 16 19	— — —	3 13 15	— — —	MHz
t <sub>W(H)</sub> t <sub>W(L)</sub>	Minimum Pulse Width (CCK, RCK)	2.0 4.5 6.0		— — —	48 12 10	125 25 21	— — —	155 31 26	— — —	190 38 32	ns
t <sub>s</sub>	Minimum Set-up Time (LOAD, ENT, ENP)	2.0 4.5 6.0		— — —	68 17 14	150 30 26	— — —	190 38 33	— — —	225 45 38	ns
t <sub>s</sub>	Minimum Set-up Time (A, B, C, D)	2.0 4.5 6.0		— — —	48 12 10	125 25 21	— — —	155 31 26	— — —	190 38 32	ns
t <sub>s</sub>	Minimum Set-up Time ( $\overline{\text{CCLR}}$ , $\overline{\text{RCLR}}$ )	2.0 4.5 6.0		— — —	48 12 10	125 25 21	— — —	155 31 26	— — —	190 38 32	ns
t <sub>s</sub>	Minimum Set-up Time (CCK-RCK)	2.0 4.5 6.0		— — —	68 17 14	150 30 26	— — —	190 38 33	— — —	225 45 38	ns
t <sub>h</sub>	Minimum Data Hold Time	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t <sub>pZL</sub> t <sub>pZH</sub>	3-State Output Enable Time	2.0 4.5 6.0	R <sub>L</sub> = 1k $\Omega$	— — —	64 16 14	130 26 22	— — —	165 33 28	— — —	195 39 33	ns
t <sub>pLZ</sub> t <sub>pHZ</sub>	3-State Output Disable Time	2.0 4.5 6.0	R <sub>L</sub> = 1k $\Omega$	— — —	80 20 17	145 29 25	— — —	180 36 31	— — —	220 44 38	ns
C <sub>IN</sub>	Input Capacitance			—	5	10	—	10	—	10	pF
C <sub>OUT</sub>	Output Capacitance			—	10	—	—	—	—	—	pF
C <sub>PD</sub> (*)	Power Dissipation Capacitance			—	95	—	—	—	—	—	pF

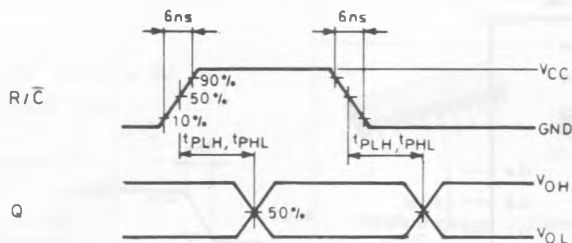
Note (\*) C<sub>PD</sub> is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit).

Average operating current can be obtained from the equation: I<sub>CC(opr.)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>IN</sub> + I<sub>CC</sub>

SWITCHING CHARACTERISTICS TEST WAVEFORM



## SWITCHING CHARACTERISTICS (Continued)



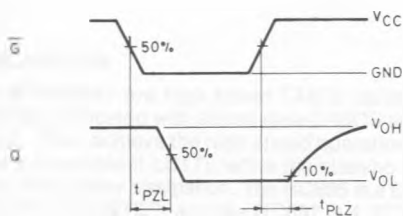
S-10606

 $t_{PLZ}$ ,  $t_{PZL}$ 

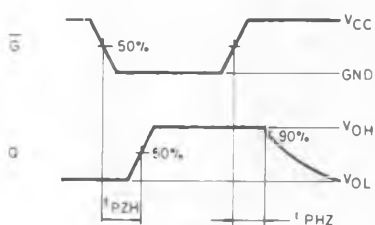
The 1k $\Omega$  load resistors should be connected between outputs and  $V_{CC}$  line and the 50pF load capacitors should be connected between outputs and GND line. All inputs except  $\bar{G}$  input should be connected to  $V_{CC}$  line or GND line such that outputs will be in low logic level while  $\bar{G}$  input is held low.

 $t_{PHZ}$ ,  $t_{PZH}$ 

The 1k $\Omega$  load resistors and the 50pF load capacitors should be connected between each output and GND line. All inputs except  $\bar{G}$  input should be connected to  $V_{CC}$  or GND line such that output will be in high logic level while  $\bar{G}$  input is held low.



S-10607



S-10608

TEST CIRCUIT  $I_{CC}$  (Opr.)

