CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, hardware preparation, installation instructions, monitor program description, operating instructions, hardware description, and support information for the M68HC11 Evaluation Board (EVB).

Downloading S-record information is contained in Appendix A. While a listing of the EVB monitor program is stored on the diskettes supplied with the EVB (see file buf25.asm). (This file may be viewed using any text reader capable of handling a 123K file.)

NOTE

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name denotes that the signal is true or valid when the signal is low.

1.2 FEATURES

EVB features include:

- An economical means of debugging user assembled code and evaluating target systems incorporating MC68HC11 microcomputer unit (MCU) device
- One-line assembler/disassembler
- Host computer downloading capability
- MC68HC11 MCU based debugging/evaluating circuitry
- MC68HC24 Port Replacement Unit (PRU) based MCU I/O expansion circuitry
- MC6850 Asynchronous Communications Interface Adapter (ACIA) based terminal I/O port circuitry
- RS-232C compatible terminal/host computer I/O ports

1.3 SPECIFICATIONS

Table 1-1 lists the EVB specifications.

Table 1-1. EVB Specifications

Characteristics	Specifications
MCU	MC68HC11A1FN
PRU	MC68HC24FN
ACIA	MC68B50
I/O ports: Terminal Host computer MCU extension	 RS-232C compatible RS-232C compatible HCMOS-TTL compatible
Temperature: Operating Storage	 +25 degrees C -40 to +85 degrees C
Relative humidity	0 to 90% (non-condensing)
Power requirements	+5 Vdc @ 0.5 A (max) +12 Vdc @ 0.1 A (max) -12 Vdc @ 0.1 A (max)
Dimensions: Width Length	 7.062 in. (17.8 cm) 4.625 in. (11.75 cm)

1.4 GENERAL DESCRIPTION

The MC68HC11 MCU device is an advanced single-chip MCU with on-chip memory and peripheral functions. Refer to the MC68HC11 MCU data sheet for additional device information. To demonstrate the capabilities of this MCU, the EVB functions with a debug monitor program called BUFFALO (Bit User Fast Friendly Aid to Logical Operations). This monitor program is contained within an on-board EPROM (external to the MCU).

The EVB provides a low cost tool for debugging and evaluation of MC68HC11 MCU-based target system equipment (Figure 1-1 is a block diagram of the EVB). The EVB is not intended to be a replacement for a much more powerful and flexible tool, such as the Motorola M68HC11EVM Evaluation Module. The EVB operates in either the debugging or evaluation (emulation) mode of operation.

The first mode of operation lets you debug your code using the BUFFALO monitor program. User code is assembled on the EVB or on a host computer and then downloaded to the EVB RAM via Motorola S-records. The second mode of operation lets you evaluate (emulate) user code in a target system environment utilizing the memory of the MC68HC11 MCU. The EVB emulates the single-chip mode of operation, even though the EVB operates in the expanded multiplexed mode of operation at all times.

Overall evaluation/debugging control of the EVB is provided by the BUFFALO monitor program via terminal interaction. The target system interface is provided by the MCU and PRU devices. RS-232C terminal/host I/O port interface circuitry provides communication and data transfer operations between the EVB and external terminal/host computer devices.

Independent baud rate selection capabilities are provided for the terminal and host I/O ports. Hardware selectable (300-9600) baud rates are provided for the ACIA-based terminal port. A non-selectable (fixed) 9600 baud rate is provided for the host port via the MCU Serial Communications Interface (SCI).

The EVB requires a user-supplied +5, +12, and -12 Vdc power supply and an RS-232C compatible terminal for operation. An RS-232C compatible host computer is used with the EVB to download Motorola S-records via the BUFFALO monitor commands.

The Motorola S-record format was devised for the purpose of encoding programs or data files in a printable format for transportation between computer systems. The transportation process can therefore be monitored and the S-records can be easily edited. Refer to Appendix A for additional S-record information.

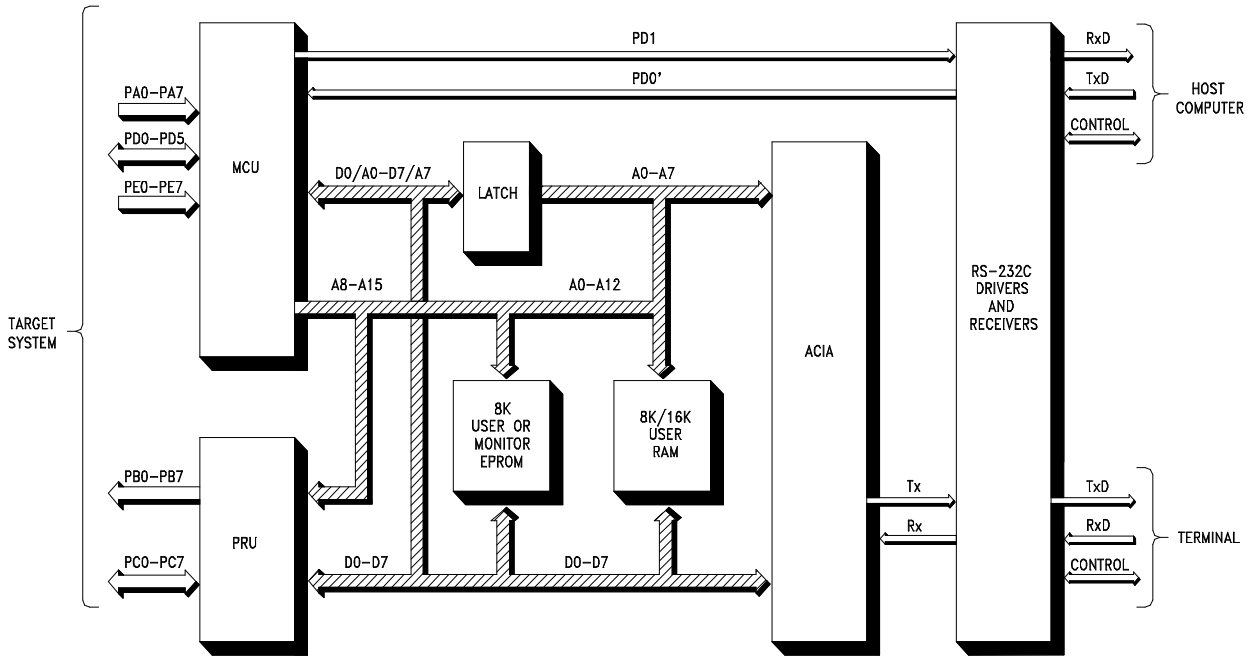


Figure 1-1. EVB Block Diagram

1.5 EQUIPMENT REQUIRED

Table 1-2 lists the external equipment requirements for EVB operation.

Table 1-2. External Equipment Requirements

External Equipment
+5, +12, -12 Vdc power supply(1)
Terminal (RS-232C compatible)
Host computer (RS-232C compatible)(2)
Terminal/host computer - EVB RS-232C cable assembly(1)
Target system - EVB MCU I/O port extension cable assembly(1)

1. Refer to Chapter 2 for details.
2. Optional - not required for basic operation

CHAPTER 5
HARDWARE DESCRIPTION

5.1 INTRODUCTION

This chapter provides an overall general description of the EVB hardware. This description is supported by a simplified block diagram (Figure 5-1) and a memory map diagram (Figure 5-2). The EVB schematic diagram, located in Chapter 6, can also be referred to for the following descriptions.

5.2 GENERAL DESCRIPTION

Overall evaluation/debugging control of the EVB is provided by the monitor BUFFALO program residing in EPROM (external to the MCU) via terminal intervention. The target system interface is provided by the MCU and PRU devices. RS-232C terminal/host I/O port interface circuitry provides communication and data transfer operations between the EVB and external terminal/host computer devices.

5.2.1 Microcomputer

The M68HC11A1 MCU (U10) operates in the expanded mode of operation. This is accomplished by +5 Vdc applied to the MCU MODA and MODB pins. The MCU configuration (CONFIG) register (implemented in EEPROM) is programmed such that the ROMON bit is cleared for EVB operations. When this bit is cleared, MCU internal ROM is disabled , and that memory space becomes externally accessed space. This allows the memory at $E000-$FFFF to contain the monitor BUFFALO program (or user program for emulation) in external EPROM.

The monitor program uses the MCU internal RAM located at $0048-$00FF. The control registers are located at $1000-$103F.

The EVB allows the user to use all the features of the monitor BUFFALO program, however it should be noted that the monitor program uses the MCU on-chip RAM locations $0048-$00FF leaving only 72 bytes for the user (i.e., $0000-$0047). This should be remembered when writing code.

5.2.2 Port Replacement Unit

The EVB operates in the expanded multiplexed mode of operation. An MC68HC24 PRU device (U1) is used to replace the MCU I/O ports B and C (including STRA and STRB control lines) used for single chip mode of operation. The PRU provides the required single chip mode I/O lines for target system evaluation (emulation) via the EVB MCU extension I/O port connector P1.

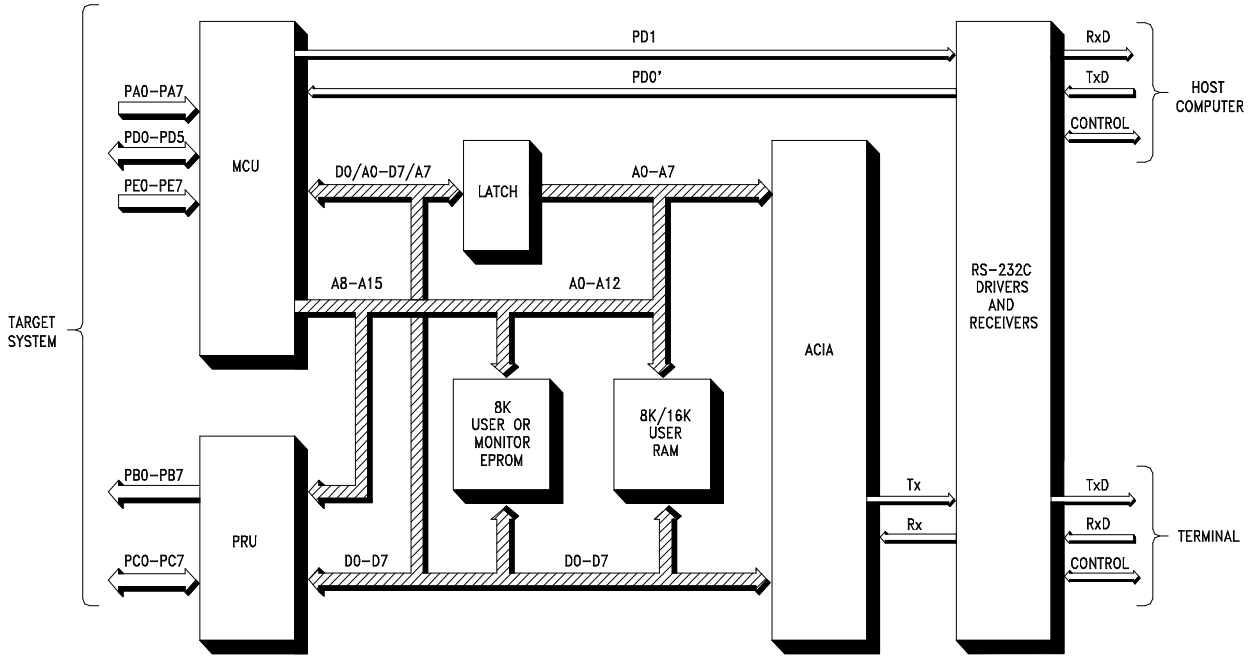
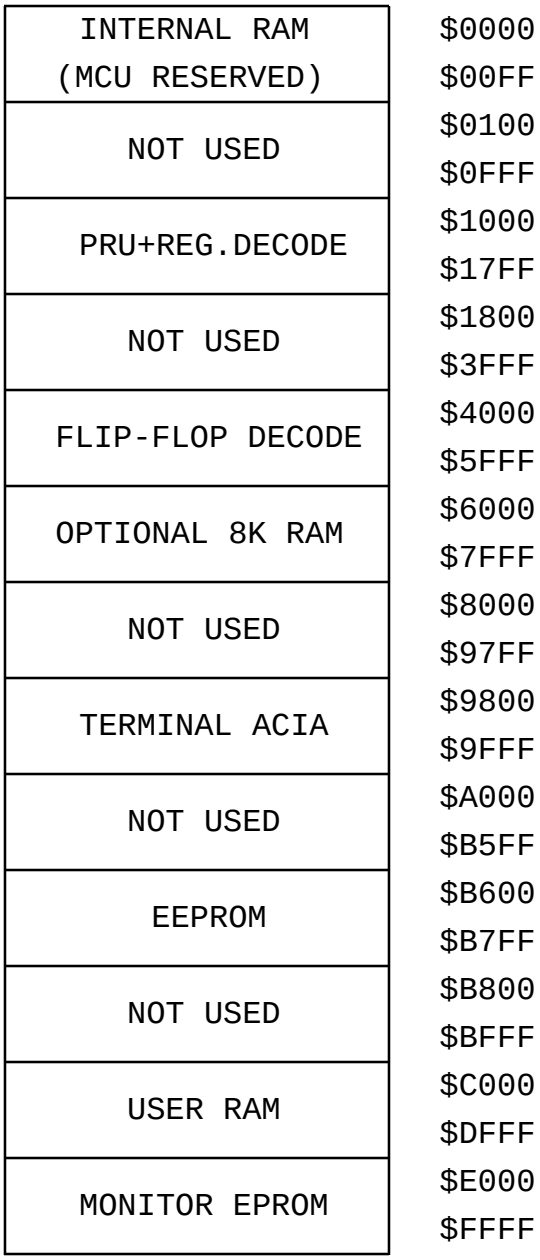


Figure 5-1. EVB Block Diagram



$0000-$0032 USER RAM
$0033-$0047 USER STACK POINTER
$0048-$00C3 MONITOR VARIABLES
$00C4-$00FF VECTOR JUMP TABLE

Figure 5-2. EVB Memory Map Diagram

5.2.3 Memory

The EVB memory map is a single map design. User RAM resides at different address locations to that of the MCU ROM. Any code debugged in the RAM which is not re-locatable will require modification before being transferred to EPROM and executed instead of the monitor (evaluation mode).

To evaluate programs normally held in ROM, an 8k byte RAM is provided (socket U5). An access time of 250 nanoseconds is necessary for a bus frequency of 2.1 MHz. Jumper headers J3 and J7 configure socket U4 for an additional 8k byte RAM supplied by the user if required. Refer to paragraph 2.3.3 for additional memory select information.

5.2.4 Address Decoding/De-multiplexing

Address decoding is accomplished via a MC74HC138 device (U6) and is segmented into 8k byte blocks. The low order address and data lines are de-multiplexed using a MC74HC373 device (U2), to communicate with ROM, RAM, and the ACIA. The PRU uses a multiplexed input direct from the MCU.

5.2.5 RS-232C I/O Port Interface Circuits

The EVB uses an MC68B50 ACIA device (U9) to communicate to a terminal via an RS-232C driver/receiver interface (terminal I/O port). The terminal I/O port baud rate is hardware selectable (300-9600 baud) via jumper header J5.

A second RS-232C driver/receiver interface (host I/O port) is fixed at 9600 baud via the MCU SCI using a 2 MHz E clock external bus. This baud rate can be changed by software by reprogramming the BAUD register in the ONSCI subroutine of the BUFFALO monitor program. Refer to the buf25.asm file on the EVB diskette for additional information pertaining to the ONSCI subroutine.

The host I/O port is provided for downloading Motorola S-records via the BUFFALO monitor commands. When using the host I/O port, either by executing the HOST or LOAD commands, The target system Serial Communications Interface (SCI) is switched to the host I/O port via the MC74HC4066 digital switch device (U7) and MC74HC74 latch device (U11). The receiver connection from the host I/O port is now connected to the RXD port of the MCU. The switching of the receiver line from the target system to the host I/O port is accomplished by writing a logic one in the bit 0 to any address in the range $4000-$5FFF. Likewise, writing a zero in bit 0 to any address in the same range results in the target system being connected to the RXD pin of the MCU.

As the RS-232C handshake lines are not used, a delay of approximately 300 milliseconds is present between successive characters sent to the host computer during the execution of the LOAD command in the monitor program.

CHAPTER 6
SUPPORT INFORMATION

6.1 INTRODUCTION

This chapter provides the connector signal descriptions, parts list with associated parts location diagram, and schematic diagrams for the EVB.

6.2 CONNECTOR SIGNAL DESCRIPTIONS

The EVB provides one input/output (I/O) connector that is used to interconnect the EVB to a target system. Connector P1 facilitates this interconnection.

Connectors P2 and P3 are also provided to facilitate interconnection of a terminal and a host computer, respectively. Connector P4 interconnects an external power supply to the EVB.

Pin assignments for the above connectors (P1 through P4) are identified in Tables 6-1 through 6-4, respectively. Connector signals are identified by pin number, signal mnemonic, and signal name and description.

Table 6-1. MCU I/O Port Connector (P1) Pin Assignments

Pin Number	Signal Mnemonic	Signal Name and Description
1	GND	Ground
2	MODB	MODE B - An input control line used for MCU mode selection. A high level enables the expanded multiplexed mode, and a low level enables the special test mode of the EVB MCU.
3	MODA	MODE A - An input control line used for MCU mode selection during reset. An open-drain output line used for LIR* status indication.
4	STRA	STROBE A - An input control line used for parallel port I/O operations.
5	E	ENABLE CLOCK - An output control line used for timing reference. E clock frequency is one fourth the frequency of the XTAL and EXTAL pins.
6	STRB	STROBE B - An output control line used for parallel port I/O operations.
7	EXTAL	EXTAL - External MCU clock input line.
8	XTAL	XTAL - Internal MCU clock line used to control the EVB clock generator circuitry.
9-16	PC0-PC7	PORT C (bits 0-7) - General purpose I/O lines.
17	RESET*	RESET - An active low bi-directional control line used to initialize the MCU.
18	XIRQ*	X INTERRUPT REQUEST - An active low input line used to request asynchronous non-maskable interrupts to the MCU.

Table 6-1. MCU I/O Port Connector (P1) Pin Assignments (continued)

Pin Number	Signal Mnemonic	Signal Name and Description
19	IRQ*	INTERRUPT REQUEST – An active low input line used to request asynchronous interrupts to the MCU.
20 21 22 23 24 25	PD0 PD1 PD2 PD3 PD4 PD5	PORT D (bits 0-5) – General purpose I/O lines. These lines can be used with the MCU Serial Communications Interface(SCI) and Serial Peripheral Interface(SPI).
26	VDD	VDD – +5.0 Vdc power.
27-34	PA7-PA0	PORT A (bits 7-0) – General purpose I/O lines.
35-42	PB7-PB0	PORT B (bits 7-0) – General purpose output lines.
43 44 45 46 47 48 49 50	PE0 PE4 PE1 PE5 PE2 PE6 PE3 PE7	PORT E (bits 0-7) – General purpose input or A/D channel input lines.
51	VRL	VOLTAGE REFERENCE LOW - Input reference supply voltage (low) line for the MCU analog-to-digital (A/D) converter. Used to increase accuracy of the A/D conversion.
52	VRH	VOLTAGE REFERENCE HIGH - Input reference supply voltage (high) line. Same purpose as pin 51.
53-60	NC	Not connected.

Table 6-2. Terminal I/O Port Connector (P2) Pin Assignments

Pin Number	Signal Mnemonic	Signal Name and Description
1	GND	PROTECTIVE GROUND
2	RXD	RECEIVED DATA - Serial data input line.
3	TXD	TRANSMITTED DATA - Serial data output line.
4	NC	Not connected.
5	CTS	CLEAR TO SEND - An output signal used to indicate ready-to-transfer data status. This pin is connected to both DSR pin 6 and DCD pin 8.
6	DSR	DATA SET READY - An output signal used to indicate an on-line/in-service/active status. This pin is connected to both CTS pin 5 and DCD pin 8.
7	SIG-GND	SIGNAL GROUND - This line provides signal ground or common return connection (common ground reference) between the EVB and RS-232C compatible terminal.
8	DCD	DATA CARRIER DETECT - An output signal used to indicate an acceptable received line (carrier) signal has been detected. This pin is connected to both CTS pin 5 and DSR pin 6.
9-19	NC	Not connected.
20	DTR	DATA TERMINAL READY - An input line used to indicate an on-line/in-service/active status.
21-25	NC	Not connected.

Table 6-3. Host I/O Port Connector (P3) Pin Assignments

Pin Number	Signal Mnemonic	Signal Name and Description
1	GND	PROTECTIVE GROUND
2	RXD	RECEIVED DATA - Serial data output line.
3	TXD	TRANSMITTED DATA - Serial data input line.
4, 5	NC	Not connected.
6	DSR	DATA SET READY - An output signal used to indicate an on-line/in-service/active status. This pin is connected to DCD pin 8.
7	SIG-GND	SIGNAL GROUND - This line provides signal ground or common return connection (common ground reference) between the EVB and RS-232C compatible host computer.
8	DCD	DATA CARRIER DETECT - An output signal used to indicate an acceptable received line (carrier) signal has been detected. This pin is connected to DSR pin 6.
9-19	NC	Not connected.
20	DTR	DATA TERMINAL READY - An input line used to indicate an on-line/in-service/active status.
21-25	NC	Not connected.

Table 6-4. Input Power Connector (P4) Pin Assignments

Pin Number	Signal Mnemonic	Signal Name and Description
1	-12 V	-12 Vdc Power - Input voltage (-12 Vdc @ 0.1 A) used by the EVB logic circuits.
2	GND	GROUND
3	+5 V	+5 Vdc Power - Input voltage (+5 Vdc @ 0.5 A) used by the EVB logic circuits.
4	+12 V	+12 Vdc Power - Input voltage (+12 Vdc @ 0.1 A) used by the EVB logic circuits.

6.3 PARTS LIST

Table 6-5 lists the components of the EVB by reference designation order. The reference designation is used to identify the particular part on the parts location diagram (Figure 6-1) that is associated with the parts list table. This parts list reflects the latest issue of hardware at the time of printing.

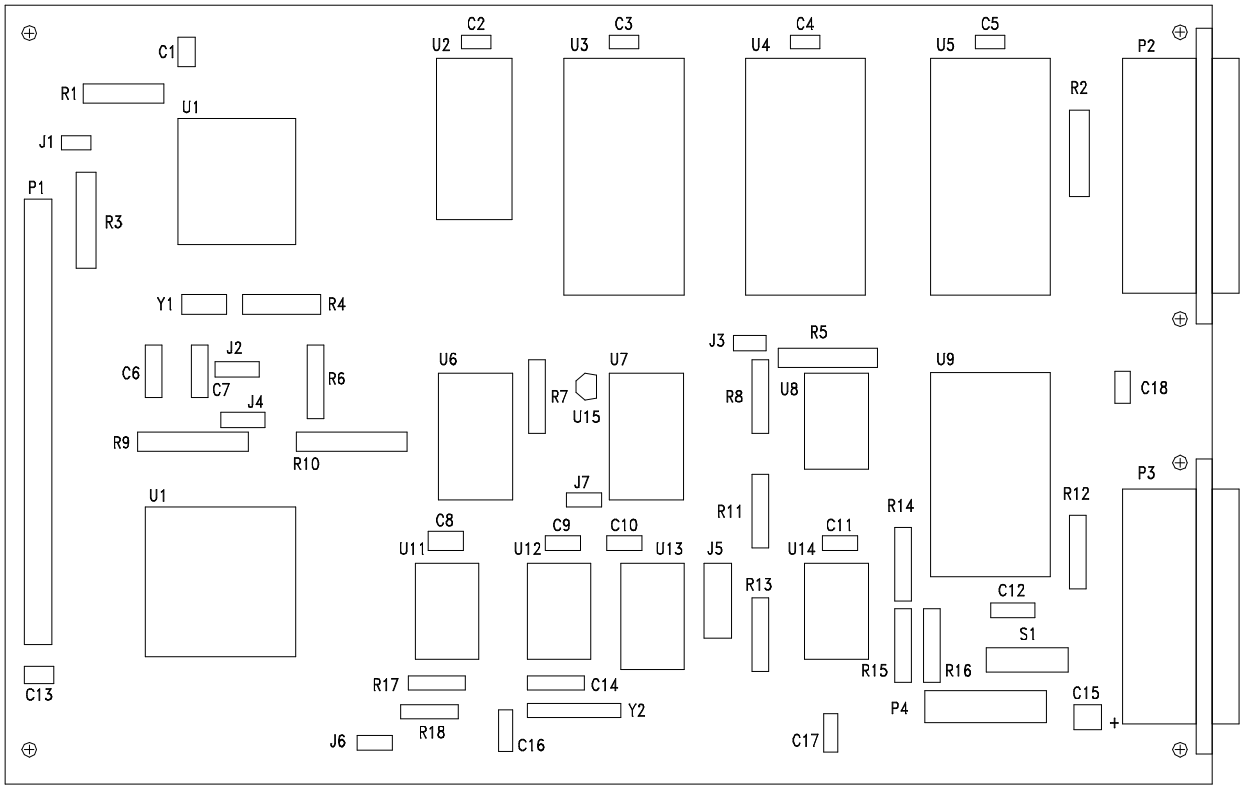


Figure 6-1. EVB Parts Location Diagram

Table 6-5. EVB Parts List

Reference Designation	Component Description
Printed Wiring Board (PWB)	M68HC11EVB
C1-C5, C8-C11, C13, C14, C17, C18	Capacitor, 0.1 uF @ 50 Vdc, +/-20%
C6, C7, C16	Capacitor, 24 pF @ 50 Vdc, +/-20%
C12	Capacitor, 1.0 uF @ 50 Vdc, +/-20%
C15	Capacitor, electrolytic, 100 uF @ 50 Vdc, +/-20%
J1, J3, J6	Header, jumper, single row post, 2 pin, Aptronics # 929705-01-02
J2, J4	Header, jumper, single row post, 3 pin, Aptronics # 929705-01-03
J5	Header, jumper, double row post, 12 pin, Aptronics # 929715-01-06
P1	Header, double row post, 60 pin, Aptronics # 929715-01-30 (MCU I/O port connector)
P2, P3	Connector, cable, 25-pin, ITT # DBP-25SAA (terminal/host I/O port connector)
P4	Terminal block, 4 position, Electrovert # 25.112.0453 (power supply connector)
R1-R3, R5-R10	Resistor, 10k ohm, 5%, 1/4W
R4	Resistor, 10M ohm, 5%, 1/4W
R11, R13-R15	Resistor, 27k ohm, 5%, 1/4W
R12	Resistor, 620 ohm, 5%, 1/4W

Table 6-5. EVB Parts List (continued)

Reference Designation	Component Description
R16	Resistor, 100k ohm, 5%, 1/4W
R17, R18	Resistor, 2.2k ohm, 5%, 1/4W
S1	Switch, push-button, SPDT, C&K #8125-R2/7527
U1	I.C., MC68HC24FN, PRU
U2	I.C., MC74HC373N, transparent latch
U3	I.C., 2764, 8k EPROM, 250 nS
U4	I.C., MCM6164, 8k RAM (user supplied)
U5	I.C., MCM6164, 8k RAM, 250 nS
U6	I.C., MC74HC138, decoder/de-multiplexer
U7	I.C., MC74HC4066/MC14066B, digital switch
U8	I.C., MC1488P, RS-232C driver
U9	I.C., MC68B50P, ACIA
U10	I.C., MC68HC11A1FN, MCU (Note 1)
U11	I.C., MC74HC74, D-type flip-flop
U12	I.C., MC74HC14, inverter
U13	I.C., MC74HC4040, binary ripple counter
U14	I.C., MC1489P, RS-232C receiver
U15	Voltage detector, 3.80-4.20 Vdc, Motorola #MC34064P or Seiko # S-8054HN
XU1	Socket, PC mount, 44 pin, PLCC, AMP # 821-551-1 (use with U1)

Table 6-5. EVB Parts List (continued)

Reference Designation	Component Description
XU3-XU5	Socket, 28 pin, DIP, Robinson Nugent # ICL-286-S7-TG (use with U3-U5)
XU9	Socket, 24 pin, DIP, Robinson Nugent # ICL-246-S7-TG (use with U9)
XU10	Socket, PC mount, 52 pin, PLCC, AMP # 821-575-1 (use with U10)
Y1	Crystal, MCU, 8.0 MHz (Notes 2 & 3)
Y2	Crystal, ACIA, 2.4576 MHz
Fabricated jumper	Aptronics # 929955-00 (use with jumper headers J1-J6)

NOTES

1. MCU supplied with the EVB have the configuration (CONFIG) register ROMON bit cleared to disable MCU internal ROM, thereby allowing external EPROM containing the BUFFALO program to control EVB operations.
2. Crystal frequencies from 4 to 8 MHz (up to 8.4 MHz) can be used without any changes to the 24 pF capacitors (C6 and C7) and 10M ohm resistor (R5) values.
3. 8 MHz crystal obtains 2 MHz E-clock/9600 baud MCU SCI operation. 4 MHz crystal obtains 1 MHz E-clock/4800 baud MCU SCI operation.

6.4 DIAGRAMS

Figure 6-2 is the EVB schematic diagram.

NOTES:

1. UNLESS OTHERWISE SPECIFIED:

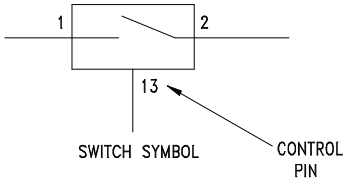
   ALL RESISTORS ARE IN OHMS, ±5%, 1/4W.
   ALL CAPACITORS ARE IN uF.
   ALL VOLTAGES ARE DC.

2. DEVICE TYPE NUMBERS LISTED BELOW ARE FOR REFERENCE ONLY. DEVICE TYPE NUMBER VARIES WITH MANUFACTURER.

REF DES	DEVICE TYPE	NOTES	GND	+5V	+12V	−12V
U1	MC68HC24	PRU	29	17		
U2	MC74HC373	TRANSPARENT LATCH	10	20		
U3	2764	8K EPROM (250ns)	14	28		
U4	(USER SUPPLIED)	8K RAM (250ns)	14	28		
U5	MCM6164	8K RAM (250ns)	14	28		
U6	MC74HC138	DECODER/DEMUX	8	16		
U7	MC74HC4066	DIGITAL SWITCH	7	14		
U8	MC1488P	RS−232C DRIVER	7		14	1
U9	MC68B50P	ACIA	1	12		
U10	MC68HC11A1	MCU	1	26		
U11	MC74HC74	D−TYPE FLIP−FLOP	7	14		
U12	MC74HC14	INVERTER	7	14		
U13	MC74HC4040	RIPPLE COUNTER	8	16		
U14	MC1489P	RS−232C RECEIVER	7			

3 DIGITAL SWITH U7 OPERATES AS FOLLOWS:

CONTROL PINS (5, 6, 12, OR 13)	SWITCH OPERATION
LOGIC ZERO (0)	OFF/OPEN
LOGIC ONE (1)	ON/CLOSED



4. NOT USED DEVICE.

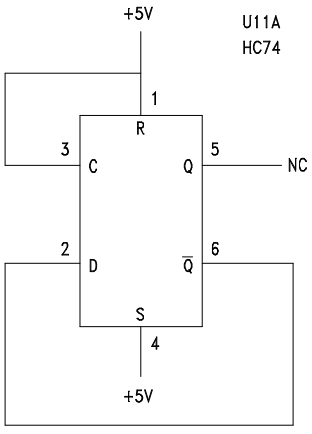


Figure 6-2. EVB Schematic Diagram (Sheet 1 of 2)

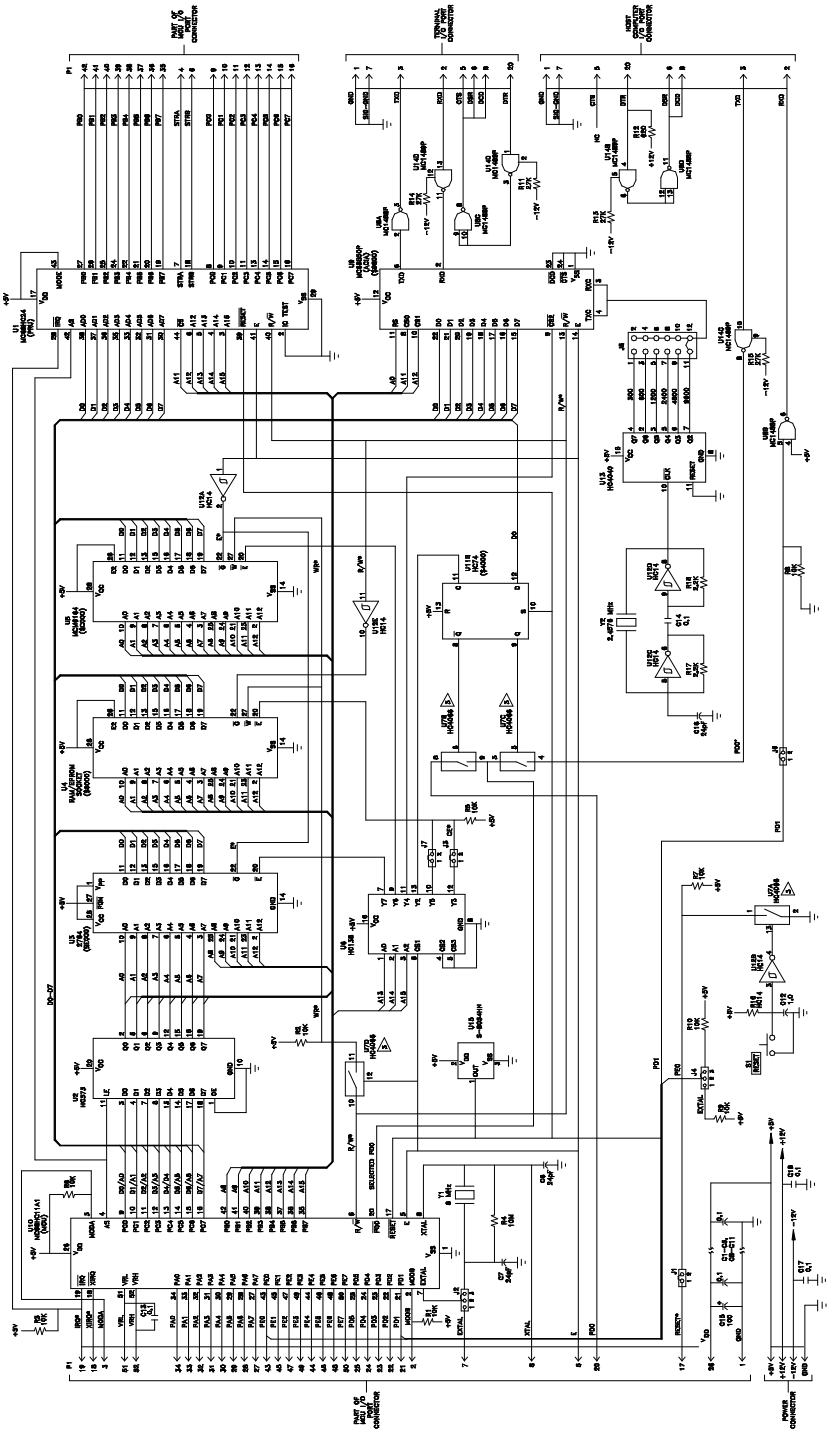


Figure 6-2. EVB Schematic Diagram (Sheet 2 of 2)