SGS-THOMSON MICROELECTRONICS

M54HC590
M74HC590

8-BIT BINARY COUNTER REGISTER (3-STATE)

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS (For RCO)
  15 LSTTL LOADS (For QA ~ QH)
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.) For QA ~ QH Output
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN) For RCO Output
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS590

B1N
Plastic Package

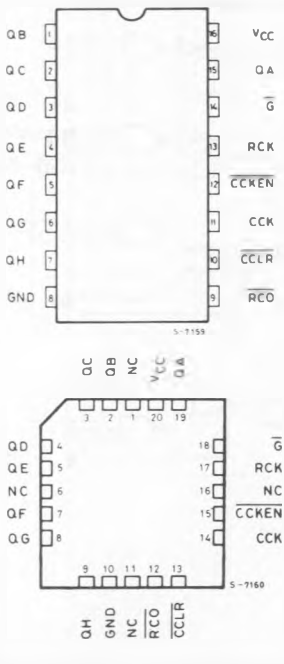
F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
M54HC590 F1
M74HC590 B1N
M74HC590 F1
M74HC590 C1
M74HC590 M1

PIN CONNECTION (top view)



NC = No Internal Connection

DESCRIPTION

The M54/74HC590 is a high speed CMOS 8-BIT BINARY COUNTER REGISTER (3-STATE) fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
These devices each contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features a direct clear input $\overline{CCLR}$ and a count enable input $\overline{CCKEN}$. For cascading, a ripple carry output $\overline{RCO}$ is provided. Expansion is easily accomplished by tying $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage, etc. Both the counter and register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register. Internal circuitry prevents clocking from the clock enable. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

TRUTH TABLE

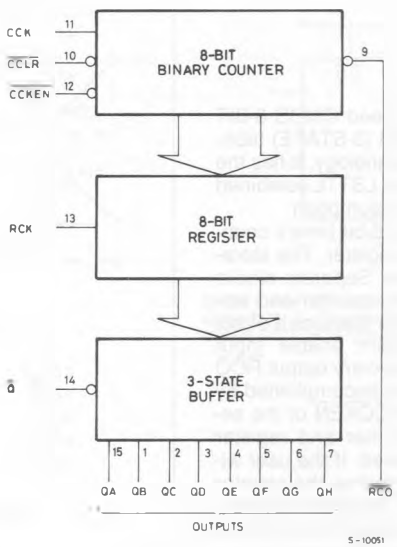
INPUTS					FUNCTION
$\overline{G}$	RCK	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	
H	X	X	X	X	Q OUTPUTS DISABLE
L	X	X	X	X	Q OUTPUTS ENABLE
X	↑	X	X	X	COUNTER DATA IS STORED INTO REGISTER.
X	↓	X	X	X	REGISTER STATE IS NOT CHANGED.
X	X	L	X	X	COUNTER CLEAR
X	X	H	L	↑	ADVANCE ONE COUNT
X	X	H	L	↓	NO COUNT
X	X	H	H	X	NO COUNT

X: DON'T CARE

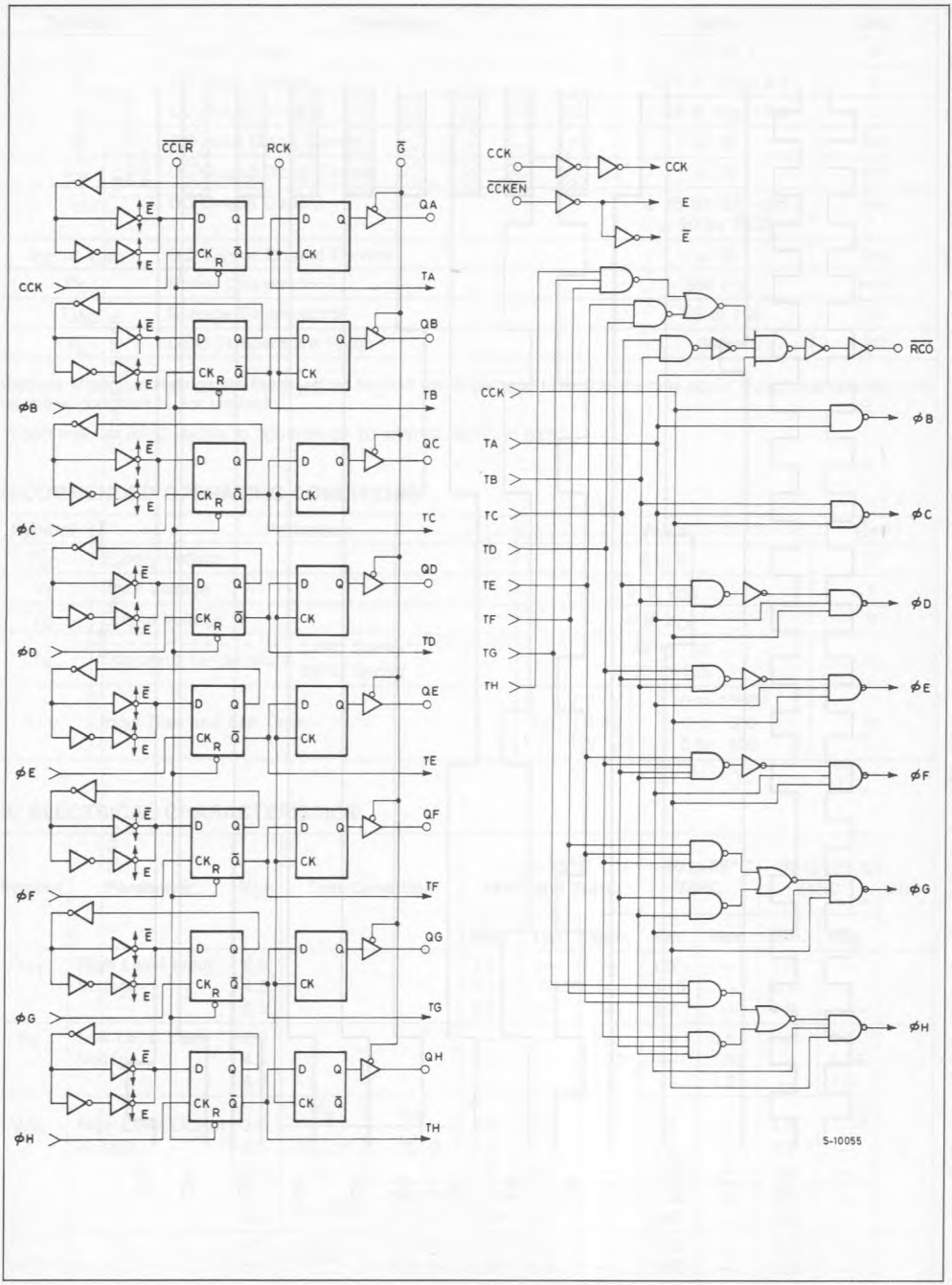
$\overline{RCO} = \overline{QA' \cdot QB' \cdot QC' \cdot QD' \cdot QE' \cdot QF' \cdot QG' \cdot QH'}$

(QA' ~ QH': INTERNAL OUTPUTS OF THE COUNTER)

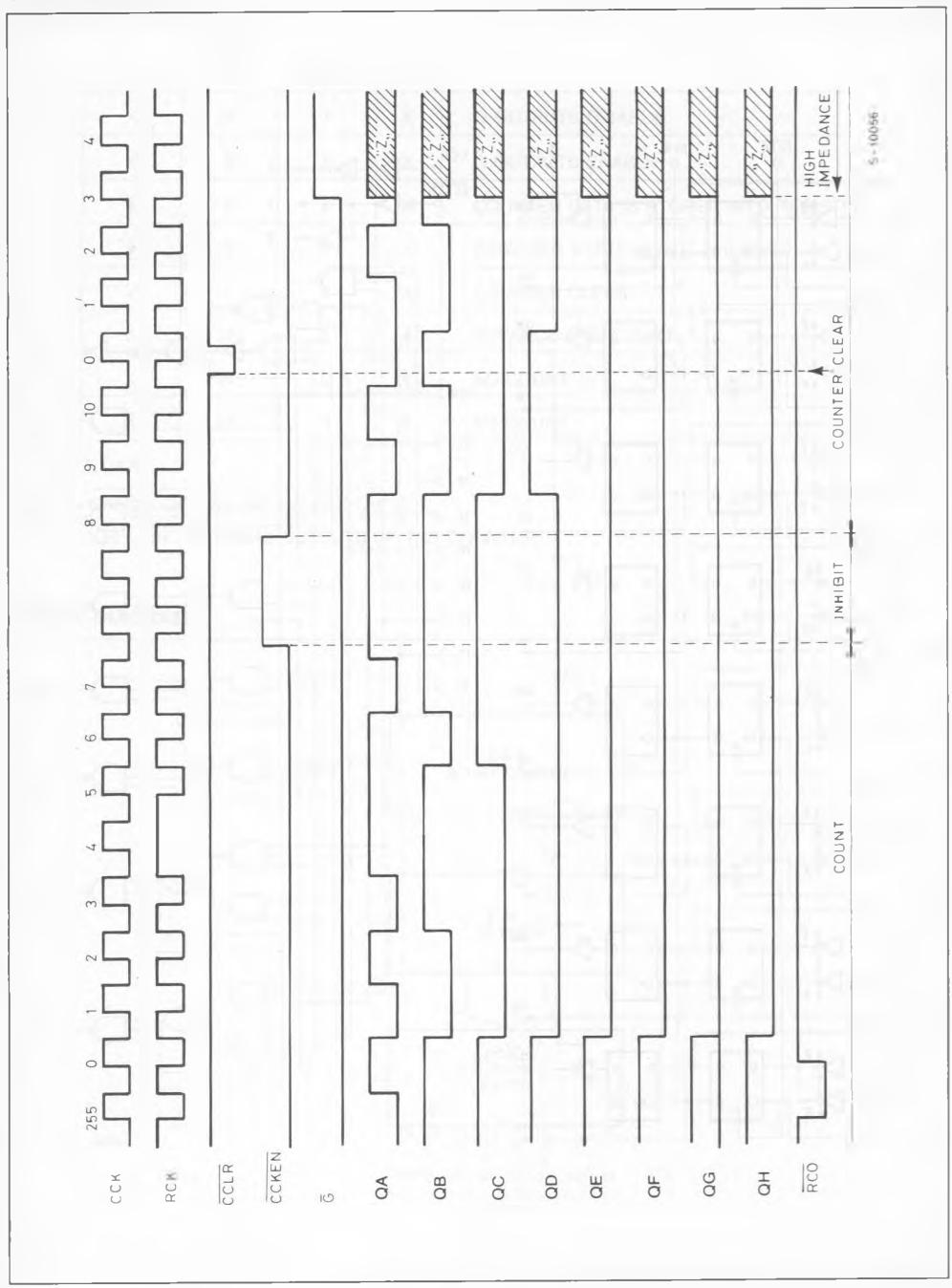
BLOCK DIAGRAM



LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 35 for QA ~ QH ± 20 for $\overline{RCO}$	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C
T_L	Lead Temperature 10sec	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_{IN}	I_{OH}	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5	Q_A ~ Q_H	−6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−7.8 mA	5.68	5.8	—	5.63	—	5.60	—	
		4.5	$\overline{RCO}$	−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OL}	Low Level Output Voltage	2.0	V_I	I_O	—	0.0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5	$Q_A \sim Q_H$	6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		7.8 mA	—	0.18	0.26	—	0.33	—	0.40	
		4.5	$\overline{RCO}$	4.0 mA		0.17	0.26	—	0.33	—	0.40	—
		6.0		5.2 mA		0.18	0.26	—	0.33	—	0.40	—
I_{OZ}	3-State Output Off-State Current	6.0	$V_{OUT} = V_{CC}$ or GND		—	—	±0.5	—	±5.0	—	±10	μA
I_{IN}	Input Leakage Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (Q Outputs)	2.0		—	25	60	—	75		90	ns
		4.5		—	7	12	—	15		18	
		6.0		—	6	10	—	13		15	
t_{TLH} t_{THL}	Output Transition Time ($\overline{RCO}$)	2.0		—	30	75	—	95		110	
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CCK - $\overline{RCO}$)	2.0		—	124	240	—	300		360	
		4.5		—	31	48	—	60		72	
		6.0		—	26	41	—	51		61	
t_{PLH}	Propagation Delay Time (CCLR-$\overline{RCO}$)	2.0		—	104	200	—	250		300	
		4.5		—	26	40	—	50		60	
		6.0		—	22	34	—	43		51	
t_{PLH} t_{PHL}	Propagation Delay Time (RCK-Q)	2.0		—	92	180	—	225		270	
		4.5		—	23	36	—	45		54	
		6.0		—	20	31	—	38		46	
f_{MAX}	Maximum Clock Frequency	2.0		4	8	—	3	—	2.6	—	MHz
		4.5		20	32	—	16	—	13	—	
		6.0		24	38	—	19	—	15	—	
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CCK, RCK)	2.0		—	48	125	—	155		190	ns
		4.5		—	12	25	—	31		38	
		6.0		—	10	21	—	26		32	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CCLR}$)	2.0		—	92	200	—	250		300	ns
		4.5		—	23	40	—	50		60	
		6.0		—	20	34	—	43		51	

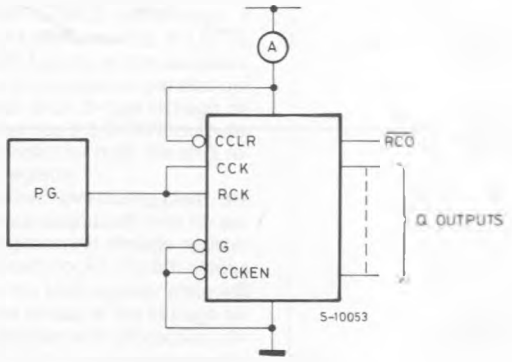
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{rem}	Minimum Removal Time ($\overline{CLEAR}$)	2.0		—	—	5	—	5	—	5	ns
		4.5		—	—	5	—	5	—	5	
		6.0		—	—	5	—	5	—	5	
t_s	Minimum Set-up Time ($\overline{CCKEN}$-CCK)	2.0		—	40	100	—	125	—	150	
		4.5		—	10	20	—	25	—	30	
		6.0		—	9	17	—	21	—	26	
t_s	Minimum Set-up Time (CCK, RCK)	2.0		—	128	245	—	305	—	370	
		4.5		—	32	49	—	61	—	74	
		6.0		—	27	42	—	52	—	63	
t_h	Minimum Hold Time	2.0		—	—	5	—	5	—	5	
		4.5		—	—	5	—	5	—	5	
		6.0		—	—	5	—	5	—	5	
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0	$R_L = 1K\Omega$	—	68	135	—	170	—	205	
		4.5		—	17	27	—	34	—	41	
		6.0		—	14	23	—	29	—	35	
t_{PLZ} t_{PHZ}	3-State Output Disable Time	2.0	$R_L = 1K\Omega$	—	88	155	—	195	—	235	
		4.5		—	22	31	—	39	—	47	
		6.0		—	19	26	—	33	—	40	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD}(1)	Power Dissipation Capacitance			—	95	—	—	—	—	—	

Note (1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

Average operating current can be obtained by the following equation: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

TEST WAVEFORM I_{CC} (Opr.)



SWITCHING CHARACTERISTICS TEST WAVEFORM