19-2886; Rev 0; 5/92

MAXIM

-48V to +5V Output Switching DC-DC Converter

General Description

The MAX650 is a low-power fixed +5V output switching DC-DC converter designed for operation from very high negative input voltages. All control functions and a 140V, 250mA PNP transistor are contained in this device, reducing external components. A soft-start eliminates overshoot on turn on, and a Shutdown pin (SHDN) allows the output to be turned on and off. In addition, peak current limiting is provided on the PNP output.

The MAX650 features user-controllable operating frequency and a separate low voltage detector with adjustable hysteresis for monitoring the supply voltage. It can be set to trip at any negative voltage with a simple voltage divider.

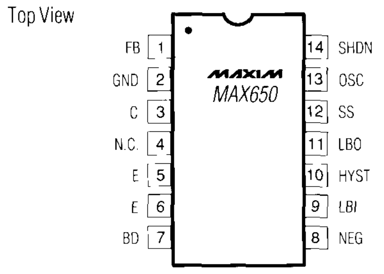
The MAX650 is available in an A version with ±5% output voltage tolerance and a B version with ±10% tolerance.

Applications

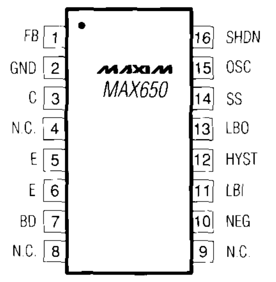
Telephone (-48V) Powered Devices

Negative Input to +5V Converter

Pin Configurations



DIP



SO

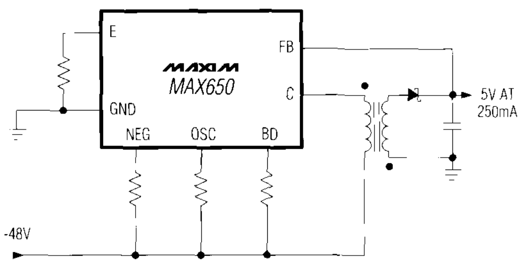
Features

- ◆ **+5V at 250mA From a -48V Source**
- ◆ **Selectable Soft-Start Function**
- ◆ **Shutdown Pin for Output On-Off Control**
- ◆ **Internal 140V, 250mA Switching PNP Transistor**
- ◆ **Low Component Count**
- ◆ **Low Battery Voltage Detector**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX650ACPD	0°C to +70°C	14 Plastic DIP
MAX650ACWE	0°C to +70°C	16 Wide SO
MAX650AC/D	0°C to +70°C	Dice
MAX650BCPD	0°C to +70°C	14 Plastic DIP
MAX650BCWE	0°C to +70°C	16 Wide SO
MAX650BC/D	0°C to +70°C	Dice
MAX650AEPD	-40°C to +85°C	14 Plastic DIP
MAX650AEWE	-40°C to +85°C	16 Wide SO
MAX650BEPD	-40°C to +85°C	14 Plastic DIP
MAX650BEWE	-40°C to +85°C	16 Wide SO
MAX650AMJD	-55°C to +125°C	14 Ceramic DIP
MAX650BMJD	-55°C to +125°C	14 Ceramic DIP

Typical Operating Circuit



-48V to +5V Output Switching DC-DC Converter

ABSOLUTE MAXIMUM RATINGS

(Unless otherwise noted, all voltages are referenced to the GND terminal.)

Collector (C) Current, I_C	-300mA
Collector (C) Voltage, V_C	-140V
Emitter (E) Voltage, V_E	-1V to +0.3V
Base BD Current, I_{BD}	-50mA
FB Voltage, V_{FB}	+7V
LBI, SS and SHDN Currents	±10mA
LBO Voltage, V_{LBO}	(V_{NEG} -0.3) to (V_{NEG} +15) V
Voltage at OSC, BD, HYST, LBI, SS, and SHDN	(V_{NEG} -0.3) to 0V
NEG Current, I_{NEG}	-25mA
OSC Current, I_{OSC}	±10mA
LBO Sink Current, I_{LBO}	-10mA
HYST Source Current, I_{HYST}	±10mA
Power Dissipation	
Plastic DIP (derate 6.5mW/°C above 25°C)	470mW
Small Outline (derate 10mW/°C above 75°C)	750mW
CERDIP (derate 11mW/°C above 75°C)	825mW
Operating Temperature	
MAX650C_	0°C to +70°C
MAX650E_	-40°C to +85°C
MAX650M_	-55°C to +125°C
Storage Temperature	-65°C to +160°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(GND = 0V, T_A = +25°C, unless otherwise noted. MIN and MAX values are based on magnitude without regard to sign.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output (load) Voltage	V_{FB}	T_A = Full MAX650A MAX650B	 +4.75 +4.5	 +5 +5	 +5.25 +5.5	V
Feedback Input Current	I_{FB}	V_{FB} = +5V		40	100	µA
Internal Zener Voltage	V_{NEG}	T_A = Full, I_{NEG} = -500µA	-6	-7	-8	V
Internal Zener Current	I_{NEG}	T_A = Full	-0.3	-0.5	-10	mA
Current Sense Voltage	V_E		-140	-175	-210	mV
Peak Collector Current	I_C				-250	mA
Collector Leakage Current	I_C	T_A = Full, V_C = -140V		0.1	10	mA
Collector (C) Saturation Voltage	V_{SAT}	T_A = Full, I_C = -250mA, I_{BD} = -25mA			-4	V
PNP Current Gain	H_{FE}	T_A = Full, $V_C \leq$ -4V I_C = -100mA I_C = -250mA	 20 10	 80 13		
Switching Frequency	F_O	I_{OSC} = -12µA T_A = +25°C T_A = Full	 17 15	 20	 23 25	kHz
Oscillator Input Voltage	V_{OSC}	I_{OSC} = -12µA		-2		V
Oscillator Input Current	I_{OSC}		-4	-12	-100	µA
Switching Duty Cycle	%ON	SS = Open Circuit SS = GND	48 24	53 27	65 33	%
Low Battery Input Threshold	V_{LBI}	T_A = Full	V_{NEG}+0.13	V_{NEG}+0.08	V_{NEG}+0.03	V
Low Battery Input Current	I_{LBI}	T_A = Full		0.1	±100	nA
Soft-Start Input Threshold	V_{SS}		-3	-4.5	-5	V
Soft-Start Input Current	I_{SS}				-10	µA
Shutdown Input Threshold	V_{SHDN}		-3	-4.5	-5	V
Shutdown Input Current	I_{SHDN}	0V > V_{SHDN} > -3V			-10	µA

Pin Description

PIN # 14-PIN DIP	PIN # 16-PIN Wide SO	NAME	FUNCTION
1	1	FB	Feedback Input. The 5V output is connected to FB, which regulates the output voltage. This input sinks approximately 40µA to V_{NEG}.
2	2	GND	Ground. This is the positive side of the -48V input supply and the negative side of the +5V output. All specified voltages are referenced to this pin.
3	3	C	Output (collector) of the PNP transistor switch. Connect to the transformer primary. This pin can withstand up to -140V on the flyback cycle and sources up to 250mA from E, depending on the base drive current at BD.
4	4, 8, 9	N.C.	No Connection. These pins are open circuit.
5, 6	5, 6	E	Current sense input (emitter) of PNP transistor. Connect to GND, either directly or through a low-value sense resistor. When the voltage on these pins is more negative than -175mV, the PNP transistor is turned off for an entire cycle.
7	7	BD	Base Drive Input of PNP transistor. Figure 1.
8	10	NEG	Negative Power Connection. Anode of 7V Zener diode whose cathode is connected to GND. An external series limiting resistor is required between this pin and the -48V input supply. This resistor must also sink the LBO current (up to 100µA).
9*	11*	LBI*	Low Battery Monitor Input. CMOS input.
10*	12*	HYST*	Low Battery Monitor Hysteresis Output. This P-channel FET sources up to 80µA to GND when the LBI input is 80mV more positive than V_{NEG}; otherwise HYST is an open circuit.
11	13	LBO	Low Battery Monitor Output. Sinks up to 100µA to NEG when LBI is 80mV more positive than V_{NEG}.
12*	14*	SS*	Soft-Start Input. Normally left open circuit for 50% duty cycle. Connect to GND through a capacitor to change the oscillator duty cycle to 25% and reduce input current on startup.
13	15	OSC	Oscillator Frequency Control Input (Figure 2). The voltage on this pin is approximately -2V.
14	16	SHDN	Shutdown Input. Leave open circuit or connect to NEG for normal operation. Connect to GND through a 100kΩ resistor to stop oscillator and turn-off output.

* Voltage limitations on HYST, LBI, and SS terminals.

HYST, LBI, and SS should not be connected to GND. This is because protection diodes associated with these terminals will be forward biased, interfering with correct operation. If low-voltage detection is not required, LBI must be connected to NEG, and the HYST terminal left open circuit. SS may be connected to GND through a 0.1µFd, or smaller capacitor, to initiate soft-start on power up. If soft-start is not required, SS should also be connected to NEG.

Operating Principle

The MAX650 is a flyback switching converter; energy from the input supply is first transferred to the transformer core through the primary winding, then discharged from the secondary winding into the load. A typical circuit consists of a battery in series with the primary coil of a transformer, a switch, a rectifier, and a filter. (Figure 3). During the first portion of the cycle, the switch is closed, and current builds up in the primary storing energy in the form of a magnetic field in the transformer's core.

During the second portion, or "flyback" part of the cycle, the switch opens, the magnetic field collapses, and the energy stored in the core is discharged through the secondary winding into the rectifier and the load. The switch is controlled by an oscillator whose output is gated on and off by a comparator that monitors the output voltage. When the output voltage is below the comparator threshold (+5V) the switch turns on for the first half of the oscillator cycle. When the output voltage is above the comparator threshold, the switch skips an entire oscillator cycle. This "pulse-skipping" technique regulates by varying the average number of cycles over time rather than varying the duty cycle of the switch on each cycle.

Figure 4 shows the block diagram of the MAX650. PNP transistor, Q1, controls the input current to the transformer. The emitter of this transistor can be connected to GND directly or through a low-value current sense resistor. The collector of the transistor connects to the primary of the transformer. Transistor base drive is set by an external resistor connected to BD. The oscillator frequency is set by another external resistor at OSC.

A CMOS voltage comparator, for low battery or low input voltage detection, is included in the MAX650. Its input threshold voltage, LBI, is biased 80mV above the negative supply pin, NEG. The output, LBO, is an N-channel FET which sinks up to 100µA to NEG, and its drain can be connected to positive potentials above GND (up to 15V above V_{NEG}).

Circuit Details

A typical application circuit is shown in Figure 4. The basic operation is set by 4 external resistors, R_{NEG}, R_{OSC}, R_{BD}, and R_{SENSE}. Output current capability is determined by the transformer, as described later.

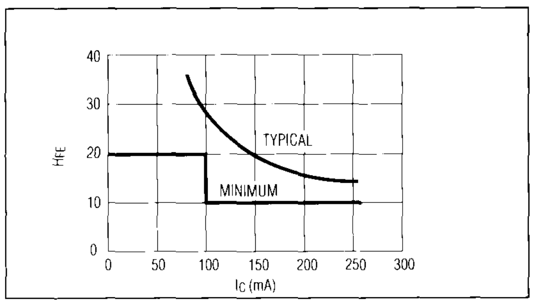


Figure 1. H_{FE} vs. Collector Current

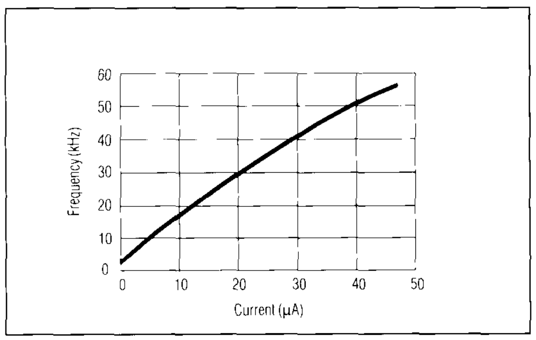


Figure 2. Oscillator Frequency vs. Oscillator Current

Supply Current, R_{NEG}

Although the MAX650 is meant to operate with high negative supply voltages (V_{IN}MIN to V_{IN}MAX), it uses approximately -7V internally. This is set by an internal 7V zener diode connected between GND and NEG. The current through this diode must be more than 300µA and less than 10mA. It is set by the size of the external voltage dropping resistor, R_{NEG}, and the supply voltage, V_{IN}MIN.

[1] $R_{NEG} = (V_{IN}MIN - V_{NEG}) / I_{NEG}$

where,

[2] $I_{NEG} = 500\mu A + I_{LBO}$

(Note that V_{IN}MIN, V_{NEG} and all currents are negative, but the calculations are simplified by using positive values.) If the low battery function is used, the LBO output sinks or furnishes load current, I_{LBO}, through the NEG pin, and this current must be added to the I_{NEG} current calculation as in Eq. 2.

Resistor, R_{NEG}, should be calculated using the lowest supply voltage, V_{IN}MIN, to insure an adequate I_{NEG} current.

Calculations for a typical application look like this:

$V_{IN}MIN = -36V$; $V_{IN}MAX = -50V$

LBO output current = -100µA

The supply resistance is calculated for the lowest supply voltage and the highest current.

[2] $I_{NEG} = 500\mu A + I_{LBO}$
$= 500\mu A + 100\mu A = 600\mu A$

[1] $R_{NEG} = (V_{IN}MIN - V_{NEG}) / I_{NEG}$
$= (36V - 7V) / 600\mu A$
$= 48{,}333\Omega$ (use 47kΩ)

With the highest input voltage, the maximum current is:

[3] $I_{NEG} = (V_{IN}MAX - V_{NEG}) / R_{NEG}$
$= (50V - 7V) / 47{,}000\Omega$
$= 915\mu A$

Oscillator Frequency, R_{OSC}

The MAX650 varies its oscillator frequency in order to keep the energy delivered to the primary of the transformer constant with varying input voltages. The oscillator frequency is a nearly linear function of the current into the OSC pin. The frequency is set by resistor, R_{OSC}, connected between OSC and the negative supply volt-

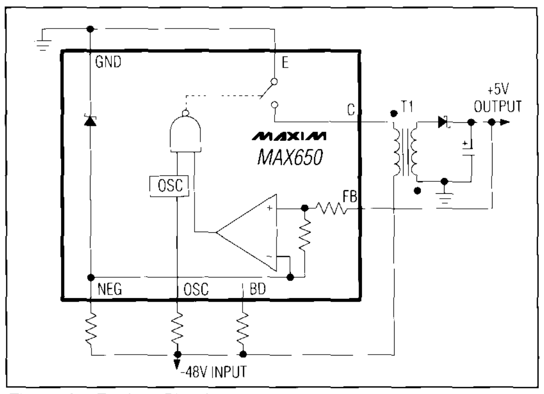
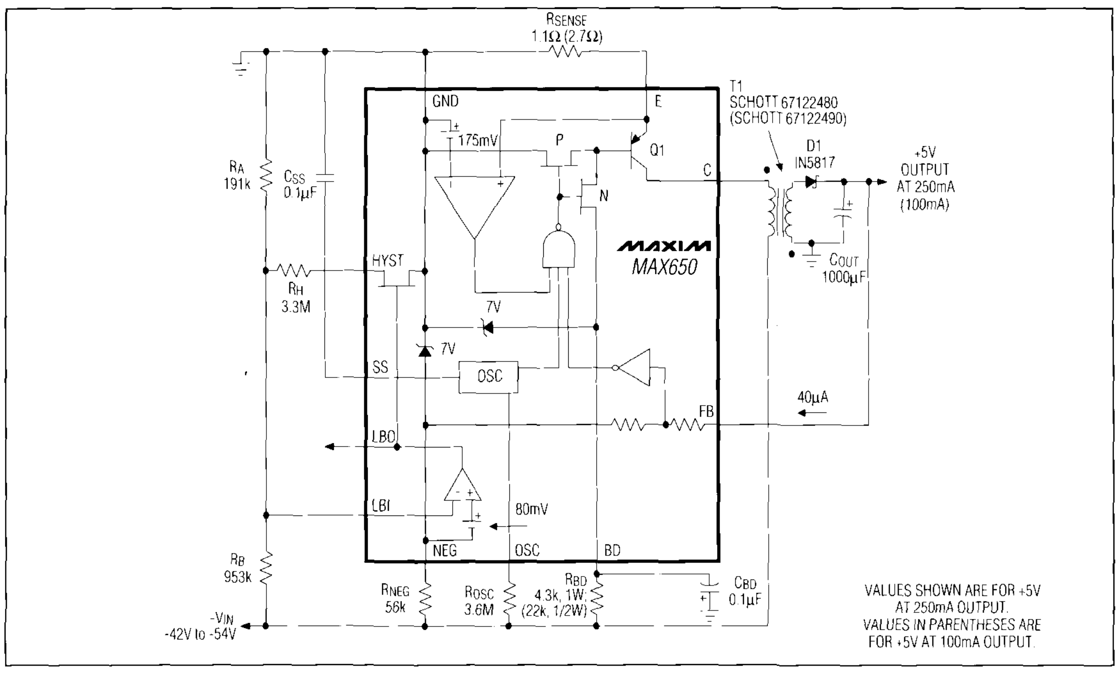


Figure 3. Typical Circuit



VALUES SHOWN ARE FOR +5V AT 250mA OUTPUT. VALUES IN PARENTHESES ARE FOR +5V AT 100mA OUTPUT.

Figure 4. Typical Application Circuit

age. Therefore, the oscillator frequency is nearly linearly proportional to the supply voltage, and the switch "on" period is inversely proportional to the supply voltage. The power stored in the primary is nearly constant with changes in supply voltage since the peak current through the switch and the primary of the transformer are proportional to the product of the "on" period of the switch and the input voltage.

Normally, the oscillator frequency is 20kHz when I_{OSC} is -12µA, as shown in Figure 2. The value of R_{OSC} is:

[4] $R_{OSC} = V_{IN}MIN / I_{OSC}$

Soft-Start

The duty cycle of the output transistor is controlled by the SS pin which has a 1µA pulldown current to the NEG pin. When the SS pin is left open or connected to NEG, soft-start is disabled and the duty cycle of the switch is approximately 50%. When it is temporarily grounded through a 0.1µFd, or smaller capacitor, the switch is on for 25% of the time and off for 75%, until the capacitor is charged to V_{NEG}. The MAX650 starts up slowly each time that power is applied and then switches over to normal operation. The soft-start circuit is shown in Figure 5. Note that the SS pin cannot be connected directly to GND.

Current Sense, R_{SENSE}

The Emitter, E, of the PNP transistor can be connected directly to GND. But, in order to protect the output transistor against destructive short-circuit currents, it should be connected to GND via a low-value current sense resistor, R_{SENSE}. An internal comparator compares the voltage generated across the sense resistor at E to an internal -175mV reference and turns off the transistor

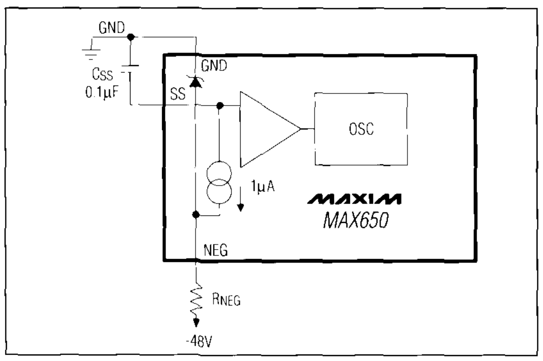


Figure 5. Soft-Start Circuit

when the peak current being switched exceeds this value. The value of R_{SENSE} is given by the formula:

[5] $R_{SENSE} = 175mV / I_{PEAK}$ (mA)

Since the maximum current that the transistor can switch is 250mA, resistors less than 0.70Ω will afford no protection. For higher values, R_{SENSE} will limit the switch current to a safe level.

Transformer

Transformer selection is governed by a number of factors. To simplify the process, Table 1 lists two transformers which have been tested with the MAX650.

The Transformer, T1, must store all of the energy that flows into the load. Accordingly, it should have a powdered iron or ferrite core, and it should have low resistance (10Ω on the primary and 0.2Ω on the secondary) to minimize losses. Small toroids or pot cores are preferred.

The transformer design is based on four values: turns ratio, frequency and duty cycle, primary inductance, and peak current. The turns ratio is calculated by dividing the maximum supply voltage by the sum of the minimum output voltage (V_{FB}) and the diode loss (V_F) and multiplying the result by 0.75 for a safety factor.

$$[6]\ \text{Turns Ratio} = \frac{0.75 \times V_{IN}MAX}{(V_{FB}MIN + \text{diode } V_F)}$$

The design works backwards from the load as follows: the diode and transformer secondary resistance losses can be lumped together as "1V" so that the maximum secondary output voltage is 6.5V. Knowing the required output current, IOUT, the Output Power, P_{OUT}, becomes:

[7] $P_{OUT} = 6.5V \times IOUT$ (Watts)

Assuming 95% efficiency in the transformer (transformer only, not the whole circuit), the input power to the primary, P_{IN} is:

$P_{IN} = 6.5V \times IOUT / 0.95$ (Watts)

[8] $P_{IN} = 6.84V \times IOUT$ (Watts)

With an oscillator frequency of 20kHz, the energy put into the coil, E_{IN}, during each "on" cycle is:

[9] $E_{IN} = P_{IN} / F_{OSC}$ (Joules)

or:

[9A] $E_{IN} = 6.84V \times IOUT / 20{,}000Hz$ (Joules)

When the switch closes, the energy builds up in the primary inductance, L, to a maximum value. This energy can also be expressed as:

[10] $E_{IN} = (V_{IN}MIN \times t_{ON})^2 / 2\,L$ (Joules)

so that the primary inductance, L, is:

[11] $L = (V_{IN}MIN \times t_{ON})^2 / 2\,E_{IN}$ (Henries)

Combining [9A] with [11], the primary inductance is:

$$[12]\quad L = \frac{(V_{IN}MIN \times t_{ON})^2}{IOUT}\ \text{(Henries)}$$

At the end of the switch "on" period (t_{ON} = 25µs for a 20kHz 50% duty-cycle switch), the current rises to a peak value, I_{PEAK}.

[13] $I_{PEAK} = V_{IN}MIN \times t_{ON} / L$ (Amperes)

I_{PEAK} must be less than 250mA to avoid exceeding the MAX650's collector current rating. When selecting the transformer, the transformer must have a peak primary current rating greater than I_{PEAK} to prevent core saturation.

In summary, set the oscillator frequency to 20kHz. The results of Equations 6, 12, and 13 determine the electrical characteristics of the transformer.

Snubbers

When the power switch opens, the primary voltage will flyback to a high negative value which depends on the leakage inductance and capacitance of the transformer. This voltage could exceed the 140V peak voltage rating of the MAX650 collector and damage it if not limited by a series R-C network, or "snubber." The snubber network is usually placed in parallel with the transformer primary, and the R-C values depend on the transformer characteristics and must be determined experimentally. 1000Ω in series with 100pF is a good starting place. The snubber does dissipate some power, reducing the overall efficiency, but this can be minimized or eliminated by using a transformer with low leakage inductance.

Larger R and smaller C values improve efficiency, but may not adequately suppress the negative spike at C. Smaller R and larger C values reduce the size of the spike, but then reduce efficiency. The optimum snubber balances these two goals.

Under ideal conditions, the snubber may be omitted. If either of the two transformers shown in Table 1 is used, the snubber is not needed.

Base Drive, R_{BD}

The output transistor, Q1, is turned on by a combination of the oscillator "on" pulse: the output voltage comparator output high, the sense comparator high, and the base drive current. The output transistor is turned off by a P-channel FET that shorts its base to GND.

In order to conserve power, the base drive current to the switching PNP transistor is set by adjusting current through the base drive pin, BD. I_{BD} is set to a value that insures that Q1 nearly saturates when it is turned on, based on the minimum beta for the output current. For example:

[14] $I_{BD} = I_{PEAK} / H_{FE}$

The H_{FE} vs. collector current is shown in Figure 1.

The base drive circuit includes a shunt zener that clamps the base drive voltage to V_{NEG} during the off period. Thus, for half of the cycle the current through BD is wasted. This loss can be recovered, however, if a 0.1µFd capacitor is placed between BD and GND. This capacitor effectively captures the lost current and makes it available for the whole cycle. More importantly, it effectively halves the required base drive current so that the base resistor is:

[15] $R_{BD} = 2 \times (V_{IN}MIN - 7V) / I_{BD}$

Note that with high current designs, R_{BD} may need to dissipate up to 600mW.

Capacitors

The output capacitor should be at least 10µF, increasing approximately 1µF/mA of output current. Low ESR capacitors, such as tantalums, are preferred. But, if aluminum electrolytics are used, each should be paralleled with a 0.1µF disk ceramic. Because of possible switching transients, 0.1µF should also be connected between NEG and GND.

Diodes

Schottky diodes are preferred for the secondary rectifier. Their low forward voltage drop and fast switching times make them the best choice for efficiency. The 1N5817 is a good example.

Low Battery Monitor

A low battery monitor with adjustable hysteresis is built into the MAX650. When LBI is connected to NEG (approximately -7V), LBO sinks up to -100µA to NEG, and the HYST pin, a P-channel FET drain, sources up to 100µA to GND. When LBI is connected to a voltage more positive than -7V, LBO and HYST outputs are open circuits. Normally LBI is connected to the negative supply via a voltage divider to GND, and a hysteresis resistor, R_H, is connected between HYST and LBI. The resistors are shown in Figure 6 and are calculated by the following formulas:

[16] $R_B = 20 \times (V_{IN}MAX - 7V)\ (k\Omega)$

[17] $R_A = \dfrac{7V \times R_B}{V_{TL} - 7V}$

Where V_{TL} is the low threshold voltage input, and $V_{IN}MAX$ is the maximum power-supply voltage. Both are positive in these calculations.

When hysteresis is used, the value of R_H, which would otherwise be open circuit, is determined by:

[18] $$R_H = \frac{R_A \times R_B \times 7V}{R_A \times (V_{TH} - 7V) - (7V \times R_B)}\ (k\Omega)$$

or:

[18A] $$R_H = \frac{V_{TL}}{(V_{TH} - V_{TL})} \times \frac{R_A \times R_B}{R_A + R_B}\ (k\Omega)$$

Where V_{TL} is the lower threshold voltage, and V_{TH} is the higher threshold voltage (again using positive values). The hysteresis is the difference between V_{TH} and V_{TL}.

Since the voltage at NEG has a range of -6V to -8V (over temperature) LBI and, thus, the higher and lower threshold voltages, cannot be set to better than ±16%.

Voltage Limitations at HYST, LBI, and SS

These three terminals may not be connected directly to GND. Connection to GND forward biases diodes associated with these terminals and interferes with the correct operation of the device. If the low voltage monitor is not

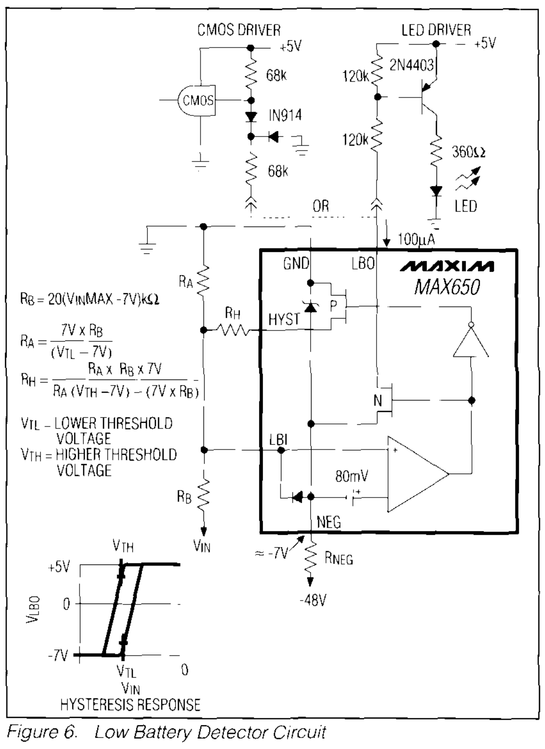


Figure 6. Low Battery Detector Circuit

required, LBI should be connected to NEG and HYST left open circuit. SS may be connected to GND through a capacitor to initiate soft start on power-up. If the soft-start function is not required, SS must be connected to NEG.

Shutdown

The SHDN trip voltage is typically -4.5V. If the function is not required, SHDN may be left open circuit or connected to NEG. The terminal has a 1µA pulldown current to NEG. To activate SHDN, this terminal may be raised positively above -4.5V and connected to GND or to a positive voltage of up to +15V with respect to NEG.

A Design Example

Figure 4 shows a complete circuit with all values. Table 1 lists the transformers that may be used to produce +5V at 250mA or 100mA. These values are derived from the following procedure, which may be adjusted for any input voltage range and output current:

$V_{IN}MIN = -42V$
$V_{IN}MAX = -54V$
$Output = +5V$ at 250mA

$V_{TL} = -42V$ (the low threshold)
$V_{TH} = -44V$ (the high threshold)
$I_{LBO} = 100\mu A$

First, set the oscillator to 20kHz with the lowest input voltage. From Figure 2, $I_{OSC} = 12\mu A$ and R_{OSC} is:

$$[4] \quad R_{OSC} = V_{IN}MIN / I_{OSC} = 42V / 12\mu A = 3.5M\Omega, \text{ use } 3.6M\Omega$$

Next, from Formula [1], calculate R_{NEG}.

$$[1] \quad R_{NEG} = (V_{IN}MIN - V_{NEG}) / I_{NEG} = (42V - 7V) / (500\mu A + 100\mu A) = 58.33k\Omega, \text{ use } 56k\Omega$$

The transformer: calculate the primary inductance using the minimum supply voltage.

$$[12] \quad L = \frac{(V_{IN}MIN \times t_{ON})^2 \times 1462}{IOUT}$$

or,

$$L = \frac{42 \times 42 \times 25 \times 25 \times 10^{-12} \times 1462}{0.25}$$

$$L = 6447\mu H = 6.5mH$$

The turns ratio should be calculated using the maximum supply voltage and the minimum output voltage, including the diode loss.

$$[6] \quad \text{Turns Ratio} = \frac{0.75 \times V_{IN}MAX}{(V_{FB}MIN + \text{diode } V_F)}$$

$$= 0.75 \times 54 / (4.5 + .4) = 40.5 / 4.9$$

$$\text{Turns Ratio} = 8.27\text{ , use } 8$$

Calculate the peak current in the primary and the transistor using the minimum input voltage again.

$$[13] \quad I_{PEAK} = V_{IN}MIN \times t_{ON} / L = 42 \times 25 \times 10^{-6} / (6500 \times 10^{-6}) = 162mA$$

From Figure 1, when $I_C = 162mA$ and $H_{FE} = 10$, and from Formula 14:

$$[14] \quad I_{BD} = I_{PEAK} / H_{FE} = .162 / 10 = 0.0162A$$

Calculate the Base Drive Resistor, R_{BD}, from Formula 15 using $V_{IN}MIN = 42V$.

$$[15] \quad R_{BD} = 2 \times (V_{IN}MIN - 7V) / I_{BD} = 2 \times (42V - 7V) / 0.0162A = 4321\Omega, \text{ use } 4.3k\Omega$$

Note that with the maximum supply voltage, the power dissipated by R_{BD} is:

$$P_{BD} = V_{BD}^2 / R_{BD} = (54 - 7)^2 / 4300 = 0.52W$$

Next, calculate value of R_{SENSE}.

$$[5] \quad R_{SENSE} = 175(mV) / I_{PEAK}(mA) = .175V / .162A = 1.08\Omega, \text{ use } 1.1\Omega$$

Last, calculate the LBI resistors.

$$[16] \quad R_B \approx 20 \times (V_{IN}MAX - 7V)\ (k\Omega) \approx 20 \times (54-7) = 940k, \text{ use } 953k\Omega$$

$$[17] \quad R_A = \frac{7V \times R_B}{V_{TL} - 7V}$$

$$= 7 \times 953k / (42 - 7) = 191k\Omega$$

$$[18] \quad R_H = \frac{R_A \times R_B \times 7}{R_A \times (V_{TH} - 7V) - (7V \times R_B)}$$

$$= \frac{191k \times 953k \times 7}{191k \times (44 - 7) - (7 \times 953k)}$$

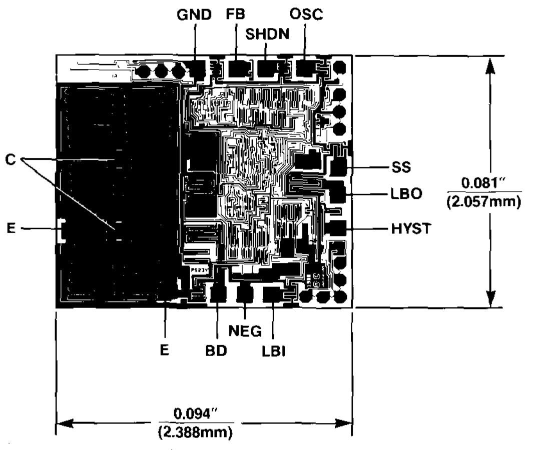
$$= 3218k, \text{ use } 3.3M$$

Table 1. Transformer and Resistor Selection Guide

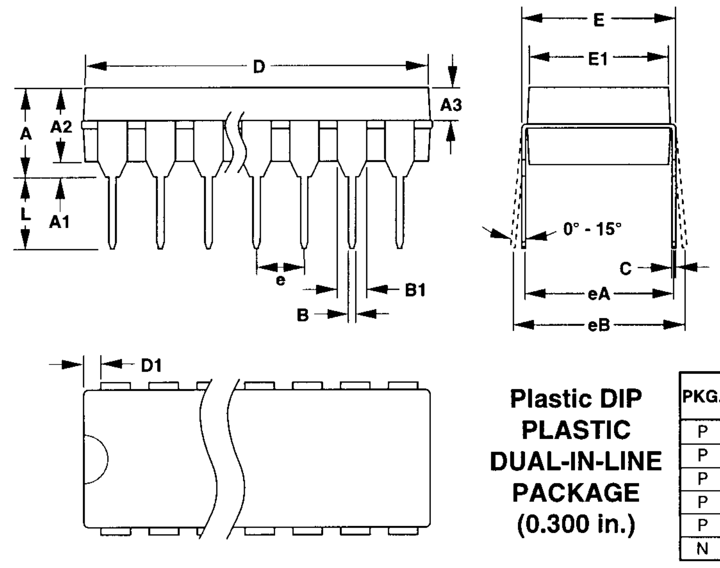
SUPPLY V (NEGATIVE)	R_{BD} (kΩ)	IOUT (mA AT 5V)	MANUFACTURER	MODEL #	PRIMARY L	TURNS RATIO (PRI:SEC)
42 to 54	4.3*	250	Schott Corp.	67122480	6.45mH	8:1
42 to 54	22*	100	Schott Corp.	67122490	16.0mH	8:1

* Use 0.1µF from BD to GND. R_{NEG} = 56k, R_{OSC} = 3.6M, Schott Corporation: (615) 889-8800.

Chip Topography



Package Information

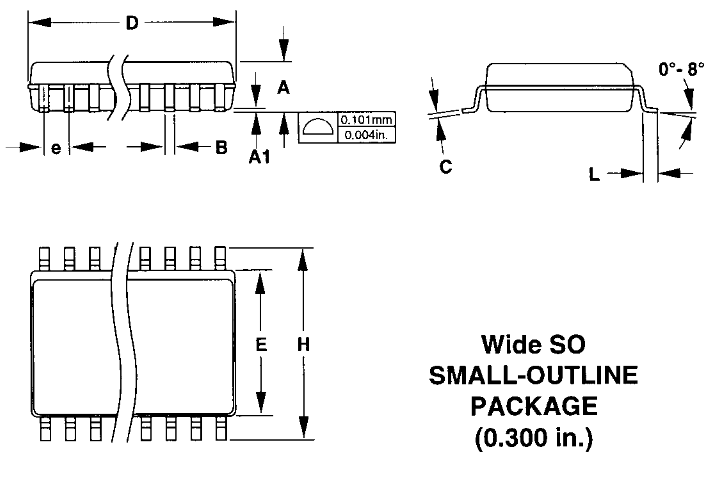


Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

21-0043A



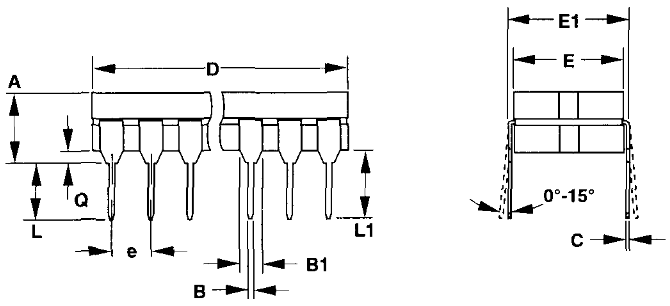
Wide SO
SMALL-OUTLINE
PACKAGE
(0.300 in.)

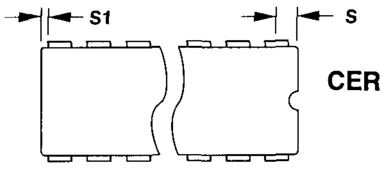
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
E	0.291	0.299	7.40	7.60
e	0.050		1.27	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.398	0.413	10.10	10.50
D	18	0.447	0.463	11.35	11.75
D	20	0.496	0.512	12.60	13.00
D	24	0.598	0.614	15.20	15.60
D	28	0.697	0.713	17.70	18.10

21-0042A

Package Information (continued)





CERDIP
CERAMIC DUAL-IN-LINE
PACKAGE
(0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.070	0.38	1.78
S	–	0.098	–	2.49
S1	0.005	–	0.13	–

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	–	0.405	–	10.29
D	14	–	0.785	–	19.94
D	16	–	0.840	–	21.34
D	18	–	0.960	–	24.38
D	20	–	1.060	–	26.92
D	24	–	1.280	–	32.51

21-0045A