



**MC14160B
MC14161B
MC14162B
MC14163B**

CMOS MSI

SYNCHRONOUS PRESETTABLE 4-BIT COUNTERS

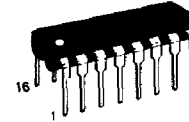
The MC14160B – MC14163B are synchronous programmable counters constructed with complementary MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. These counters are functionally equivalent to the 74160–74163 TTL counters.

Two are synchronous programmable BCD counters with asynchronous and synchronous clear inputs respectively (MC14160B, MC14162B). The other two are synchronous programmable 4-bit binary counters with the asynchronous and synchronous clear respectively (MC14161B, MC14163B).

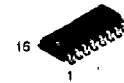
- Internal Look-Ahead for Fast Counting
- Carry Output for N-Bit Cascading
- Synchronously Programmable
- Synchronous Counting
- Load Control Line
- Synchronous or Asynchronous Clear
- Positive Edge Clocked



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = -55° to 125°C for all packages.

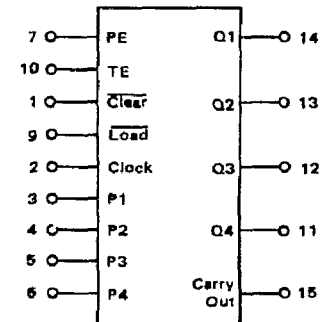
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MC14160B thru MC14163B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		10	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.56 μA/kHz) f + I _{DD}							μAdc
10	I _T = (1.10 μA/kHz) f + I _{DD}									
15	I _T = (1.90 μA/kHz) f + I _{DD}									

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

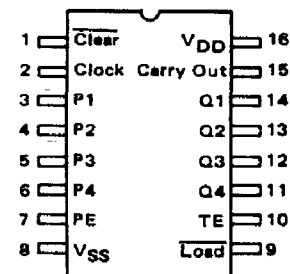
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

PIN ASSIGNMENT



MC14160B thru MC14163B

SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD} V _{dc}	Min	Typ #	Max	Unit			
Output Rise Time	t_{TLH}	5.0	—	100	200	ns			
		10	—	50	100				
		15	—	40	80				
Output Fall Time	t_{THL}	5.0	—	100	200	ns			
		10	—	50	100				
		15	—	40	80				
Propagation Delay Time Clock to Q $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 305 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 132 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 87 \text{ ns}$ Clock to Carry Out $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 395 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 167 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 112 \text{ ns}$ TE to Carry Out $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 225 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 112 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 77 \text{ ns}$ Clear to Q (MC14160B, MC14161B only) $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 110 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 37 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 22 \text{ ns}$	t_{PLH}, t_{PHL}	5.0	—	350	700	ns			
		10	—	150	300				
		15	—	100	200				
		5.0	—	440	880				
		10	—	185	370				
		15	—	125	250				
		5.0	—	300	600				
		10	—	130	260				
		15	—	90	180				
		5.0	—	350	700				
		10	—	150	300				
		15	—	100	200				
		Setup Times Data to Clock Load to Clock Enable to Clock (PE or TE) Clear to Clock (MC14162B, MC14163B only)	t_{su}	5.0	320		160	—	ns
				10	130		65	—	
				15	90		45	—	
5.0	600			300	—				
10	260			130	—				
15	180			90	—				
5.0	420			210	—				
10	170			85	—				
15	120			60	—				
5.0	310			155	—				
10	110			55	—				
15	70			35	—				
Hold Times Clock to Data Clock to Load Clock to PE Clock to TE Clock to Clear (MC14162B, MC14163B only)	t_h	5.0	-10	-80	—	ns			
		10	-5	-25	—				
		15	0	-15	—				
		5.0	-40	-195	—				
		10	-10	-80	—				
		15	-5	-50	—				
		5.0	-40	-175	—				
		10	-10	-70	—				
		15	0	-40	—				
		5.0	-150	-280	—				
		10	-30	-130	—				
		15	-20	-80	—				
Clear Removal Time (MC14160B, MC14161B only)	t_{rem}	5.0	90	30	—	ns			
		10	65	20	—				
		15	55	20	—				

MC14160B thru MC14163B

SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$) (Continued)

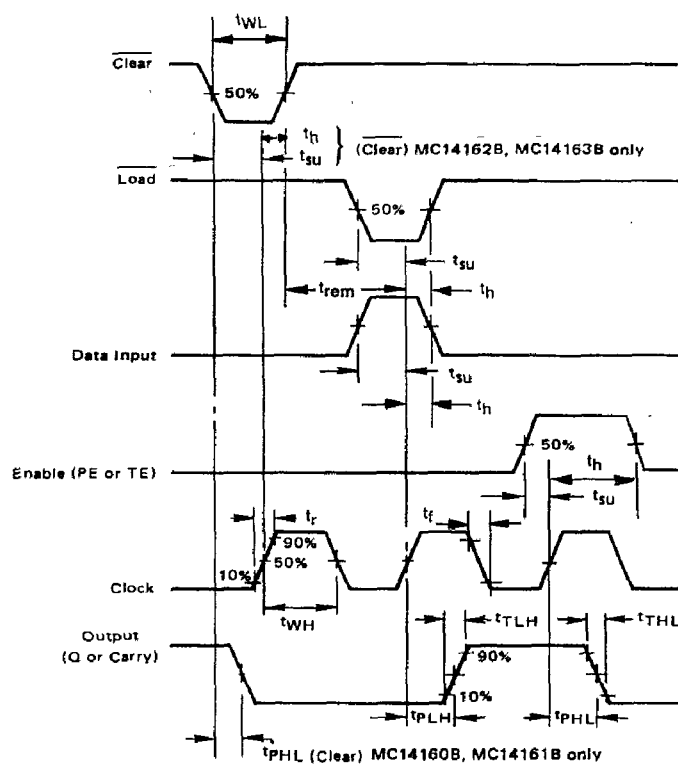
Characteristic	Symbol	V _{DD} V _{dc}	Min	Typ #	Max	Unit
Clear Pulse Width, Low (MC14160B, MC14161B only)	t _{WL}	5.0	200	100	—	ns
		10	90	45	—	
		15	60	30	—	
Clock Pulse Width, High	t _{WH}	5.0	250	125	—	ns
		10	100	50	—	
		15	70	35	—	
Clock Rise and Fall Time	t _r , t _f	5	—	—	15	μs
		10	—	—	5	
		15	—	—	4	
Clock Pulse Frequency	f _{cl}	5.0	—	2.0	1.0	MHz
		10	—	5.0	2.5	
		15	—	8.0	4.0	

*The formulas given are for the typical characteristics only at 25°C.

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MC14160B thru MC14163B

SWITCHING WAVEFORMS



FUNCTIONAL DESCRIPTION

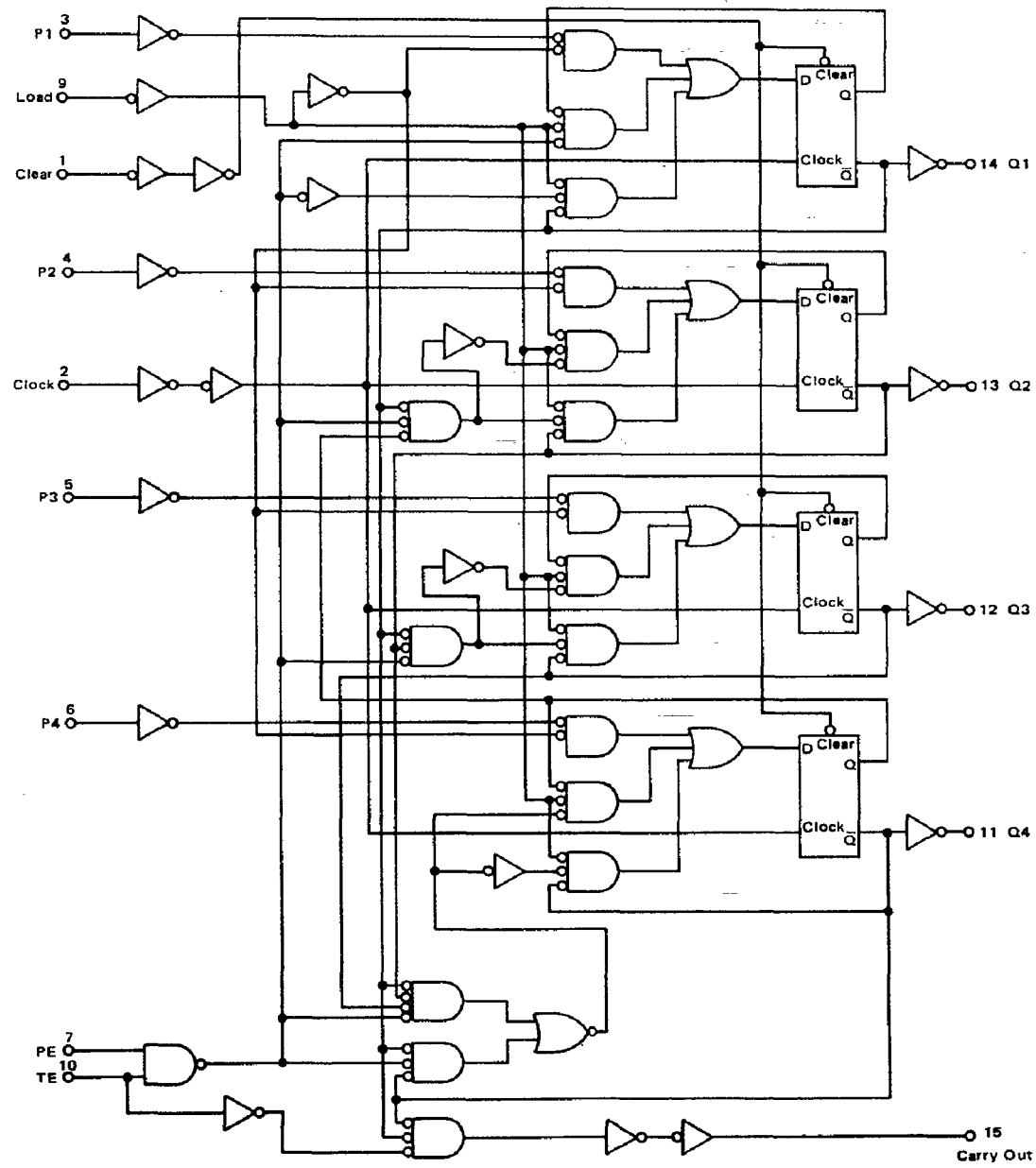
These counters are fully programmable; that is the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the MC14160B, MC14161B is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load or enable inputs. The clear function for the MC14162B and MC14163B is synchronous and a low level at the clear inputs sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily; decoding the maximum count de-

sired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs (PE, TE) must be high to count, and enable input TE fed forward to enable the carry output. The carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages.

MC14160B thru MC14163B

MC14160B, MC14162B LOGIC DIAGRAM
(Clear is synchronous for MC14162B)

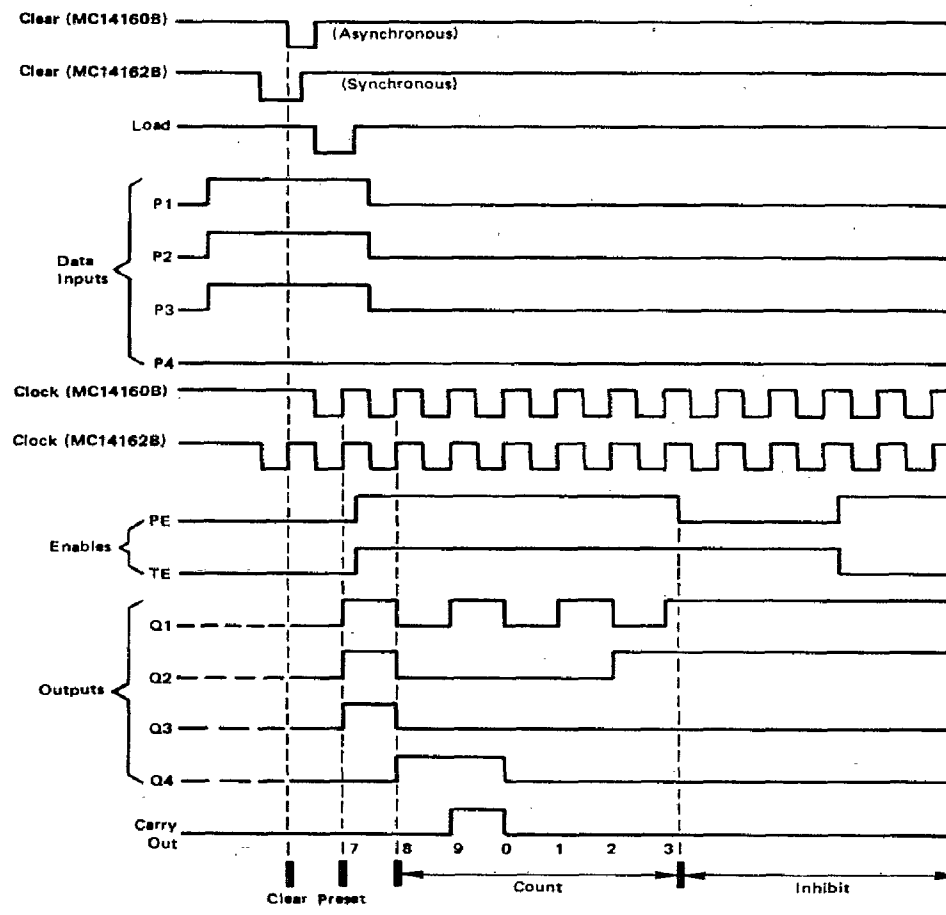


MC14160B thru MC14163B

MC14160B, MC14162B TIMING DIAGRAM

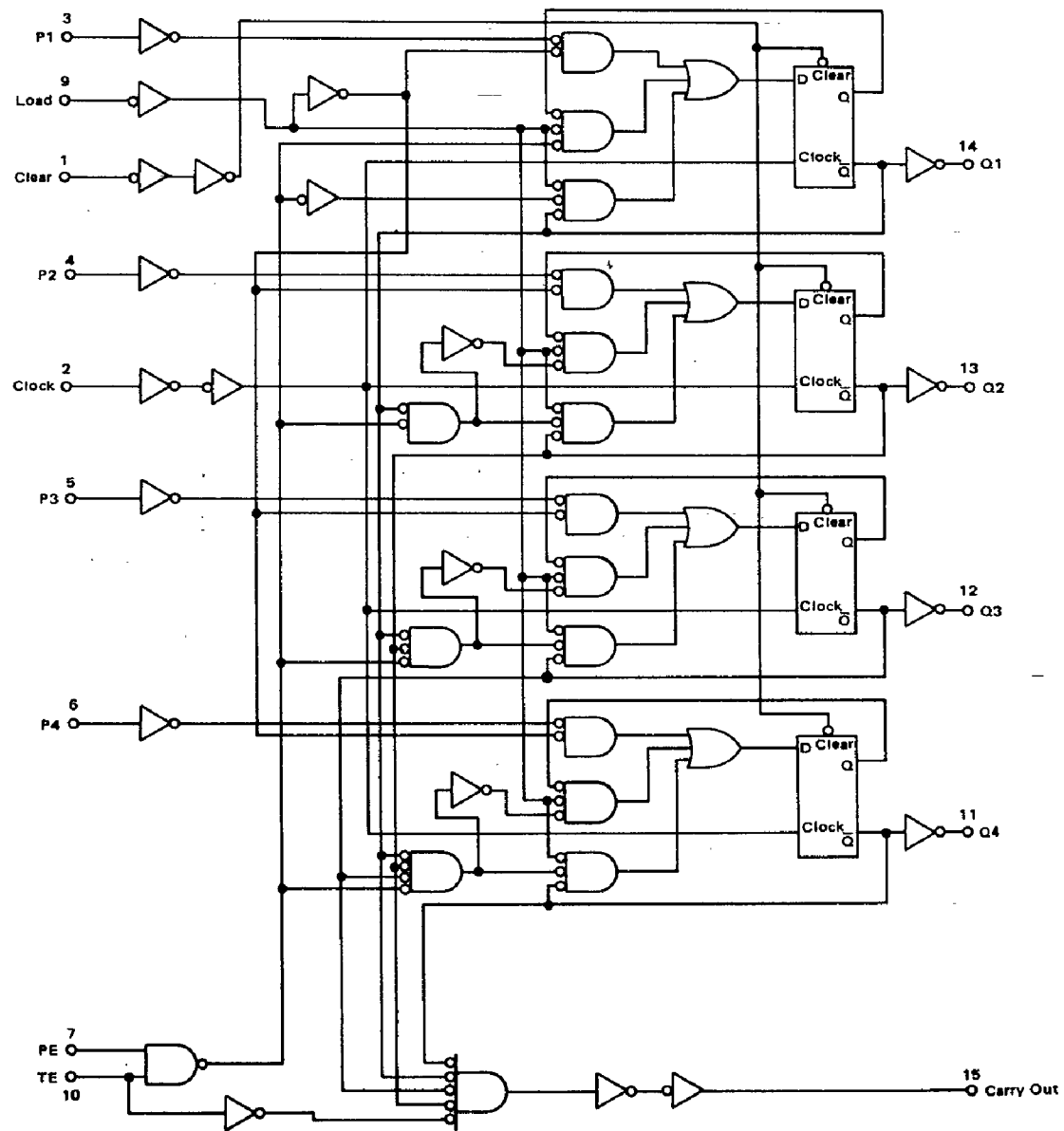
Sequence illustrated in waveforms:

1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit



MC14160B thru MC14163B

MC14161B, MC14163B LOGIC DIAGRAM
(Clear is Synchronous for MC14163B)



MC14160B thru MC14163B

MC14161B, MC14163B TIMING DIAGRAM

- Sequence illustrated in waveforms:
1. Clear outputs to zero.
 2. Preset to binary twelve.
 3. Count to thirteen, fourteen, fifteen, zero, one, and two.
 4. Inhibit

