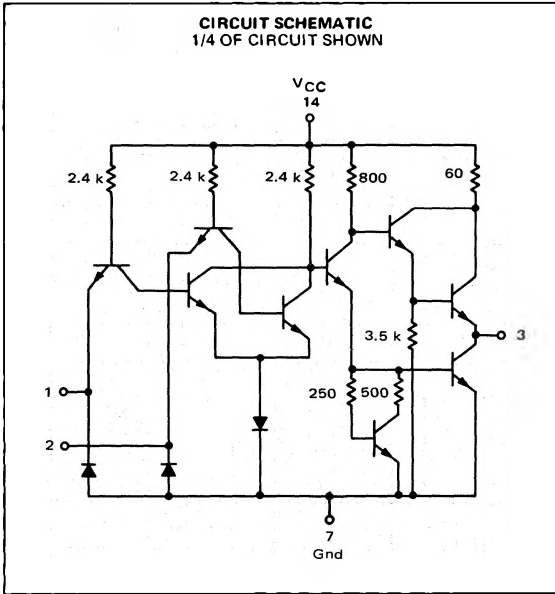


QUAD 2-INPUT "OR" GATE

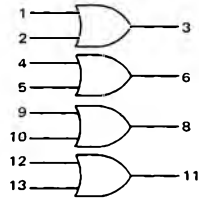
MC3100/MC3000 series

MC3103F • MC3003F
MC3103L • MC3003L,P

CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN



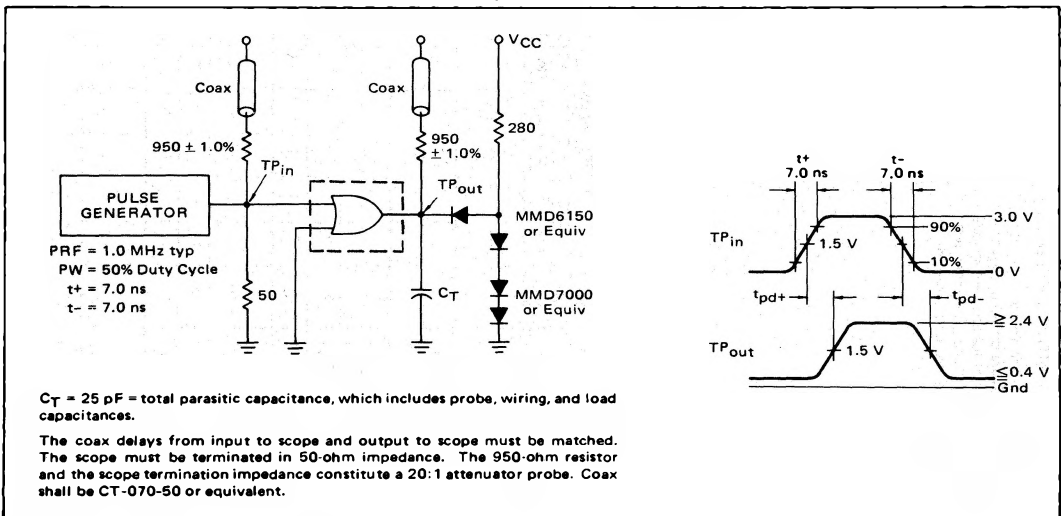
This device consists of four 2-input OR gates. This non-inverting function is useful for optimizing logic design, or for direct implementation of standard logic equations.



Positive Logic: $3 = 1 + 2$
Negative Logic: $3 = 1 \cdot 2$

Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 150 mW typ/pkg
Propagation Delay Time = 9.0 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

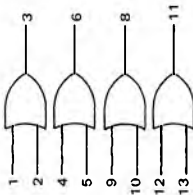


See General Information section for packaging.

MC3103, MC3003 (continued)

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



Characteristic	Symbol	Pin Under Test	MC3103 Test Limits						MC3003 Test Limits						TEST CURRENT / VOLTAGE VALUES													
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C		mA				Volts									
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	I _{OL}	I _{OH}	I _{in}	I _b	V _{IL}	V _{IH}	V _F	V _R	V _{BH}	V _{max}	V _{CC}	V _{CCL}	V _{CCH}	
Input Forward Current	I _F	1	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-2.0	-	-	-	-	-	-	-	-	-	-	-	-	-
Leakage Current	I _R	1	-	50	-	50	-	50	-	50	-	50	-	50	-	50	-	-	-	-	-	-	-	-	-	-	-	-
Breakdown Voltage	BV _{in}	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Clamp Voltage	V _D	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Output Output Voltage	V _{OL}	3	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	1	-	-	-	-	-	-	-	-	-	-
Output Output Voltage	V _{OH}	3	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	2.5	-	1	-	-	-	-	-	-	-	-	-	-	-
Short-Circuit Current	I _{SC}	3	-10	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-40	-100	-	-	-	-	-	-	-	-	-	-	-	-
Power Requirements (Total Device)	I _{max}	14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Maximum Power Supply Current	I _{PDH}	14	-	34	-	34	-	34	-	34	-	34	-	34	-	34	-	-	-	-	-	-	-	-	-	-	-	-
Power Supply Drain	I _{PDL}	14	-	58	-	58	-	58	-	58	-	58	-	58	-	58	-	-	-	-	-	-	-	-	-	-	-	-
Switching Parameters Turn-On Delay	t _{pd+}	1,3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Switching Parameters Turn-Off Delay	t _{pd-}	1,3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

* Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{REF}