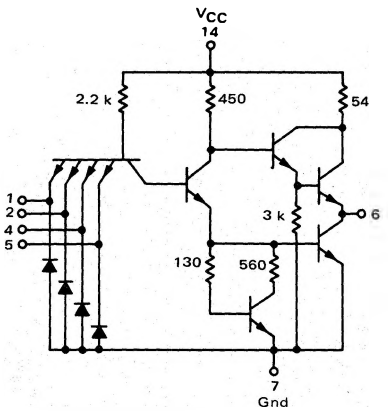
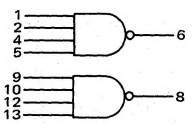
DUAL 4-INPUT "NAND" POWER GATE

# MC3125F • MC3025F
# MC3125L • MC3025L,P

**CIRCUIT SCHEMATIC**
1/2 OF CIRCUIT SHOWN



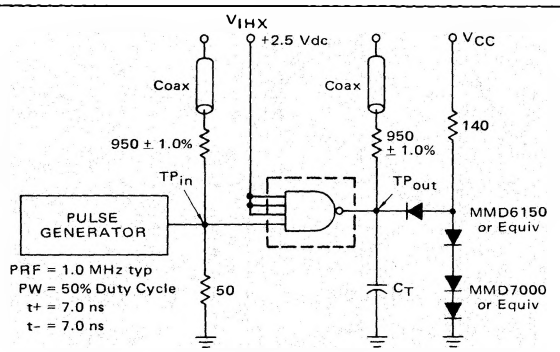

This device consists of two 4-input NAND power gate circuits. Each gate is designed for driving high fan-out loads (20).

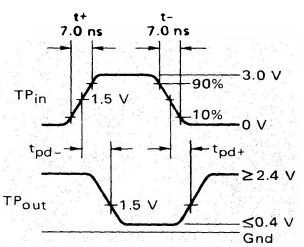



Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$
Negative Logic: $6 = \overline{1 + 2 + 4 + 5}$

Input Loading Factor = 1.3
Output Loading Factor = 20
Total Power Dissipation = 70 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

**SWITCHING TIME TEST CIRCUIT AND WAVEFORMS**



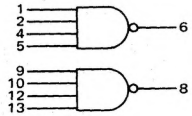

$C_T$ = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

See General Information section for packaging.

## ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.




| @ Test Temperature | TEST CURRENT/VOLTAGE VALUES | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | mA | | | | Volts | | | | | | | | | |
| | $I_{OL}$ | $I_{OH}$ | $I_{in}$ | $I_D$ | $V_{IL}$ | $V_{IH}$ | $V_F$ | $V_R$ | $V_{RH}$ | $V_{max}$ | $V_{CC}$ | $V_{CCL}$ | $V_{CCH}$ | $V_{IHX}$ |
| MC3125 −55°C | 40 | -4.0 | - | - | 1.1 | 2.0 | 0.4 | 2.4 | 4.0 | - | 5.0 | 4.5 | 5.5 | - |
| MC3125 +25°C | 40 | -4.0 | 1.0 | -10 | 1.1 | 1.8 | 0.4 | 2.4 | 4.0 | 7.0 | 5.0 | 4.5 | 5.5 | 2.5 |
| MC3125 +125°C | 40 | -4.0 | - | - | 0.8 | 1.8 | 0.4 | 2.4 | 4.0 | - | 5.0 | 4.5 | 5.5 | - |
| MC3025 0°C | 40 | -4.0 | - | - | 1.1 | 2.0 | 0.4 | 2.5 | 4.0 | - | 5.0 | 4.75 | 5.25 | - |
| MC3025 +25°C | 40 | -4.0 | 1.0 | -10 | 1.1 | 1.8 | 0.4 | 2.5 | 4.0 | 7.0 | 5.0 | 4.75 | 5.25 | 2.5 |
| MC3025 +75°C | 40 | -4.0 | - | - | 0.9 | 1.8 | 0.4 | 2.5 | 4.0 | - | 5.0 | 4.75 | 5.25 | - |

| Characteristic | Symbol | Pin Under Test | MC3125 Test Limits −55°C Min | MC3125 Test Limits −55°C Max | MC3125 Test Limits +25°C Min | MC3125 Test Limits +25°C Max | MC3125 Test Limits +125°C Min | MC3125 Test Limits +125°C Max | MC3025 Test Limits 0°C Min | MC3025 Test Limits 0°C Max | MC3025 Test Limits +25°C Min | MC3025 Test Limits +25°C Max | MC3025 Test Limits +75°C Min | MC3025 Test Limits +75°C Max | Unit | TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: $I_{OL}$ | $I_{OH}$ | $I_{in}$ | $I_D$ | $V_{IL}$ | $V_{IH}$ | $V_F$ | $V_R$ | $V_{RH}$ | $V_{max}$ | $V_{CC}$ | $V_{CCL}$ | $V_{CCH}$ | $V_{IHX}$ | Gnd |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Input** Forward Current | $I_F$ | 1 | - | -2.6 | - | -2.6 | - | -2.6 | - | -2.6 | - | -2.6 | - | -2.6 | mAdc | - | - | - | - | - | - | 1 | - | 2, 4, 5 | - | - | - | 14 | - | 7* |
| Leakage Current | $I_R$ | 1 | - | 50 | - | 50 | - | 50 | - | 50 | - | 50 | - | 50 | μAdc | - | - | - | - | - | - | - | 1 | - | - | - | - | 14 | - | 2, 4, 5, 7* |
| Breakdown Voltage | $BV_{in}$ | 1 | - | - | 5.5 | - | - | - | - | - | 5.5 | - | - | - | Vdc | - | - | 1 | - | - | - | - | - | - | - | - | - | 14 | - | 2, 4, 5, 7* |
| Clamp Voltage | $V_D$ | 1 | - | - | - | -1.5 | - | - | - | - | - | -1.5 | - | - | Vdc | - | - | - | 1 | - | - | - | - | - | - | - | 14 | - | - | 7* |
| **Output** Output Voltage | $V_{OL}$ | 6 | - | 0.4 | - | 0.4 | - | 0.4 | - | 0.4 | - | 0.4 | - | 0.4 | Vdc | 6 | - | - | - | - | 1 | - | - | 2, 4, 5 | - | - | 14 | - | - | 7* |
| | $V_{OH}$ | 6 | 2.4 | - | 2.4 | - | 2.4 | - | 2.5 | - | 2.5 | - | 2.5 | - | Vdc | - | 6 | - | - | 1 | - | - | - | 2, 4, 5 | - | - | 14 | - | - | 7 |
| Short-Circuit Current | $I_{SC}$ | 6 | -50 | -125 | -50 | -125 | -50 | -125 | -50 | -125 | -50 | -125 | -50 | -125 | mAdc | - | - | - | - | - | - | - | - | - | - | - | - | 14 | - | 1,2,4,5,6,7* |
| **Power Requirements (Total Device)** Maximum Power Supply Current | $I_{max}$ | 14 | - | - | - | 16 | - | - | - | - | - | 16 | - | - | mAdc | - | - | - | - | - | - | - | - | - | 14 | - | - | - | - | 1, 2, 4, 5, 7 9, 10, 12, 13 |
| Power Supply Drain | $I_{PDH}$ | 14 | - | 34 | - | 34 | - | 34 | - | 34 | - | 34 | - | 34 | mAdc | - | - | - | - | - | - | - | - | 1, 2, 4, 5, 9, 10, 12, 13 | - | - | - | 14 | - | 7 |
| | $I_{PDL}$ | 14 | - | 10.6 | - | 10.6 | - | 10.6 | - | 10.6 | - | 10.6 | - | 10.6 | mAdc | - | - | - | - | - | - | - | - | - | - | - | - | 14 | - | 1, 2, 4, 5, 7 9, 10, 12, 13 |
| **Switching Parameters** | | | | | | | | | | | | | | | | Pulse In | Pulse Out | | | | | | | | | | | | | |
| Turn-On Delay | $t_{pd-}$ | 1,6 | - | - | - | 12 | - | - | - | - | - | 12 | - | - | ns | 1 | 6 | - | - | - | - | - | - | - | - | 14 | - | - | 2, 4, 5 | 7* |
| Turn-Off Delay | $t_{pd+}$ | 1,6 | - | - | - | 12 | - | - | - | - | - | 12 | - | - | ns | 1 | 6 | - | - | - | - | - | - | - | - | 14 | - | - | 2, 4, 5 | 7* |

*Since this is an inverting gate, power drain is minimized by grounding the inputs to gates not under test.