

DUAL J-K FLIP-FLOP

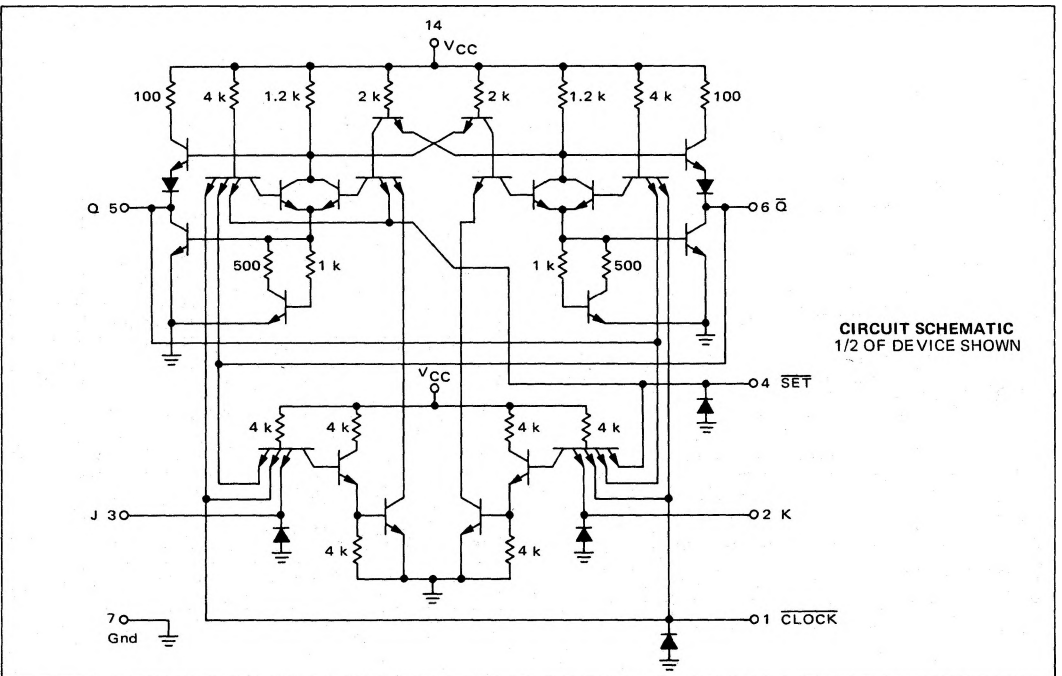
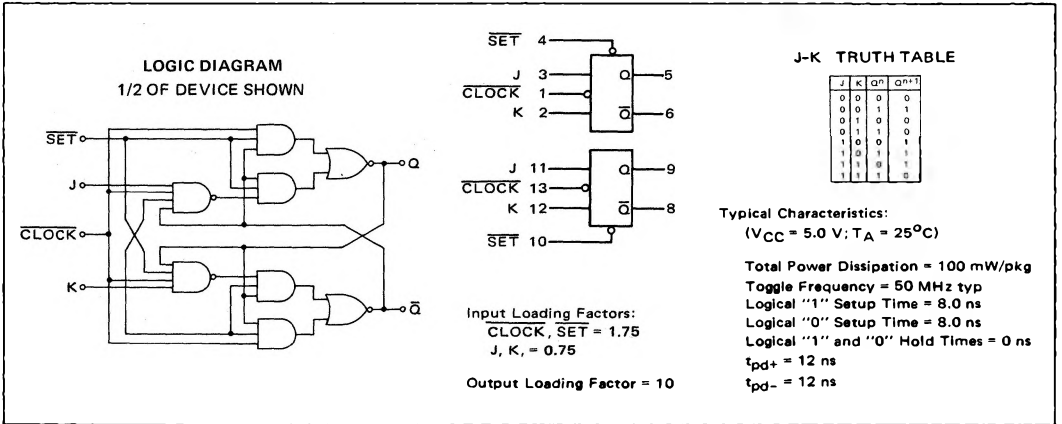
MC3100/MC3000 series

MC3162F • MC3062F
MC3162L • MC3062L,P

This dual JK flip-flop triggers on the negative edge of the clock. Each flip-flop is provided with a separate direct SET input. These direct inputs provide a means of presetting the flip-flop to initial conditions or other asynchronous operations.

Data may be applied to or changed at, the clocked inputs at any time during the clock cycle, except during the time interval between

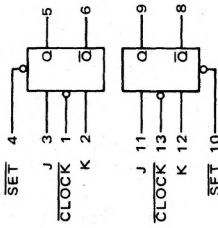
the Set up and Hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between Set up and Hold time is stored in the flip-flop when the clock falls. Each flip-flop may be set at anytime without regard to the clock state by applying a low level to the SET input.



See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



MC3162, MC3062 (continued)

Characteristic	Symbol	Pin Under Test	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:												P ₁ *	Gnd			
			MC3162 Test Limits			MC3062 Test Limits			TEST CURRENT/VOLTAGE VALUES										
			-55°C	+25°C	+125°C	0°C	+25°C	+75°C	I _{OL}	I _{OH}	I _{in}	I _b	V _F	V _R			V _{RH}	V _{max}	V _{CCL}
Input Forward Current	I _F	2	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-1.5	-	-	-	-	-	-	-	
	I _{FS}	3	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-4.7	-	-	-	-	-	-	-	
	I _{FC}	1	-4.5	-4.5	-4.5	-4.5	-4.5	-4.5	-4.5	-4.5	-4.5	-	-	-	-	-	-	-	
	I _R	2	50	50	50	50	50	50	50	50	50	-	-	-	-	-	-	-	
Leakage Current	I _{RS}	4	150	150	150	150	150	150	150	150	150	-	-	-	-	-	-	-	
	I _{RC}	1	150	150	150	150	150	150	150	150	150	-	-	-	-	-	-	-	
Breakdown Voltage	BV _{In}	2	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	-	-	-	-	-	-	-	
		3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
		4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
		1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
Clamp Voltage	V _D	2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
		3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
		4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
		1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
Output Output Voltage	V _{OL}	5	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	-	-	-	-	-	-	-	
		6	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	-	-	-	-	-	-	-	
	V _{OH}	5	2.4	2.4	2.4	2.5	2.5	2.5	2.5	2.5	2.5	-	-	-	-	-	-	-	
		6	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	-	-	-	-	-	-	-	
	I _{SC}	5	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-	-	-	-	-	-	-
		6	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-	-	-	-	-	-	-
Power Requirements (Total Device)	I _{max}	14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
	I _{max}	14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
	I _{PD}	14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	

* Momentarily ground pin prior to taking measurement. (If pin is also in another column the pin must be returned to that voltage or current for measurement.)

OPERATING CHARACTERISTICS

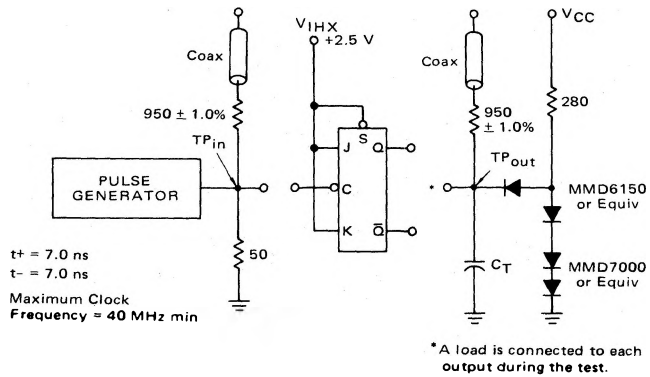
The data must be present 12 ns prior to the fall of the clock and remain until 0 ns after the clock falls.

The flip-flop is set to the Q = 1 state by applying a low level to the SET input. The direct SET inputs may be used at any time without regard to the clock state. If these inputs are not used they should be returned to a voltage between 2.0 and 5.5 Vdc.

Negative edge triggering – The input state during the time interval between the Setup and Hold times is stored in the flip-flop when the clock goes low.

Unused clocked inputs should be tied to the clock, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc.

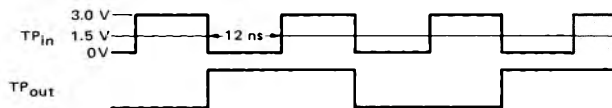
MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

VOLTAGE WAVEFORMS AND DEFINITIONS

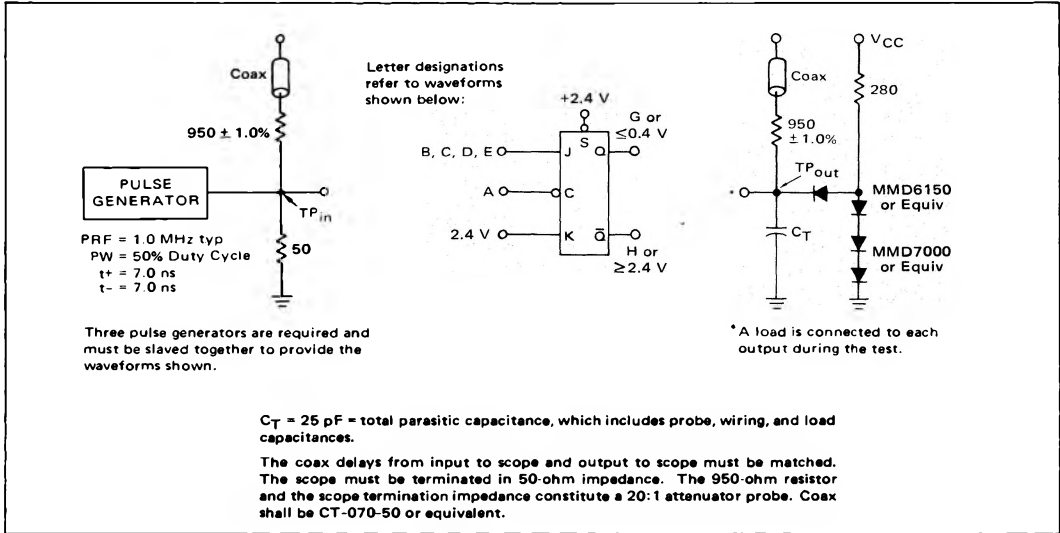


MC3162, MC3062 (continued)

OPERATING CHARACTERISTICS (continued)

SWITCHING TIME TEST CIRCUIT

(For J Inputs; to test other inputs, refer to Test Procedures Chart)



VOLTAGE WAVEFORMS AND DEFINITIONS

