MC3100/MC3000 series

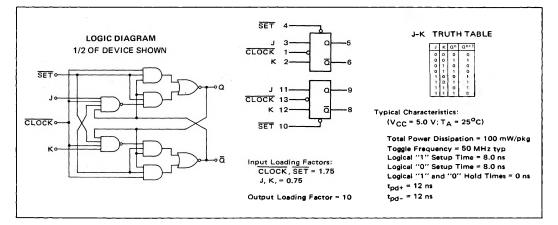
MC3162F • MC3062F MC3162L • MC3062L,P

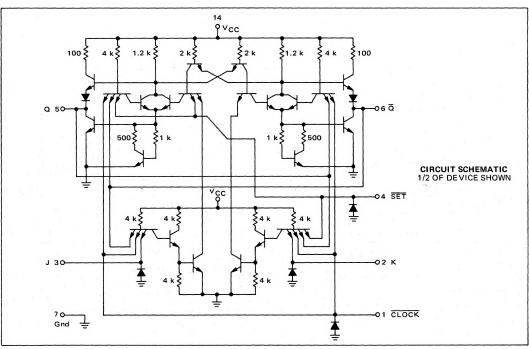
DUAL J-K FLIP-FLOP

This dual JK flip-flop triggers on the negative edge of the clock. Each flip-flop is provided with a separate direct \overline{SET} input. These direct inputs provide a means of presetting the flip-flop to initial conditions or other asynchronous operations.

Data may be applied to or changed at, the clocked inputs at any time during the clock cycle, except during the time interval between

the Set up and Hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The date state at the inputs throughout the interval between Set up and Hold time is stored in the flip-flop when the clock falls. Each flip-flop may be set at anytime without regard to the clock state by applying a low level to the SET input.

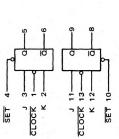




See General Information section for packaging.

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Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.



					C	CLOCK	1	٢									1		IFUL CONVENT / A CLIRACE		-1	TUC			_		-
						¥	2	Т		9				@ Test			MA	}	_		-	Volts					
									וו				Ter	Temperature	re lor		HOH I	 	~ <	>~	V _{RH}	V max	V _{CCL}	V CCH			
						٦	- 11 L	Т		6				(-55°C	C 20		-2.0	- 1	0.4	4 2.4			4.5	5.5			
					5	CLOCK 13-	13	9				W	MC3162	\ +25°C	°C 20		-2.0 1.	1.0 -10	0 0.4	4 2.4	1 4.0	7.0	4.5	5.5			
						¥	K 12	۲	0	80				(+125°C	°C 20	-	-2.0 -	-	0.4	4 2.4	4.0	-	4.5	5.5			
						SET 10-	10-	7) 0°C	°C 20	-	-2.0 -	1	0.4	4 2.5	5 4.0	-	4.75	5,25			-
												Ż	MC3062	~	°C 20	-	-2.0 1.	1.0 -10	0 0.4	4 2.5	5 4.0	7.0	4.75	5.25			
														(+75°C	°C 20	\square	-2.0	<u>'</u>	0.4	4 2.5	5 4.0	-	4.75	5.25			
		Pin	-	WC	3162	MC3162 Test Limits	imits			MC306	52 Tes	MC3062 Test Limits	S		-	TEST	CURREN	U/V0	LTAGE	APPII	ID TO PI	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:	BELOW				
		Under		-55°C	+	+25°C	+125°C	5°C	0°C		+25°C	-	+75°C					+	-						_		
Characteristic	Symbol	Test	_	Min Max	Min	Min Max	Min	Max	Min /	Max N	Min Max	-	Min Max	ix Unit	t _o	HOL		م_ ي.	- C	R_R<	V _{RH}	Vmax	V _{ccL}	VccH	* -	Gnd	
Input Forward Current	Ŧ	3 M	- F - F	-1.5	т.	-1.5	1.1	-1.5		-1.5		-1.5 -	-1.5	5 mAdc 5 mAdc					2,6	 2 C	1,4			14 14		3,7,13 2,7,13	
	$I_{F\overline{S}}$	4		-4.7		-4.7		-4.7		-4.7	4-	-4.7 -	-4.7	7 mAdc	-	•		1	4,6	1 9	1,2	1	1.	14	1	3,7,13	
	IFC		1.1	-4.5	1.1	-4.5	1.1	-4.5	1 1	-4.5	4.4	-4.5 -	-4.5	5 mAdc 5 mAdc	· · 0 0	1 1		· · · ·	1,6	1 1	2,3	1 1	1.1	14 14	4 -	7,13 7,13	
Leakage Current	I _R	00	1.1	50	1.1	50		50		50	2 2 2	50 -	50	μAdc μAdc		1 1				00	60 61	i'i		14 14		1,4,7,13 1,4,7,13	
	$I_{\rm R\overline{S}}$	4	1	150	1	150	1	150	1	150	- 18	150 -	150	0 µAdc	-	1		-	-	4	e	1		14	1	1,2,7,13	
	IRC	1	1	150	r:	150	1	150	<u>.</u>	150	- 15	150 -	150	0 µAdc	-		-	1	'	-	-			14	•	2,3,4,7,13	
Breakdown Voltage	BV _{in}	0 6 4 1	i i i i i	1.1.1.1	5.5		1111	1 1 1 1		1 I I I	€2°			Vdc				01004-		1 1 1 1		1111		14 •	1111	1,4,7,13 1,4,7,13 1,2,7,13 2,3,4,7,13	
Clamp Voltage	UD D	1435				-1.5		1.1.1.1			+	2		Vdc				010041				а <u>т</u> тт 	14			7,13	
Output Output Voltage	v _{oL}	و <u>م</u>	• • •	0.4 0.4		0.4 0.4		0.4		-	- 0.4		0.4		6.0				+ + + + + + + + + + + + + + + + + + +	• •		1.1	14 14		r0 4	1,7,13 1,7,13	
	НОЛ	6 5	2.5	î î î	2.5	i. j	2.5	1 1	2.5	1 1	2.5 -	2.5	5	Vdc		9		· ·	4 -	1 1	- 4		14		4 LC	$^{7}_{1,7,13}$	
Short-Circuit Current	Isc	5	-20	-65	-20	-65	-20	-65	-20	-65 -2	-20 -65	5 -20	-65	5 mAdc	lc -	1		-1 -1	'	1	1	•	• •	14	•	4,5,7,13	
Power Requirements (Total Device) Maximum Power Supply Current	Imax	14	1	1. 1. ² .		41			. 1		- 41			mAdc	r gc				. 1	1		14	1 I.		1	4,7,10	
Power Supply Drain	IPD	14	T.	31	1	31	1	31	1, 1	31	- 31	-	31	l mAdc	lc -	1		•	1	1	1	1		14	•	4,7,10	
									•	1		:															1

* Momentarily ground pin prior to taking measurement. (If pin is also in another column the pin must be returned to that voltage or current for measurement.)

MC3162, MC3062 (continued)

TEST CURRENT/VOLTAGE VALUES

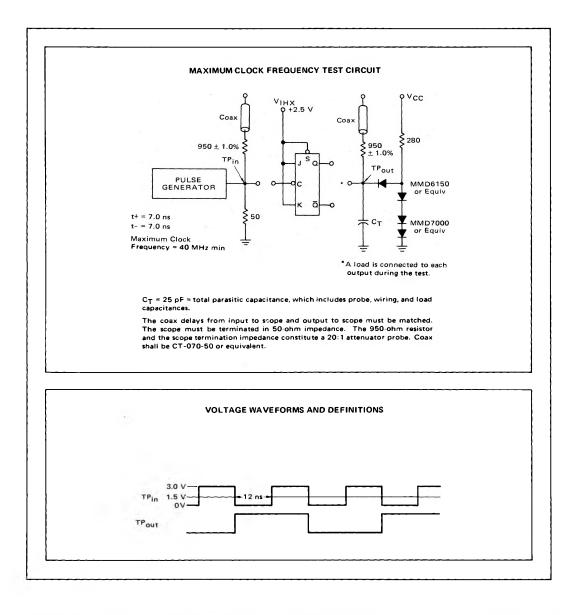
OPERATING CHARACTERISTICS

The data must be present 12 ns prior to the fall of the clock and remain until 0 ns after the clock falls.

The flip-flop is set to the Q = 1 state by applying a low level to the \overline{SET} input. The direct \overline{SET} inputs may be used at any time without regard to the clock state. If these inputs are not used they should be returned to a voltage between 2.0 and 5.5 Vdc.

Negative edge triggering – The input state during the time interval between the Setup and Hold times is stored in the flip-flop when the clock goes low.

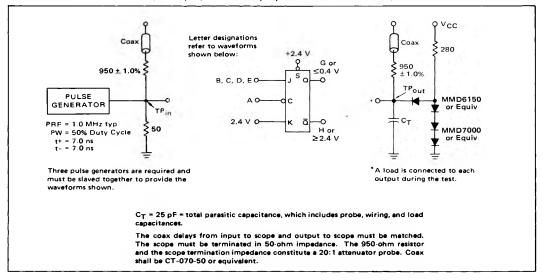
Unused clocked inputs should be tied to the clock, to the internally connected output, or to a voltage between 2.0 and 5.5 Vdc.



MC3162, MC3062 (continued)

OPERATING CHARACTERISTICS (continued)

SWITCHING TIME TEST CIRCUIT (For J Inputs; to test other inputs, refer to Test Procedures Chart)



VOLTAGE WAVEFORMS AND DEFINITIONS

CLOCK (Must be used on all tests)					INPU	т		LIMITS (ns
B 3.0 V		TEST	•ر	SET.	к•	٥.	ō٠	Max
0 V	ſ	^t Setup "1" J	6	2.4 V	2.4 V	G	т	15
C 3.0 V +30 ns+	For J tests, the flip flop is reset by alter-	1401d "1" J	c	2.4 V	2.4 V	G	н	0
0 v_t 1.5 V	nate clock pulses	^t Setup "0" J	D	2.4 V	240	≤0.4 ∨	≥2.4 v	15
D 3.0 V	L	^t Hold ''0'' J	E	24 V	2.4 V	≤0.4 ∨	≥2.4 ∨	0
0 V		^t Setup "1" K	Gnd	F	8	н	G	15
		tHold "1" K	Gnd	F	с	н	e O	0**
E 3.0 V + 1.5 V		^t Setup "O" K	Gnd	F	D	≥2.4 V	≤0.4 V	15
0 V		¹ Hold "O" K	Gnd	F	E	22.4V	≲0.4 V	0
F 3.0 V	++30 ns+ + +1.5 ∨	10d+) ''1'' j test.) ''1'' K test.	18
0 V	t _{sd} -	tpd≁					, "1" j test. , "1" қ test.	18
0 V /	1.5 V	t _{sd+}	Delay fr	om SET te	a during	Setup "1	"K test.	18
H 3.0 V		4d-	Delay fr	om SET u	a during	Setup "1	" K 1051.	18