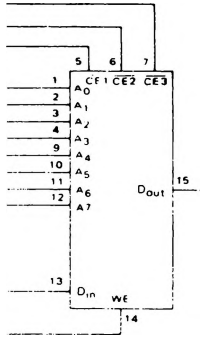

TRUTH TABLE

MODE	INPUT			OUTPUT
	CE	WE	Din	Dout
Write 0	L	L	L	L
Write 1	L	L	H	L
Read	L	H	X	D
Disabled	H	X	X	L

X = Don't Care

t_{Access} = 18 ns (typ) (Address Inputs)

256-Bit Random Access Memory

The MCM10144 is a fully decoded 256-bit Random Access Read/Write Memory organized as 256 one bit words. Stored data is selected by means of an eight bit address, consisting of inputs A0 through A7.

The MCM10144 has three active-low chip enable inputs for increased logic flexibility permitting memory expansion up to 2048 words without additional decoding. For larger memories, the upper address words are selected by using one of the $\overline{CE}$ inputs for enabling 1024 word segments.

The MCM10144 operating mode (all $\overline{CE}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the WRITE mode, the output, D_{out}, is low and the data state present at the data input (pin 13) is stored at the selected address. With the $\overline{WE}$ high the chip is in the READ mode and the data state at the selected memory location will be presented, noninverted at the data output (pin 15).

Open emitter outputs permit full *wire-ORing* to data buses, with D_{out} low when the chip is disabled.

The device is fully compatible with the MECL 10,000 logic family. It is designed for use in high speed scratch pad, control, cache, and buffer storage applications.