MCP6021/2/3/4

Rail-to-Rail Input/Output, 10 MHz Op Amps

Features

- Rail-to-Rail Input/Output
- Wide Bandwidth: 10 MHz (typ)
- Low Noise: 8.7 nV/√Hz, at 10 kHz (typ)
- Low Offset Voltage: 500 µV (max), at 25°C
- Mid-Supply V_{REF} : MCP6021 and MCP6023
- Low Supply Current: 1 mA (typ)
- Total Harmonic Distortion: 0.00053% (typ., G = 1)
- Unity Gain Stable
- Power Supply Range: 2.5V to 5.5V

Typical Applications

- Driving A/D Converters
- Multi-Pole Active Filters
- Barcode Scanners
- Audio Processing
- Communications
- DAC Buffer
- Test Equipment
- Medical Instrumentation

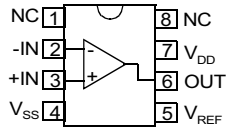
Description

The MCP6021, MCP6022, MCP6023, and MCP6024 from Microchip Technology, Inc. are rail-to-rail input and output op amps with high performance. Key specs include: wide bandwidth (10 MHz), low noise (8.7 nV/√Hz), low input offset voltage (500 µV), and low distortion (0.00053% THD+N). These features make these op amps well suited for applications requiring high performance and bandwidth. The MCP6023 also offers a chip select ($\overline{CS}$) that gives power savings when the part is not in use.

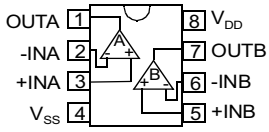
The single MCP6021 is available in standard 8-lead PDIP, SOIC, TSSOP. The dual MCP6022 is offered in standard 8-lead PDIP, SOIC, and TSSOP packages. The single MCP6023 with Chip Select ($\overline{CS}$) is offered in standard 8-lead PDIP, SOIC, and TSSOP packages. Finally, the quad MCP6024 is offered in 14-lead PDIP, SOIC and TSSOP packages. All devices are specified from -40°C to +85°C with power supplies from 2.5V to 5.5V.

Package Types

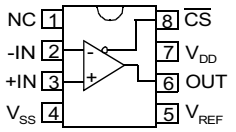
MCP6021
PDIP, SOIC, TSSOP



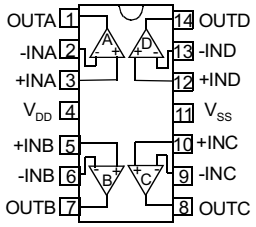
MCP6022
PDIP, SOIC, TSSOP



MCP6023
PDIP, SOIC, TSSOP



MCP6024
PDIP, SOIC, TSSOP



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{DD}.....7.0V
All inputs and outputs w.r.t. ..... V_{SS} –0.3V to V_{DD} +0.3V
Difference Input voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .....continuous
Current at Input Pins .....±2 mA
Current at Output and Supply Pins .....±30 mA
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-55°C to +125°C
Junction Temp. ..... 150°C
ESD protection on all pins (HBM) ..... ≥ 2 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

NAME	FUNCTION
+IN/+INA/+INB/+INC/+IND	Non-inverting Input Terminals
-IN/-INA/-INB/-INC/-IND	Inverting Input Terminals
V_{DD}	Positive Power Supply
V_{SS}	Negative Power Supply
$\overline{CS}$	Chip Select
V_{REF}	Reference Voltage
OUT/OUTA/OUTB/OUTC/OUTD	Output Terminals
NC	No internal connection

DC CHARACTERISTICS

Unless otherwise indicated, all limits are specified for: T_A = 25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ~ V_{DD}/2, and R_L = 10 kΩ to V_{DD}/2.

PARAMETERS	SYM	MIN	TYP	MAX	UNITS	CONDITIONS
Input Offset:						
Input Offset Voltage	V_{OS}	-500	—	+500	µV	
Input Offset Voltage Temperature Drift	dV_{OS}/dT	—	±3.0	—	µV/°C	T_A= -40°C to +85°C
Power Supply Rejection Ratio	PSRR	74	90	—	dB	V_{CM} = 0V
Input Current and Impedance:						
Input Bias Current	I_B	—	1	—	pA	
Input Bias Current Over Temperature	I_B	—	—	150	pA	T_A= -40°C to +85°C
Input Offset Current	I_{OS}	—	±1	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||3	—	Ω||pF	
Common Mode:						
Common-Mode Input Range	V_{CMR}	V_{SS}–0.3	—	V_{DD}+0.3	V	
Common-Mode Rejection Ratio	CMRR	74	90	—	dB	V_{DD} = 5V, V_{CM} = -0.3 and 5.3V
Common-Mode Rejection Ratio	CMRR	70	85	—	dB	V_{DD} = 5V, V_{CM} = 3 and 5.3V
Common-Mode Rejection Ratio	CMRR	74	90	—	dB	V_{DD} = 5V, V_{CM} = -0.3 and 3V
Voltage Reference: (MCP6021 and MCP6023 only)						
V_{REF} Accuracy (V_{REF} - V_{DD}/2)	ΔV_{REF}	-50	—	+50	mV	
V_{REF} Temperature Drift	dV_{REF}/dT	—	±100	—	µV/°C	T_A= -40°C to +85°C
Open Loop Gain:						
DC Open Loop Gain (Large Signal)	A_{OL}	90	110	—	dB	V_{CM} = 0V, V_{OUT} = V_{SS}+300 mV and V_{DD}-300 mV
Output:						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS}+15	—	V_{DD}–20	mV	
Output Short Circuit Current	I_O	—	±30	—	mA	V_{DD} = 5.5V
Power Supply:						
Supply Voltage	V_S	2.5	—	5.5	V	
Quiescent Current per Amplifier	I_Q	0.5	1.0	1.35	mA	I_O = 0

AC CHARACTERISTICS

Unless otherwise indicated, all limits are specified for: T_A = 25°C, V_{DD} = +5.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ~ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2, and C_L = 60 pF.

PARAMETERS	SYM	MIN	TYP	MAX	UNITS	CONDITIONS
AC Response:						
Gain Bandwidth Product	GBWP	—	10	—	MHz	
Phase Margin at Unity Gain	θ_M	—	65	—	°	G = 1
Settling Time, 0.2%	t_{SETTLE}	—	250	—	ns	G = 1, V_{OUT} = 100mV_{p-p}
Slew Rate	SR	—	7.0	—	V/µs	
Distortion:						
Total Harmonic Distortion plus Noise	THD+N	—	0.00053	—	%	G = 1, V_{OUT} = 0.25V + 3.25V @ 1kHz, BW = 22 kHz
Total Harmonic Distortion plus Noise	THD+N	—	0.00064	—	%	G = 1, V_{OUT} = 0.25V + 3.25V, R_L = 600Ω @ 1kHz, BW = 22 kHz
Total Harmonic Distortion plus Noise	THD+N	—	0.0014	—	%	G = 1, V_{OUT} = 4V_{P-P} @ 1 kHz, BW = 22 kHz
Total Harmonic Distortion plus Noise	THD+N	—	0.0009	—	%	G = 10, V_{OUT} = 4V_{P-P} @ 1 kHz, BW = 22 kHz
Total Harmonic Distortion plus Noise	THD+N	—	0.005	—	%	G = 100, V_{OUT} = 4V_{P-P} @ 1 kHz, BW = 22 kHz
Noise:						
Input Voltage Noise	E_n	—	2.9	—	µVp-p	f = 0.1 Hz to 10 Hz
Input Voltage Noise Density	e_n	—	8.7	—	nV/√Hz	f = 10 kHz
Input Current Noise Density	i_n	—	3	—	fA/√Hz	f = 1 kHz

CHIP SELECT SPECIFICATIONS FOR MCP6023

Unless otherwise indicated, all limits are specified for: T_A = 25°C, V_{DD} = +2.5V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ~ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2, and C_L = 60 pF.

PARAMETERS	SYM	MIN	TYP	MAX	UNITS	CONDITIONS
$\overline{CS}$ Low Specifications:						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	0	—	0.2V_{DD}	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	—	0.01	—	µA	$\overline{CS}$ = V_{SS}
$\overline{CS}$ High Specifications:						
$\overline{CS}$ Logic Threshold, High	V_{IH}	0.8V_{DD}	—	V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	0.01	—	µA	$\overline{CS}$ = V_{DD}
$\overline{CS}$ Input High, GND Current	I_Q	—	0.05	—	µA	$\overline{CS}$ = V_{DD}
Amplifier Output Leakage	—	—	0.01	—	µA	
Dynamic Specifications:						
$\overline{CS}$ Low to Amplifier Output High Turn-on Time	t_{ON}	—	2	10	µs	G = 1, V_{IN} = V_{SS}, $\overline{CS}$ = 0.2V_{DD} to V_{OUT} = 0.45V_{DD} time
$\overline{CS}$ High to Amplifier Output High Z Turn-off Time	t_{OFF}	—	0.01	—	µs	G = 1, V_{IN} = V_{SS}, $\overline{CS}$ = 0.8V_{DD} to V_{OUT} = 0.05V_{DD} time
Hysteresis	V_{HYST}	—	0.6	—	V	

TEMPERATURE SPECIFICATIONS

Unless otherwise indicated, all limits are specified for: V_{DD} = +2.5V to +5.5V, and V_{SS} = GND.

PARAMETERS	SYM	MIN	TYP	MAX	UNITS	CONDITIONS
Temperature Ranges:						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+85	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances:		—		—		
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-TSSOP	θ_{JA}	—	124	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

2.0 TYPICAL PERFORMANCE CHARACTERISTICS

Note:	The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = +5.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ~ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2, and C_L = 60 pF.

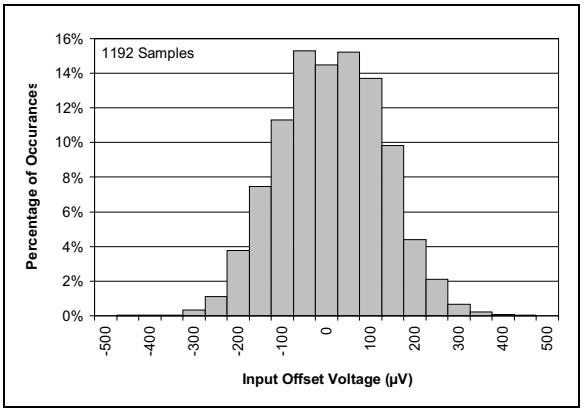


FIGURE 2-1: *Histogram of Input Offset Voltage.*

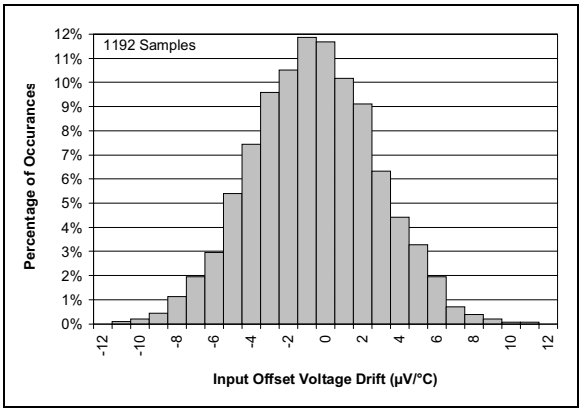


FIGURE 2-4: *Histogram of Input Offset Voltage Drift.*

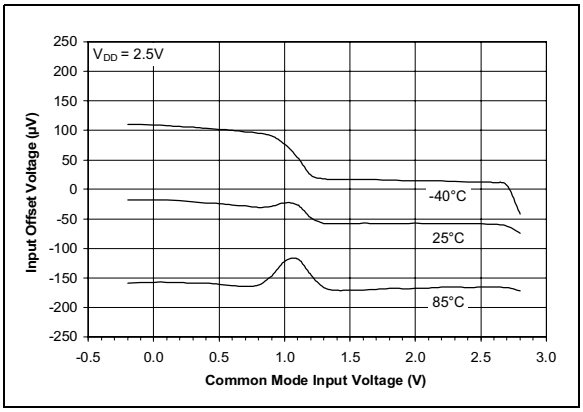


FIGURE 2-2: *Input Offset Voltage vs. Common Mode Input Voltage vs. Temperature with V_{DD} = 2.5V.*

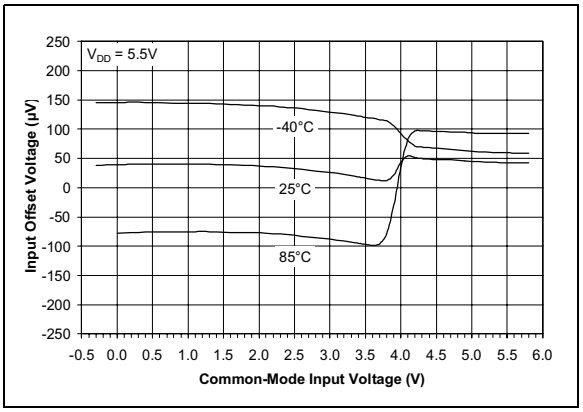


FIGURE 2-5: *Input Offset Voltage vs. Common Mode Input Voltage vs. Temperature with V_{DD} = 5.5V.*

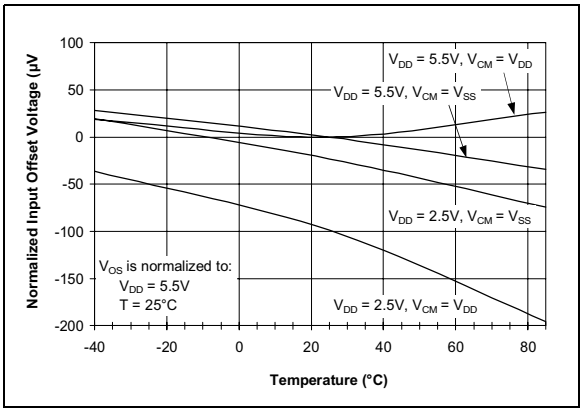


FIGURE 2-3: *Normalized Input Offset Voltage vs. Temperature.*

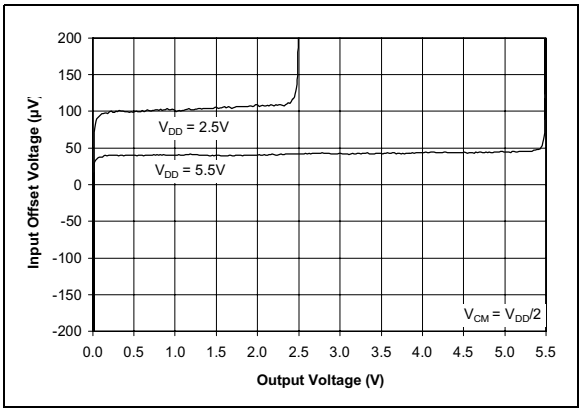


FIGURE 2-6: *Input Offset Voltage vs. Output Voltage vs. Power Supply Voltage.*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = +5.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ~ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2, and C_L = 60 pF.

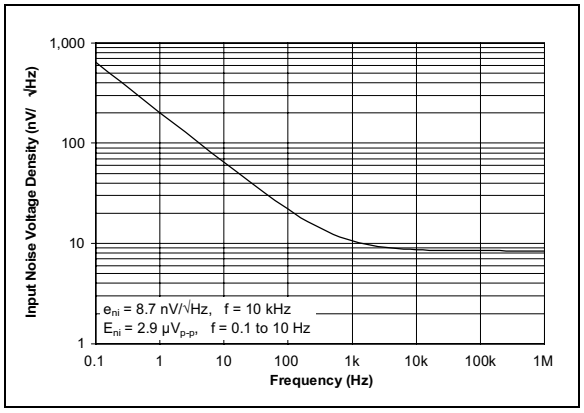


FIGURE 2-7: *Input Noise Voltage Density vs. Frequency.*

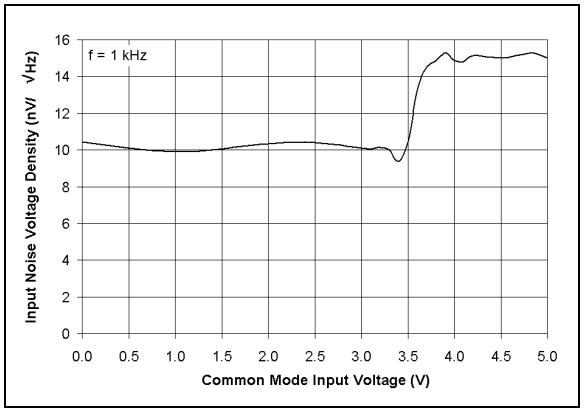


FIGURE 2-10: *Input Noise Voltage Density at 1 kHz vs. Common Mode Input Voltage.*

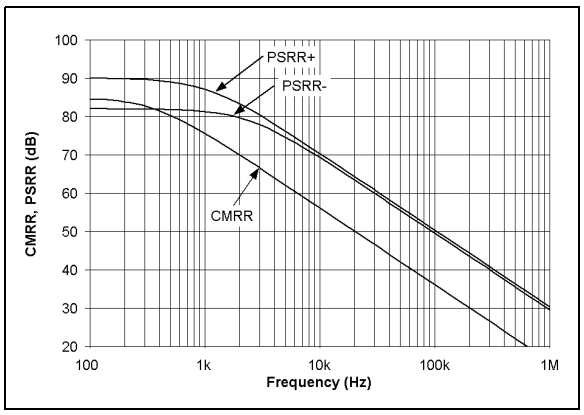


FIGURE 2-8: *Common Mode Rejection Ratio, Power Supply Rejection Ratio vs. Frequency.*

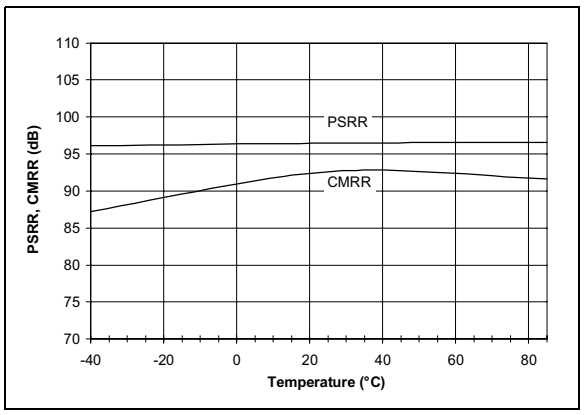


FIGURE 2-11: *Common Mode Rejection Ratio, Power Supply Rejection Ratio vs. Temperature.*

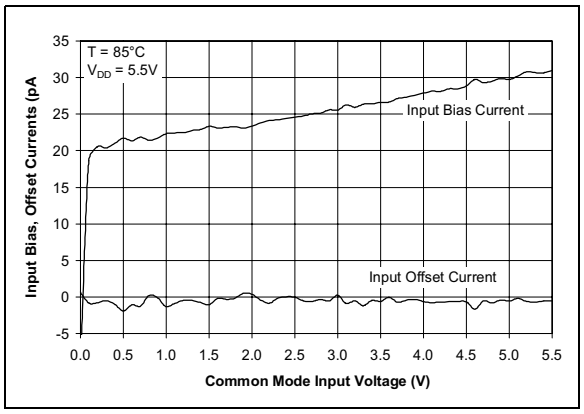


FIGURE 2-9: *Input Bias, Offset Currents vs. Common Mode Input Voltage with Temperature = 85°C.*

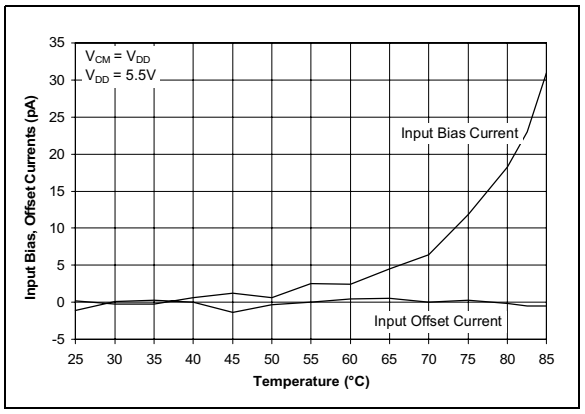


FIGURE 2-12: *Input Bias, Offset Currents vs. Temperature with V_{CM} = V_{DD}.*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = +5.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ~ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2, and C_L = 60 pF.

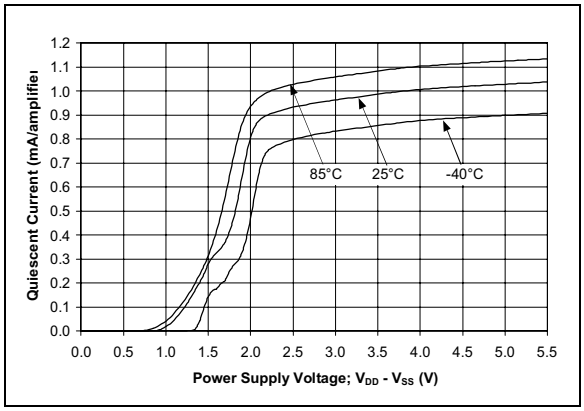


FIGURE 2-13: *Input Bias Current vs. Power Supply Voltage vs. Temperature.*

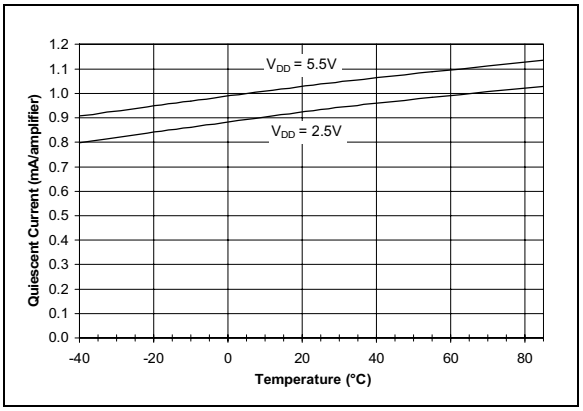


FIGURE 2-16: *Quiescent Current vs. Temperature vs. Power Supply Voltage.*

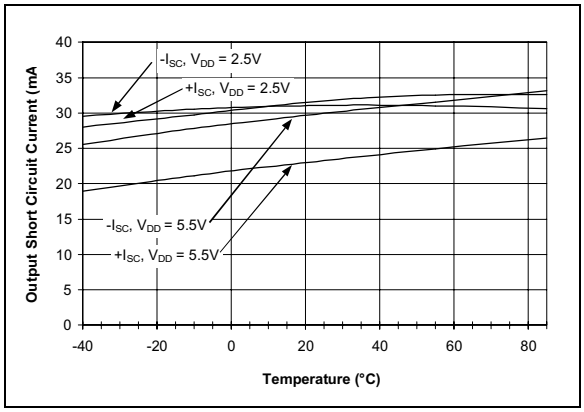


FIGURE 2-14: *Output Short Circuit Current vs. Temperature vs. Power Supply Voltage.*

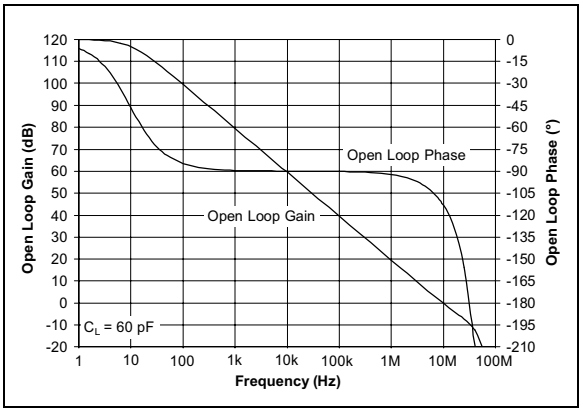


FIGURE 2-17: *Open Loop Gain, Phase vs. Frequency.*

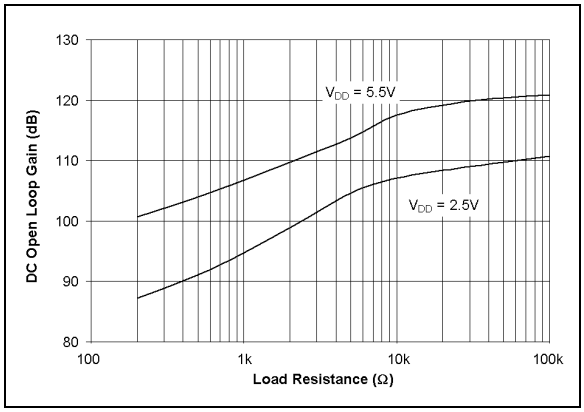


FIGURE 2-15: *DC Open Loop Gain vs. Load Resistance vs. Power supply Voltage.*

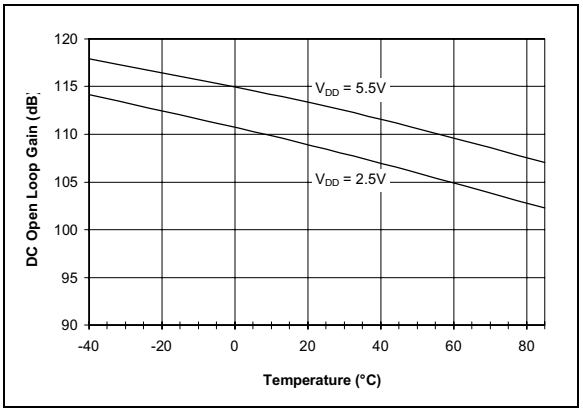


FIGURE 2-18: *DC Open Loop Gain vs. Temperature vs. Power Supply Voltage.*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = +5.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ~ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2, and C_L = 60 pF.

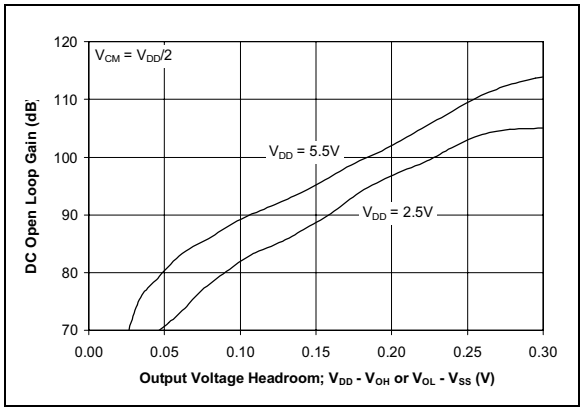


FIGURE 2-19: *Small Signal DC Open Loop Gain vs. Output Voltage Headroom.*

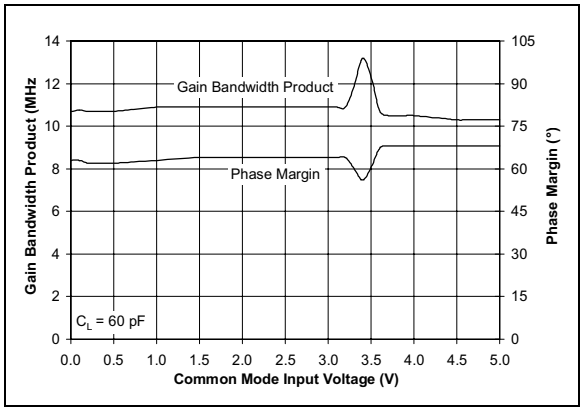


FIGURE 2-22: *Gain Bandwidth Product, Phase Margin vs. Common Mode Input Voltage.*

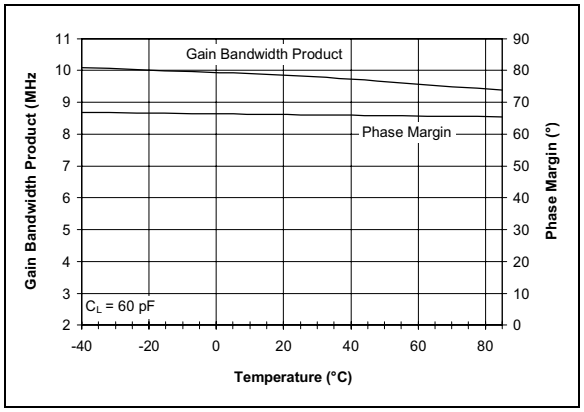


FIGURE 2-20: *Gain Bandwidth Product, Phase Margin vs. Temperature.*

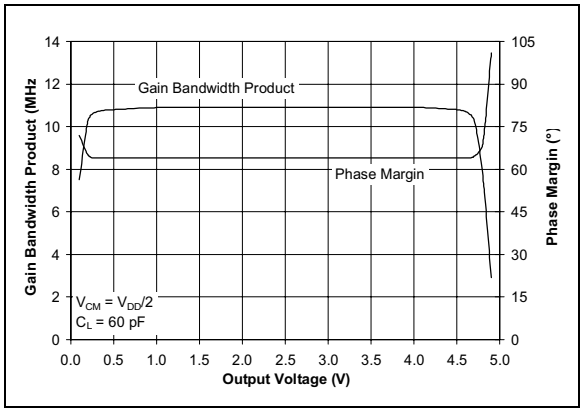


FIGURE 2-23: *Gain Bandwidth Product, Phase Margin vs. Output Voltage.*

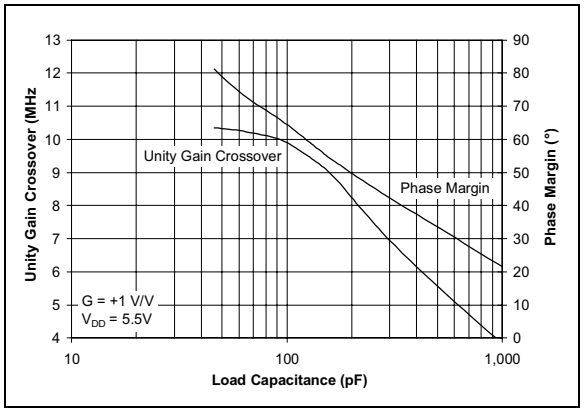


FIGURE 2-21: *Unity Gain Crossover, Phase Margin vs. Load Capacitance with V_{DD} = 5.5V.*

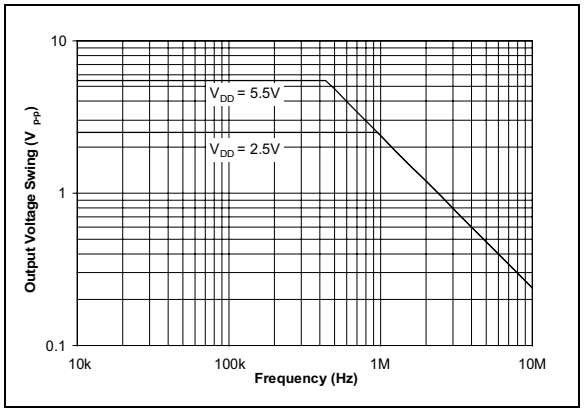


FIGURE 2-24: *Output Voltage Swing vs. Frequency vs. Power Supply Voltage.*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = +5.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ~ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2, and C_L = 60 pF.

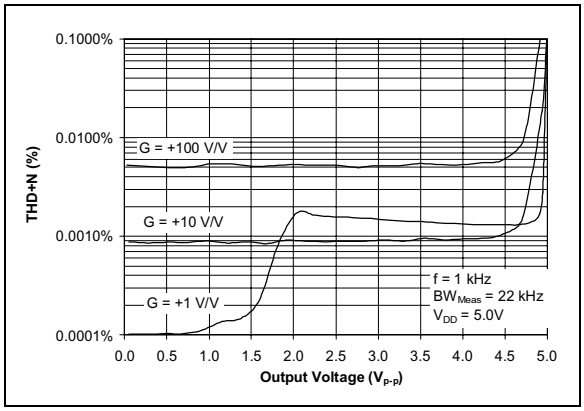


FIGURE 2-25: *Total Harmonic Distortion plus Noise vs. Output Voltage with f = 1 kHz.*

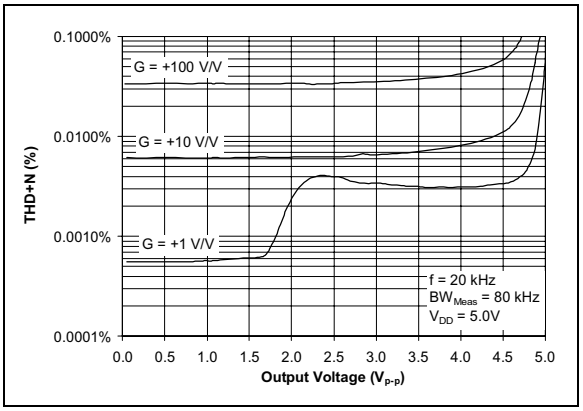


FIGURE 2-28: *Total Harmonic Distortion plus Noise vs. Output Voltage with f = 20 kHz.*

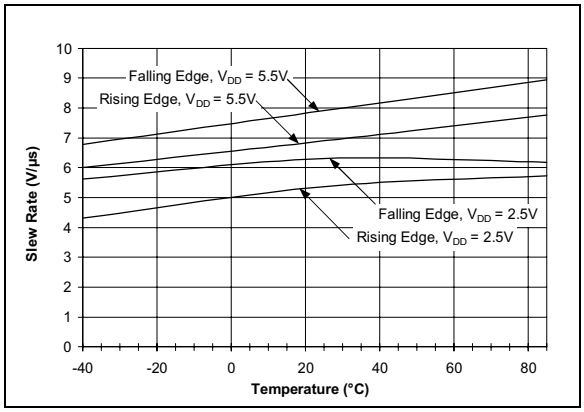


FIGURE 2-26: *Slew Rate vs. Temperature vs. Power Supply Voltage.*

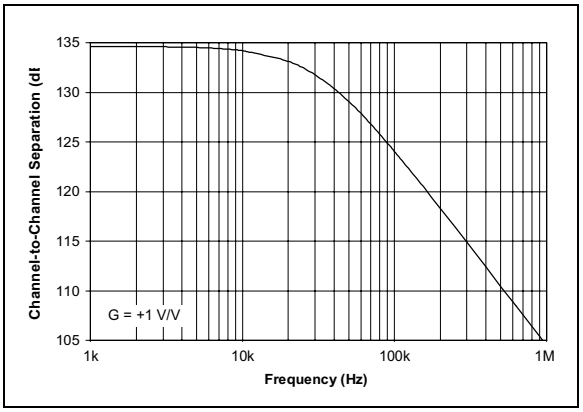


FIGURE 2-29: *Channel–to–Channel Separation vs. Frequency (MCP6022 and MCP6024 only).*

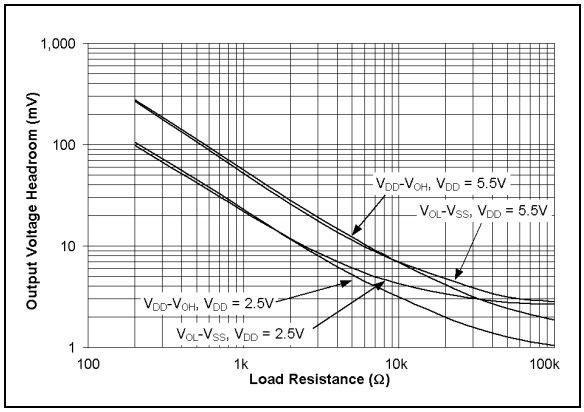


FIGURE 2-27: *Output Voltage Headroom vs. Load Resistance vs. Power Supply Voltage.*

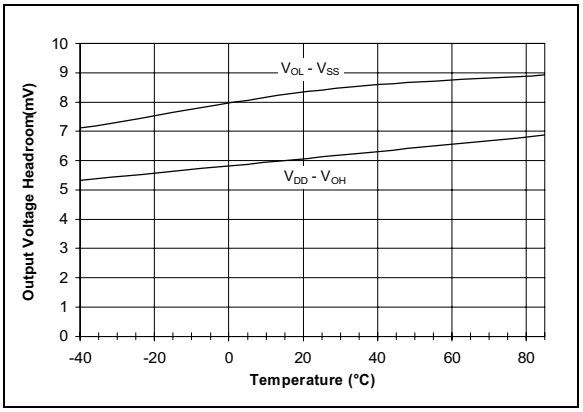


FIGURE 2-30: *Output Voltage Headroom vs. Temperature.*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = +5.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ~ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2, and C_L = 60 pF.

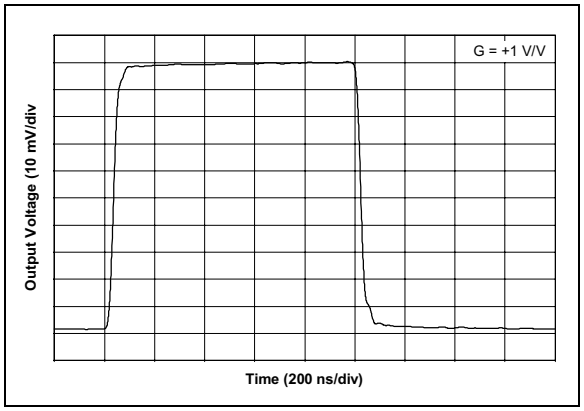


FIGURE 2-31: *Small Signal Non-inverting Pulse Response.*

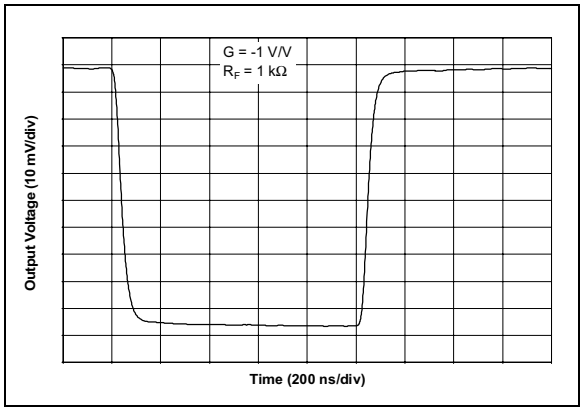


FIGURE 2-34: *Small Signal Inverting Pulse Response.*

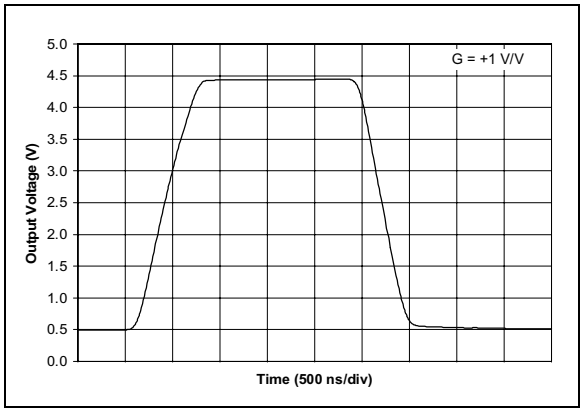


FIGURE 2-32: *Large Signal Non-inverting Pulse Response.*

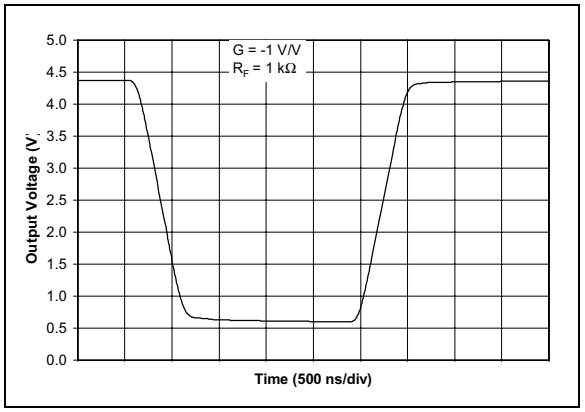


FIGURE 2-35: *Large Signal Inverting Pulse Response.*

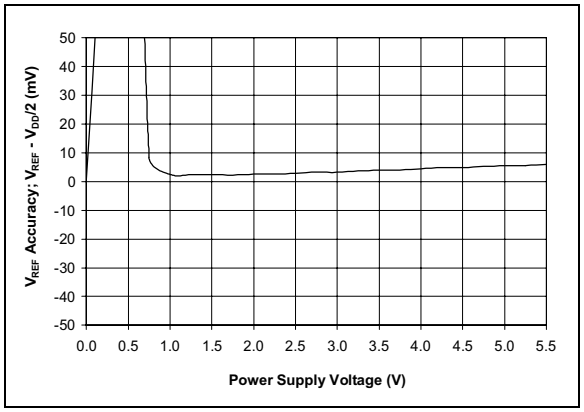


FIGURE 2-33: *V_{REF} Accuracy vs. Power Supply Voltage (MCP6021 and MCP6023 only).*

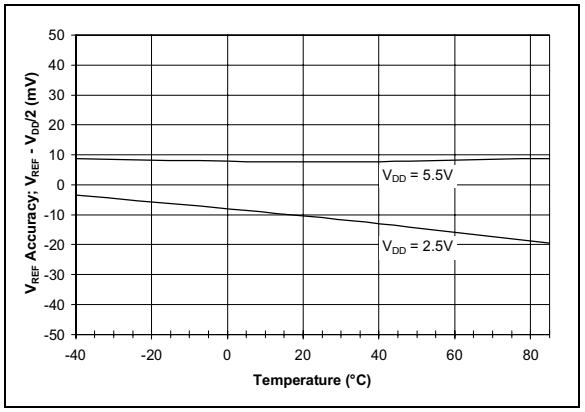


FIGURE 2-36: *V_{REF} Accuracy vs. Temperature (MCP6021 and MCP6023 only).*

Note: Unless otherwise indicated, T_A = 25°C, V_{DD} = +5.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ~ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2, and C_L = 60 pF.

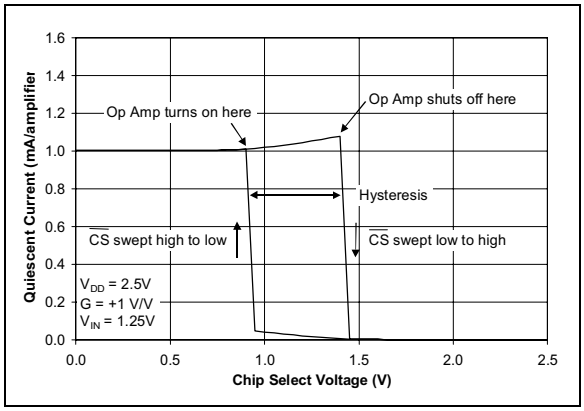


FIGURE 2-37: *Chip Select ($\overline{CS}$) Hysteresis (MCP6023 only) with V_{DD} = 2.5V.*

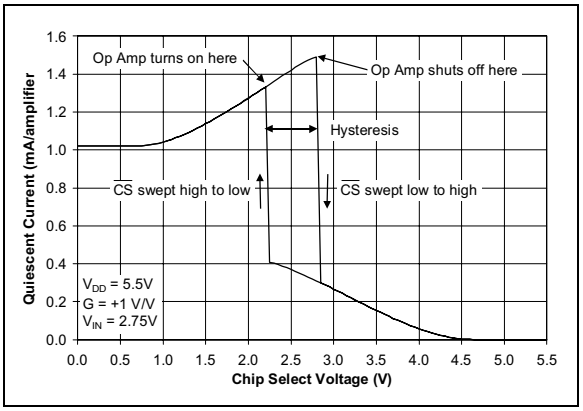


FIGURE 2-39: *Chip Select ($\overline{CS}$) Hysteresis (MCP6023 only) with V_{DD} = 5.5V.*

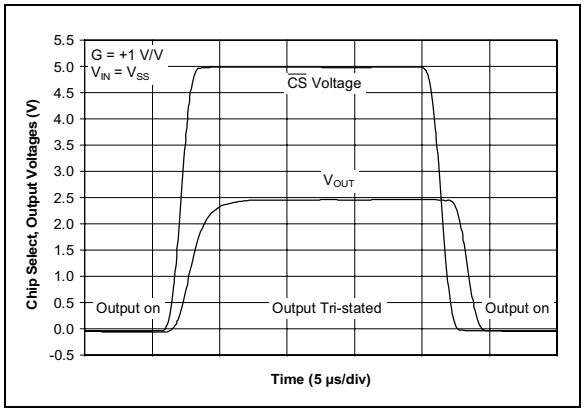


FIGURE 2-38: *Chip Select ($\overline{CS}$) to Amplifier Output Response Time (MCP6023 only).*

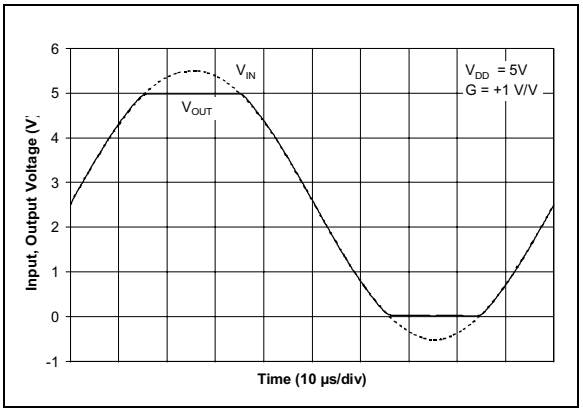


FIGURE 2-40: *The MCP6021/2/3/4 family shows no phase reversal under overdrive.*

3.0 APPLICATIONS INFORMATION

3.1 Rail-to-Rail Input

The input stage of the MCP6021/2/3/4 family of devices uses two differential input stages in parallel; one operates at low V_{CM} (common mode input voltage), and the other at high V_{CM}. With this topology, these op amps still operate with V_{CM} up to 0.3V past either supply rail. The input offset voltage is measured at both $V_{CM} = V_{SS}$-0.3V and V_{DD}+0.3V to ensure proper operation.

3.2 Rail-to-Rail Output

The Maximum Output Voltage Swing is the maximum swing possible under a particular output load. According to the spec table, the output can reach within 20 mV of either supply rail when R_L = 10 kΩ. See Figures 2-27 and 2-30 for more information on typical performance.

3.3 Input Voltage and Phase Reversal

The MCP6021/2/3/4 amplifier family is designed with CMOS input devices. It is designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 3-1 shows an input voltage exceeding both supplies with no resulting phase inversion.

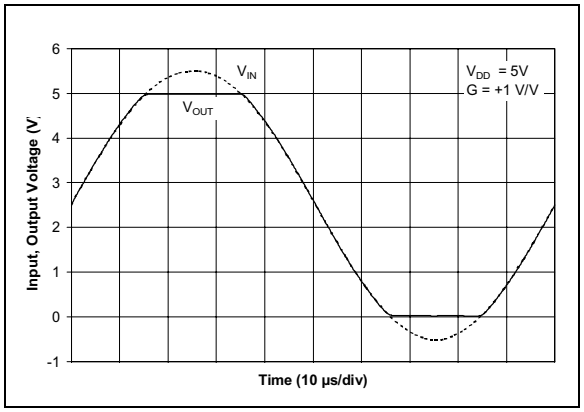


FIGURE 3-1: *The MCP6021/2/3/4 family shows no phase reversal under overdrive.*

The maximum operating common-mode voltage that can be applied to the inputs is V_{SS} - 0.3V to V_{DD} + 0.3V. Voltages on the input that exceed this absolute maximum rating can cause excessive current to flow in or out of the input pins. Current beyond ±2 mA can cause possible reliability problems. Applications that exceed this rating must be externally limited with an input resistor as shown in Figure 3-2.

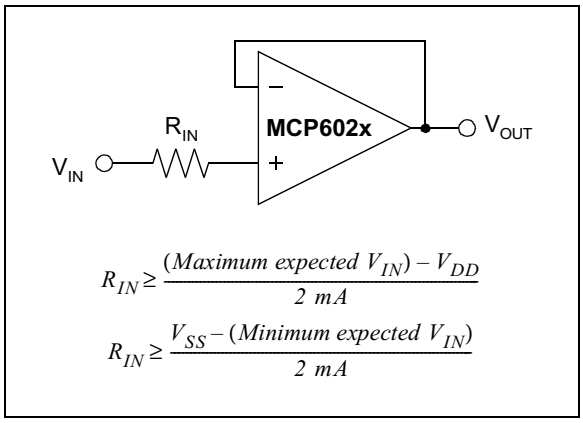


FIGURE 3-2: *R_{IN} limits the current flow into an input pin.*

3.4 Capacitive Load and Stability

Driving capacitive loads can cause stability problems, and reduced bandwidth, for voltage feedback op amps. A buffer configuration (G = +1V/V) is the most sensitive to capacitive loads. Figure 3-3 shows how increasing the load capacitance will decrease the phase margin and the unity gain crossover frequency (where the feedback loop gain is unity, and where phase margin is measured for G = +1 V/V).

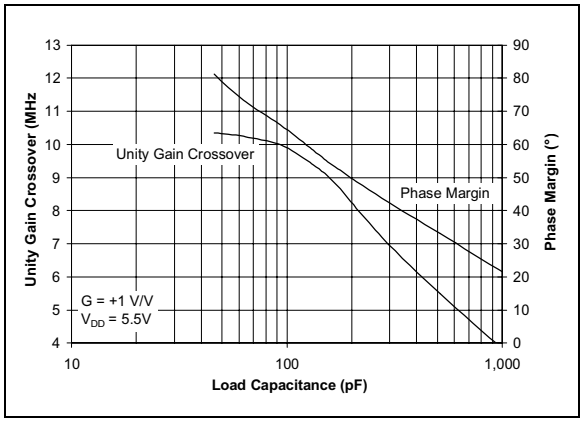


FIGURE 3-3: *Unity Gain Crossover Frequency, Phase Margin vs. Load Capacitance with V_{DD} = 5.5V.*

For non-inverting (inverting) gain op amp circuits, a phase margin (θ_M) of 45° gives about 25% overshoot in the step response, and $\theta_M \geq 65°$ gives little overshoot. With $\theta_M \geq 65°$, layout and component parasitics should not degrade the circuit performance. At a minimum, keep $\theta_M \geq 45°$.

If the amplifier is required to drive larger capacitive loads, the circuit shown in Figure 3-5 can be used. A small series resistor (R_{ISO}) at the output of the amplfiier improves the phase margin by making the load more resistive at high frequencies. It will not, however, improve the bandwidth.

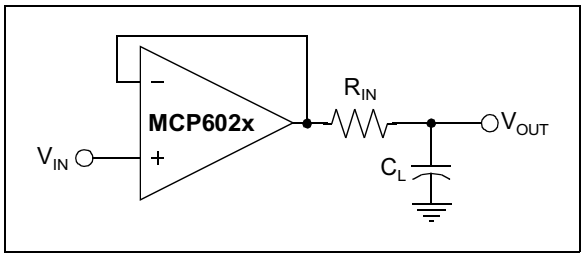


FIGURE 3-4: *Amplifier circuit that stabilizes large capacitive loads.*

The recommended values for R_{ISO} are shown in Figure 3-5. The x-axis is the load capacitance (C_L) divided by the equivalent non-inverting gain G.

For inverting gains, use

$$G = 1 + |\text{"inverting gain"}|$$

(e.g., G = +2 for an inverting gain of -1). The values in Figure 3-5 give a nearly flat frequency response with maximum bandwidth.

Parasitic capacitances in the circuit, such as the op amp input capacitances, may significantly increase the desired value of R_{ISO}. Keep the resistor values low to avoid this effect, and verify your circuit on the bench.

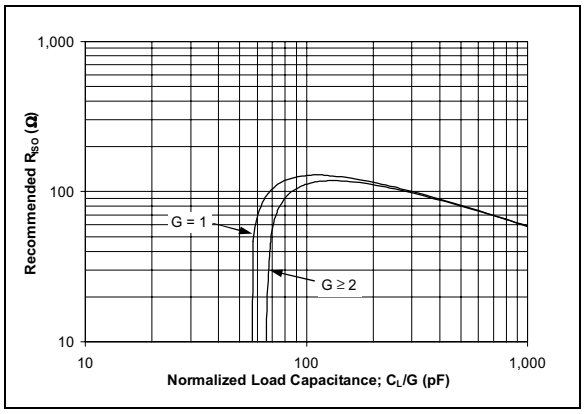


FIGURE 3-5: *Recommended R_{ISO} values for different capacitive loads and gains.*

3.5 Chip Select ($\overline{CS}$) on the MCP6023

The MCP6023 is a single amplifier with a chip select option. When $\overline{CS}$ is pulled high, the supply current drops to less than 50 nA (typ), and is pulled through the $\overline{CS}$ pin to V_{SS}. When this happens, the amplifier output is put into a high impedance state. By pulling $\overline{CS}$ low, the amplifier is enabled. If the $\overline{CS}$ pin is left floating, the amplifier may not operated properly. Figure 3-6 shows the output voltage and supply current response to a $\overline{CS}$ pulse.

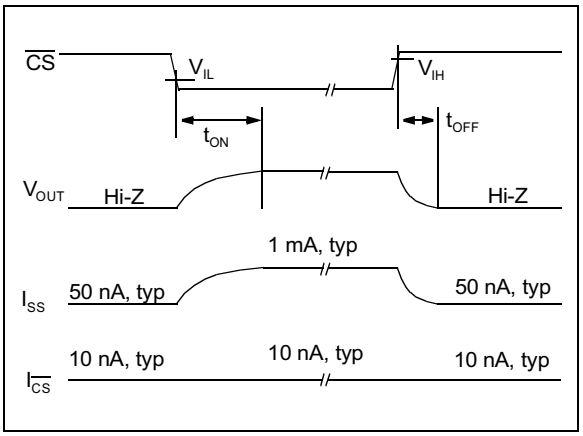


FIGURE 3-6: *Timing diagram for the $\overline{CS}$ pin on the MCP6023.*

3.6 Reference Voltage on the MCP6021 and MCP6023

The single op amps (MCP6021 and MCP6023) have an internally supplied mid-supply reference voltage connected to the V_{REF} pin. Figure 3-7 is a simplified diagram of the internal circuitry. For the MCP6021, $\overline{CS}$ is internally tied to V_{SS}, which always keeps the op amp on, and always provides a mid-supply reference. With the MCP6023, taking the $\overline{CS}$ pin high conserves power by shutting down both the op amp and the V_{REF} circuitry. Taking the $\overline{CS}$ pin low turns on the op amp and V_{REF} circuitry.

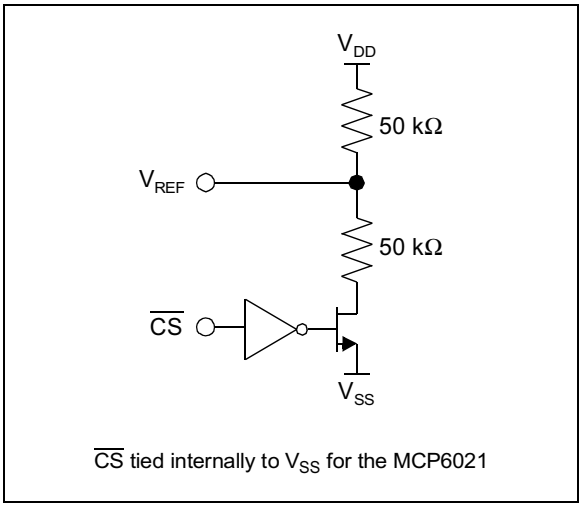


FIGURE 3-7: *Simplified internal V_{REF} circuit (MCP6021 and MCP6023 only).*

For a non-inverting gain circuit using the internal mid-supply reference, see Figure 3-9A. The DC-blocking capacitor (C_B) also reduces noise by coupling the op amp input to the source. To use the internal mid-supply reference for an inverting gain circuit, just connect the V_{REF} pin to the non-inverting input as shown in

Figure 3-9B. Note the bypass capacitor used to reduce noise. If you do not need the mid-supply reference, just leave the V_{REF} pin open.

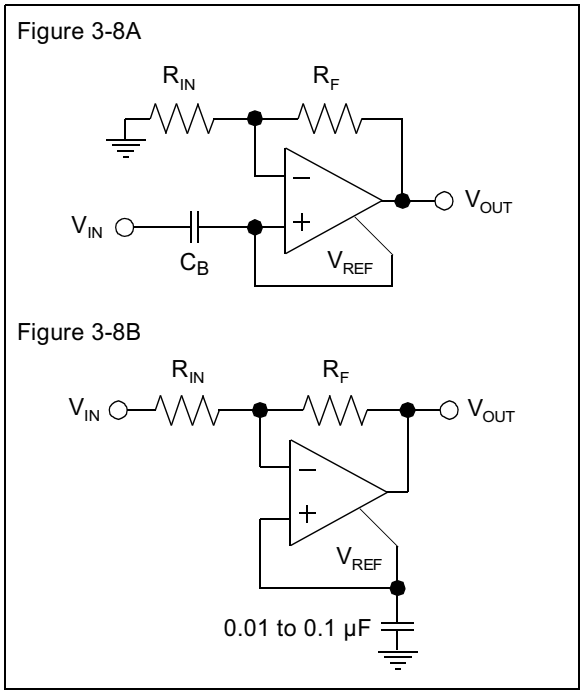


FIGURE 3-8: *Non-inverting and inverting gain circuits using the internal reference voltage V_{REF} (MCP6021 and MCP6023 only).*

3.7 Layout Considerations

Good PC board layout techniques will help you achieve the performance shown in the specs and Typical Performance Curves. It will also help you minimize EMC (Electro-Magnetic Compatibility) issues.

3.7.1 SURFACE LEAKAGE

In applications where low input bias current is critical, PC board surface leakage effects and signal coupling from trace to trace need to be considered.

Surface leakage is caused by a difference in voltage between traces, combined with high humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow; this is greater than the input current of the MCP6021/2/3/4 family at 25°C (1 pA, typ).

The simplest technique to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin; Figure 3-9 shows an example of a typical layout.

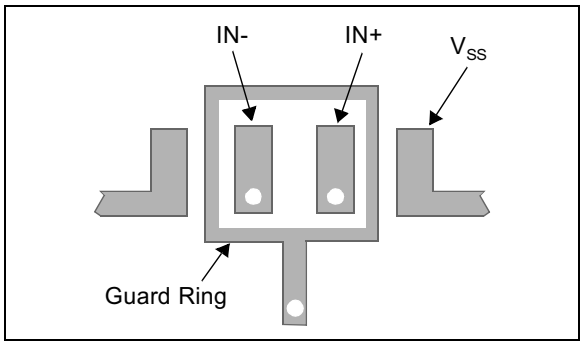


FIGURE 3-9: *Example of a Guard Ring layout.*

Circuit schematics for different guard ring implementations are shown in Figure 3-10. Figure 3-10A biases the guard ring to the input common mode voltage, which is most effective for non-inverting gains, including unity gain. Figure 3-10B biases the guard ring to a reference voltage (V_{REF}, which can be ground). This is useful for inverting gains and precision photo sensing circuits.

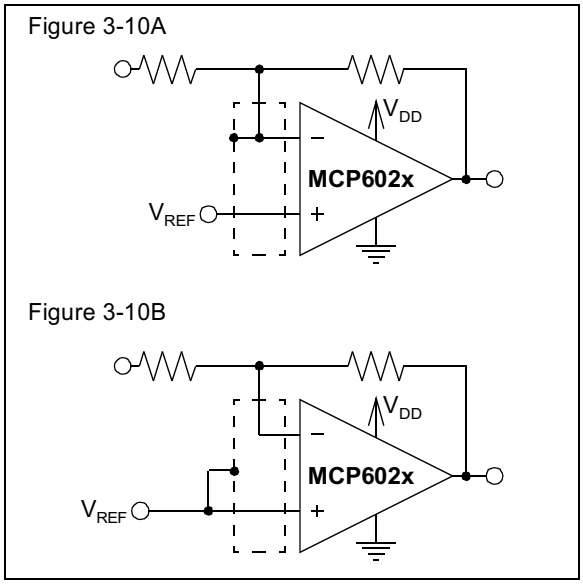


FIGURE 3-10: *Two possible guard ring connection strategies to reduce surface leakage effects.*

3.7.2 COMPONENT PLACEMENT

Separate digital from analog, low speed from high speed, and low power from high power. This will reduce crosstalk.

Keep sensitive traces short and straight. Separate them from interfering components and traces. This is especially important for high frequency (low rise time) signals.

Use a 0.1 µF supply bypass capacitor within 0.1" (2.5mm) of the V_{DD} pin. It must connect directly to the ground plane.

3.7.3 SIGNAL COUPLING

The input pins of the MCP6021/2/3/4 family of op amps are high impedance, which allows noise injection. This noise can be capacitively or magnetically coupled. In either case, using a ground plane helps reduce noise injection.

When the noise is coupled capacitively, the ground plane provides additional shunt capacitance from each trace to ground; Figure 3-11 shows the equivalent circuit. Placing a small resistor (or large capacitor) from Trace 2 to ground will help attenuate the coupled signal.

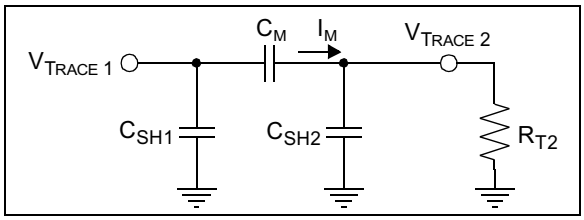


FIGURE 3-11: *Equivalent circuit for capacitive coupling between traces on a PC board with ground plane.*

When noise is coupled magnetically, ground plane reduces the mutual inductance between traces. Increasing the separation between traces makes a significant difference. Changing the direction of one of the traces can also reduce magnetic coupling.

If these techniques are not enough, it may help to place guard traces next to the victim trace. They should be on both sides of the victim trace, and as close as possible. Connect the guard traces to ground plane at both ends, and in the middle for long traces.

3.8 Typical Applications

3.8.1 A/D CONVERTER DRIVER AND ANTI-ALIASING FILTER

Figure 3-12 shows a 5th order Bessel filter that can be used as an A/D converter driver. It has a bandwidth of 20 kHz, and an excellent step response. It will work well for conversion rates of 80 ksps and greater (it has 28 dB attenuation at 60 kHz).

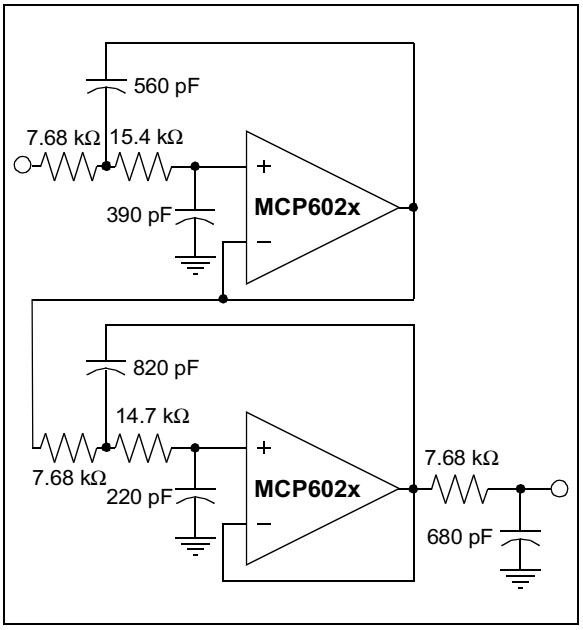


FIGURE 3-12: *A/D converter driver and anti-aliasing filter with a 20 kHz cutoff frequency.*

This filter can easily be adjusted to another bandwidth by multiplying all capacitors by the same factor. Alternatively, the resistors can all be scaled by another common factor to adjust the bandwidth.

3.8.2 OPTICAL DETECTOR AMPLIFIER

Figure 3-13 shows the MCP6021 op amp used as a transimpedance amplifier in a photo detector circuit. The photo detector looks like a capacitive current source, so the 100 kΩ resistor gains the input signal to a reasonable level. The 5.6 pF capacitor stabilizes this circuit, and produces a flat frequency response with a bandwidth of 370 kHz.

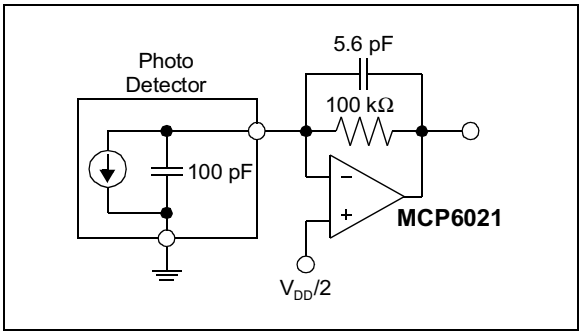


FIGURE 3-13: *Transimpedance amplifier for an optical detector.*

4.0 SPICE MACROMODEL

The SPICE macromodel for the MCP6021, MCP6022, MCP6023, and MCP6024 simulates the typical amplifier performance of: offset voltage, DC power supply rejection, input capacitance, DC common mode rejection, open loop gain over frequency, phase margin, output swing, DC power supply current, input common mode range, output voltage range vs. load, and input voltage noise.

The characteristics of these devices are similar in terms of performance and behavior. This single op amp macromodel supports all four devices with the exception of the chip select function of the MCP6023, which is not modeled.

The listing for this macromodel is shown on the next page. the most recent revision of the model can be downloaded from Microchip's web site at www.microchip.com.

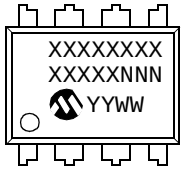
```
.SUBCKT MCP6021 1 2 3 4 5
*               | | | | |
*               | | | | Output
*               | | | Negative Supply
*               | | Positive Supply
*               | Inverting Input
*               Non-inverting Input
*
* Macromodel for the MCP6021/2/3/4 op amp family:
*   MCP6021 (single)
*   MCP6022 (dual)
*   MCP6023 (single w/ CS; chip select is not modeled)
*   MCP6024 (quad)
*
* Revision History:
*   REV A: 10-02-01 created KEB
*
* Recommendations:
*   Use PSPICE (or SPICE 2G6; other simulators may require translation)
*   For a quick, effective design, use a combination of: data sheet
*     specs, bench testing, and simulations with this macromodel
*   For high impedance circuits, set GMIN=100F in the .OPTIONS
*     statement
*
* Supported:
*   Typical performance at room temperature (25 degrees C)
*   DC, AC, Transient, and Noise analyses.
*   Most specs, including: offsets, DC PSRR, DC CMRR, input impedance,
*     open loop gain, voltage ranges, supply current, ... , etc.
*
* Not Supported:
*   Chip Select (MCP6023)
*   Variation in specs vs. Power Supply Voltage
*   Distortion (detailed non-linear behavior)
*   Temperature analysis
*   Process variation
*   Behavior outside normal operating region
*
* Input Stage
V10  3 10 -0.6
R10 10 11 1.63K
R11 10 12 1.63K
C11 11 12 222F
C12  1  0 6P
E12  1 14 POLY(2) 26 0 27 0   0 1 1
I12 14  0 1.5P
M12 11 14 15 15 NMI
C13 14  2 3P
M14 12  2 15 15 NMI
I14  2  0 0.5P
C14  2  0 6P
```

```
I15 15  4 500U
V16 16  4 0.36
D16 16 15 DL
V13  3 13 -80M
D13 14 13 DL
*
* PSRR and CMRR
G26  0 26 POLY(1) 3 4   -308U 56U
R26 26  0 1
G27  0 27 POLY(2) 1 3 2 4   -240U 24U 24U
R27 27  0 1
*
* Open Loop Gain, Slew Rate
G30  0 30 POLY(1) 12 11   0 1K
R30 30  0 1
D31 30 31 DL
E31 31  0 POLY(1) 3 4   57.2 8.33
D32 32 30 DL
E32  0 32 POLY(1) 3 4   74.0 8.00
G33  0 33 POLY(1) 30 0   0 316
R33 33  0 1
C33 33  0 4.58M
G34  0 34 POLY(1) 33 0   0 1
R34 34  0 1
C34 34  0 159P
*
* Output Stage
G40  0 40 POLY(1) 47 5   0 10
D41 40 41 DL
R41 41  0 1K
D42 42 40 DL
R42 42  0 1K
G43  3  0 POLY(1) 41 0   500U  1M
G44  0  4 POLY(1) 42 0   500U -1M
D45 47 45 DLS
E45 45  0 POLY(2) 3 0 41 0   -20M 1 -20.4M
E46 46  0 POLY(2) 4 0 42 0    20M 1 -20.4M
D46 46 47 DLS
G47  0 47 POLY(3) 3 0 4 0 34 0   0 8M 8M 16M
R47 47  0 62.5
R48 47  5 0.1
C48  5  0 2P
*
* Models
.MODEL NMI NMOS L=2 W=75 AF=1 KF=0.1F
.MODEL DL   D N=1   IS=1F
.MODEL DLS  D N=10M IS=1F
*
.ENDS MCP6021
```

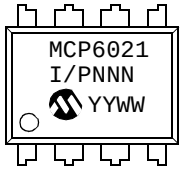
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

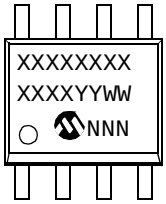
8-Lead PDIP (300 mil)



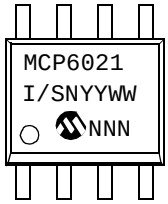
Example:



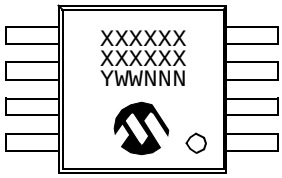
8-Lead SOIC (150 mil)



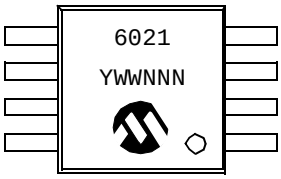
Example:



8-Lead TSSOP



Example:



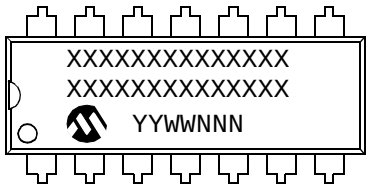
Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

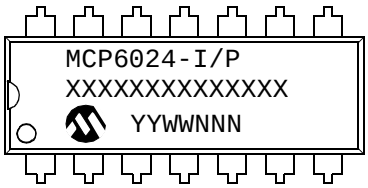
***** Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

Package Marking Information (Continued)

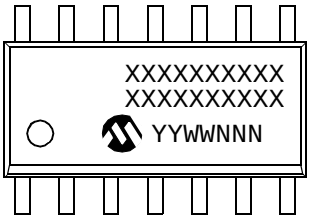
14-Lead PDIP (300 mil) (MCP6024)



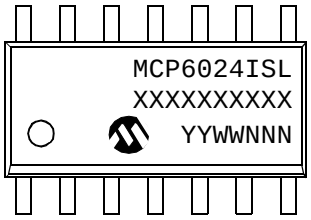
Example:



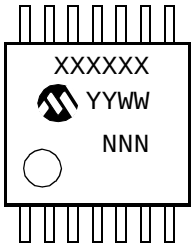
14-Lead SOIC (150 mil) (MCP6024)



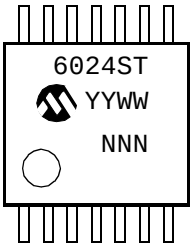
Example:



14-Lead TSSOP (MCP6024)



Example:

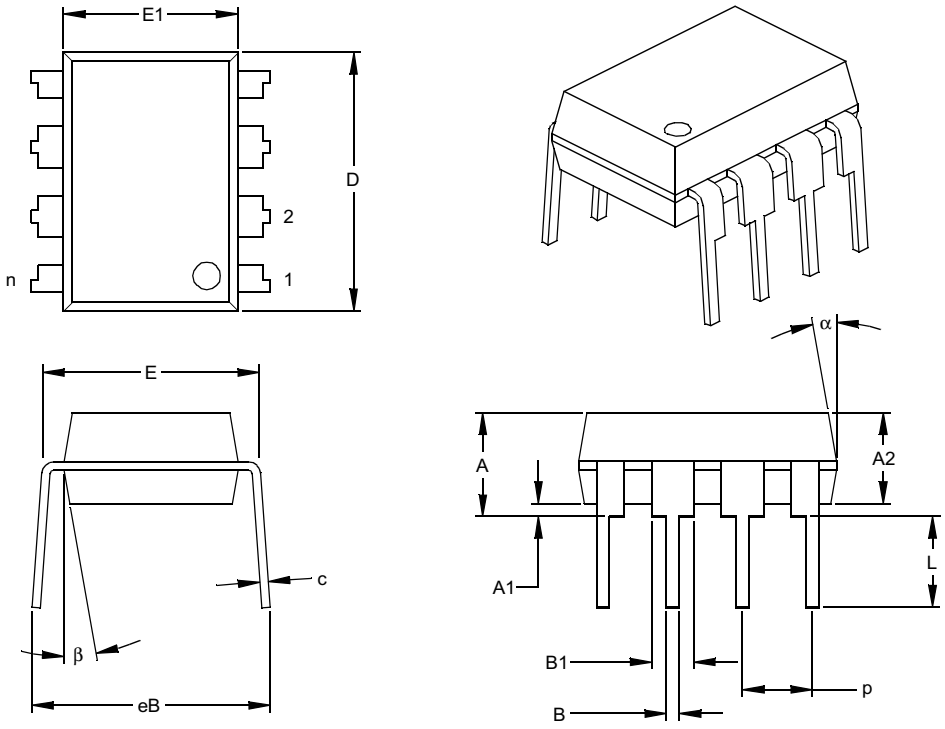


Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

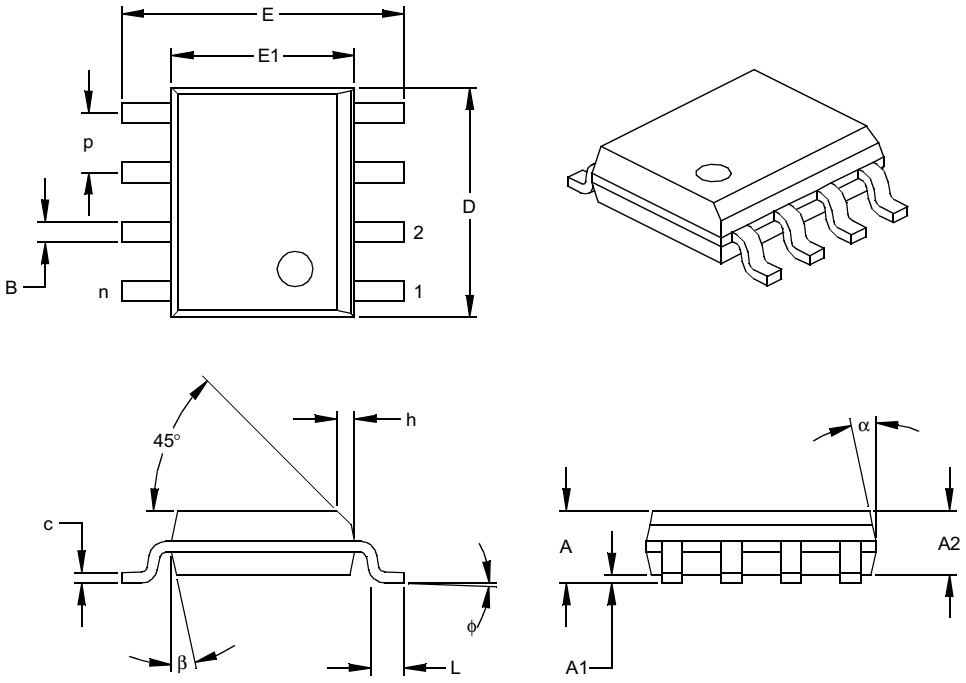


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

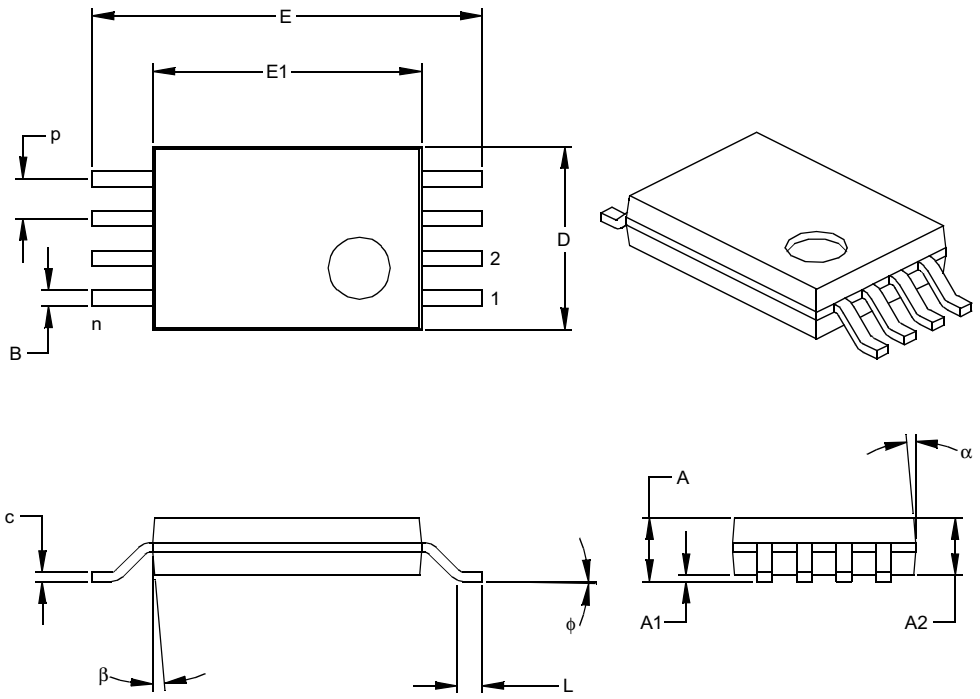


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)

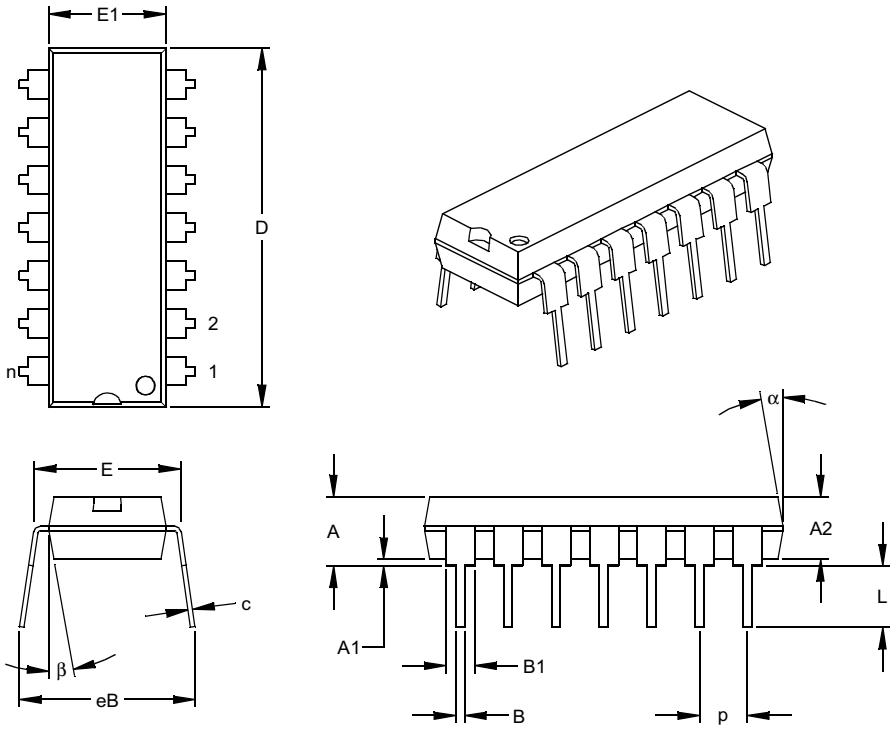


Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-086

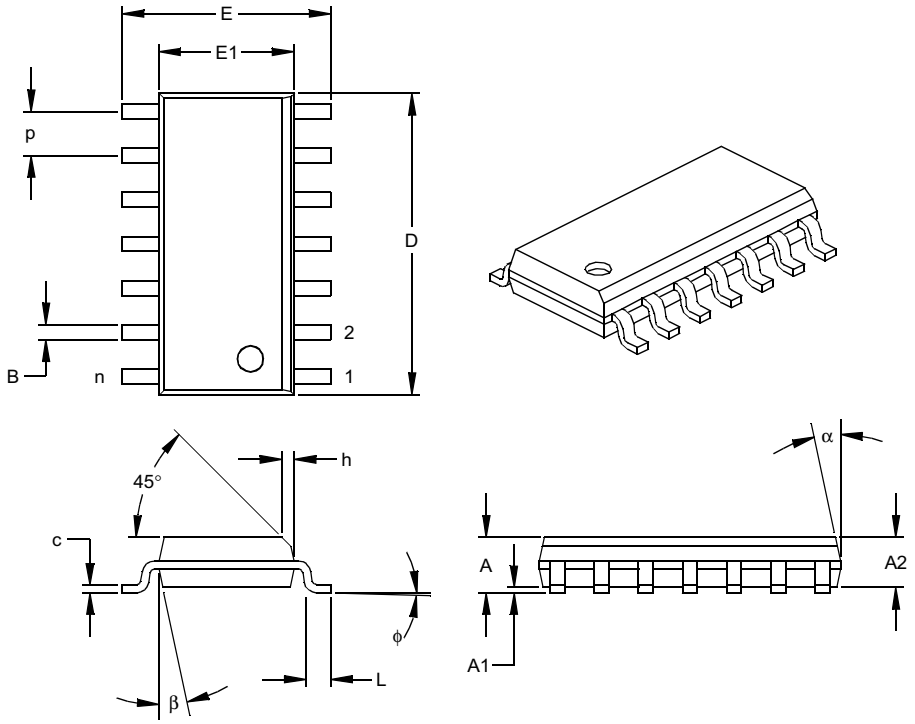
14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-005

14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)

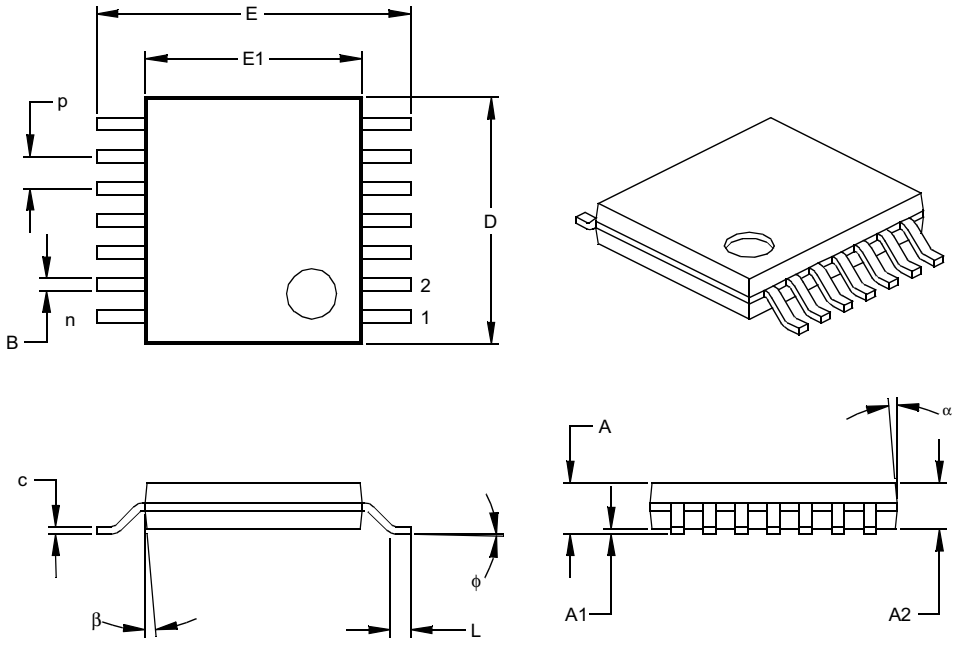


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-065

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B1	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-087

NOTES:

ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web (WWW) site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape or Microsoft Explorer. Files are also available for FTP download from our FTP site.

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The Microchip web site is available by using your favorite Internet browser to attach to:

www.microchip.com

The file transfer site is available by using an FTP service to connect to:

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The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

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013001

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Device: **MCP6021/2/3/4** Literature Number: **DS21685A**

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this data sheet easy to follow? If not, why?

4. What additions to the data sheet do you think would enhance the structure and subject?

5. What deletions from the data sheet could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

8. How would you improve our software, systems, and silicon products?

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP6021	CMOS Single Op Amp
	MCP6021T	CMOS Single Op Amp (Tape and Reel for SOIC, TSSOP)
	MCP6022	CMOS Dual Op Amp
	MCP6022T	CMOS Dual Op Amp (Tape and Reel for SOIC and TSSOP)
	MCP6023	CMOS Single Op Amp w/ $\overline{CS}$ Function
	MCP6023T	CMOS Single Op Amp w/ $\overline{CS}$ Function (Tape and Reel for SOIC and TSSOP)
	MCP6024	CMOS Quad Op Amp
	MCP6024T	CMOS Quad Op Amp (Tape and Reel for SOIC and TSSOP)
Temperature Range:	I =	-40°C to +85°C
Package:	P =	Plastic DIP (300 mil Body), 8-lead, 14-lead
	SN =	Plastic SOIC (150mil Body), 8-lead
	SL =	Plastic SOIC (150 mil Body), 14-lead
	ST =	Plastic TSSOP, 8-lead, 14-lead

Examples:

a) MCP6021-I/P: Industrial temperature, PDIP package.

b) MCP6021-I/SN: Industrial temperature, SOIC package.

c) MCP6022-I/P: Industrial temperature, PDIP package.

d) MCP6022T-I/ST: Tape and Reel, Industrial temperature, TSSOP package.

e) MCP6023-I/P: Industrial temperature, PDIP package.

f) MCP6023-I/SN: Industrial temperature, SOIC package.

g) MCP6024-I/SL: Industrial temperature, SOIC package.

h) MCP6024T-I/ST: Tape and Reel, Industrial temperature, TSSOP package.

Sales and Support

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
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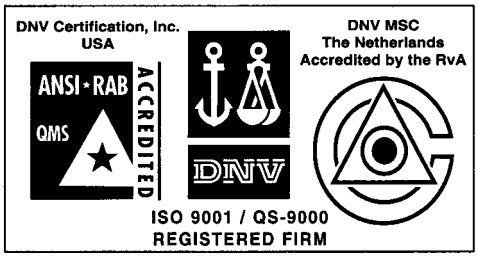
Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System
Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

NOTES:

Trademarks



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