SGS-THOMSON MICROELECTRONICS

MK41H80(N,P)-20/25/35

4K × 4 CMOS TAGRAM™

- 4K × 4 SRAM WITH ONBOARD 4 BIT COMPARATOR
- 20, 25, AND 35ns ADDRESS TO COMPARE ACCESS TIME
- 12, 15, AND 20ns TAG DATA TO COMPARE ACCESS TIME
- EQUAL ACCESS, READ AND WRITE CYCLE TIMES
- FLASH CLEAR FUNCTION
- 22-PIN, 300 MIL PLASTIC AND CERAMIC DIP
- ALL INPUTS AND OUTPUTS ARE TTL COMPATIBLE, LOW CAPACITANCE, AND PROTECTED AGAINST STATIC DISCHARGE
- WORD WIDTH EXPANDABLE

N
DIP-22
(Plastic Package)

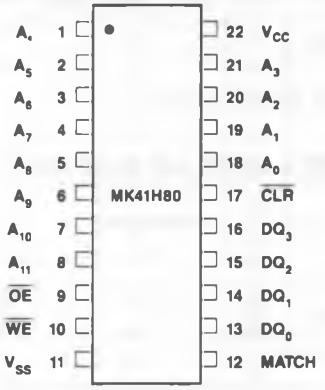
P
DIP-22
(Ceramic Package)

TRUTH TABLE

$\overline{WE}$	$\overline{OE}$	$\overline{CLR}$	MATCH	MODE
H	H	H	Valid	Compare Cycle
L	X	H	Invalid	Write Cycle
H	L	H	Invalid	Read Cycle
X	X	L	Invalid	Flash Clear Cycle

X = Don't Care

FIGURE 1. PIN CONNECTIONS



PIN NAMES

A_0 - A_{11}	- Address Inputs
DQ_0 - DQ_3	- Data Input/Output
MATCH	- Comparator Output
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable
$\overline{CLR}$	- Flash Clear
V_{CC}	- Power (+5V)
V_{SS}	- Ground

DESCRIPTION

The MK41H80 is a member of SGS-THOMSON's 4K × 4 CMOS Static RAM family featuring fully static operation requiring no external clocks or timing strobes. Cycle Time and Compare Access Time are equal. The MK41H80 is powered by a single +5V ±10% power supply and the inputs and outputs are fully TTL compatible.

The MK41H80 features an onboard 4 bit comparator that compares RAM contents and current input data. The result is an active high match on the MATCH pin or an active low miss on the MATCH pin. The MATCH pins of several MK41H80's can be nanded together to provide enabling or acknowledging signals to the data cache or processor.

Tag data can be read from the data pins by bringing Output Enable ($\overline{OE}$) low. This will allow data stored in the memory array to be displayed at the Outputs (DQ_0-DQ_3).

Flash Clear operation is provided on the MK41H80 via the ($\overline{CLR}$) pin. A low applied to the $\overline{CLR}$ pin clears all RAM bits to a logic zero.

FIGURE 2. COMPARE AND WRITE CYCLE

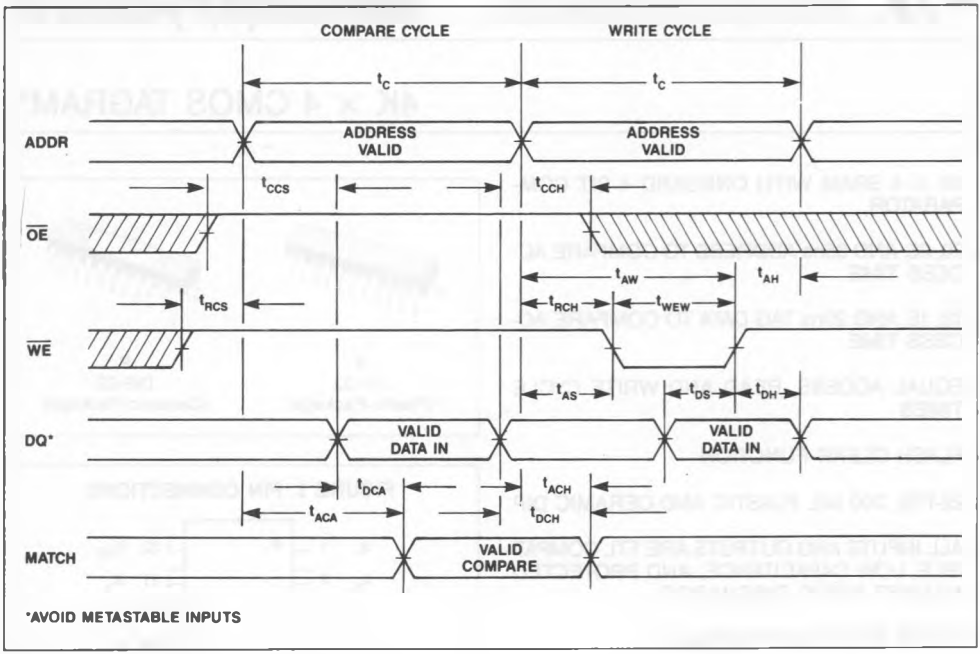
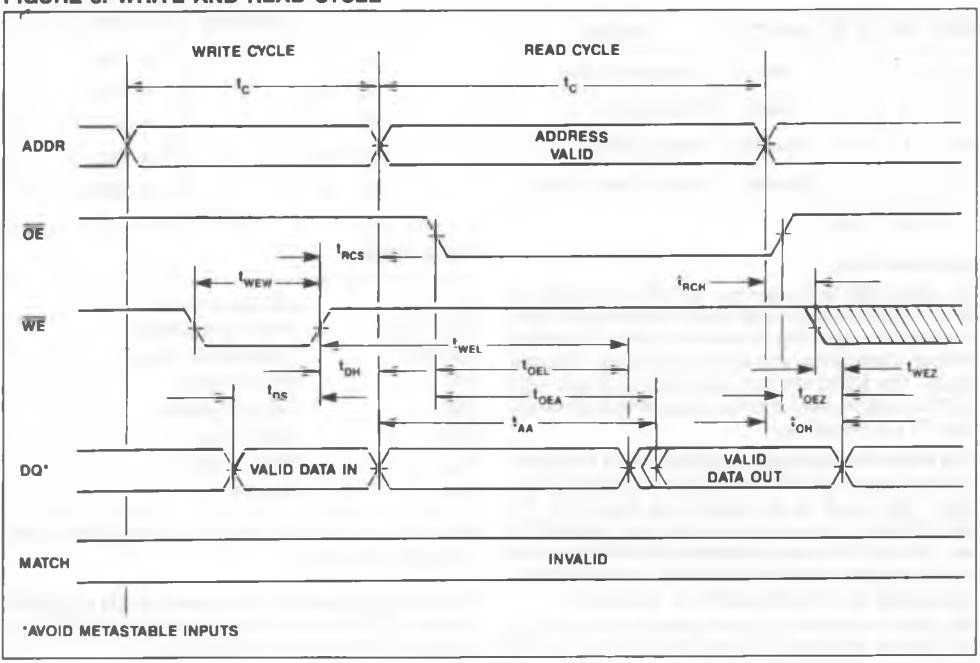


FIGURE 3. WRITE AND READ CYCLE



COMPARE, WRITE AND READ TIMING

The MK41H80 employs three signals for device control. The Write Enable ($\overline{WE}$) pin enables a Write Cycle if low and either a Compare Cycle or a Read Cycle when high. The $\overline{OE}$ pin enables a Read Cycle if low or a Compare Cycle if high. The $\overline{CLR}$ pin enables a Flash Clear Cycle when brought low.

The MK41H80 begins a Compare Cycle with the application of a valid address (see Figure 2). A valid MATCH is enabled when $\overline{OE}$ and $\overline{WE}$ go high in conjunction with their respective Set Up and Hold times. MATCH will occur t_{ACA} after a valid address, and t_{DCA} after valid Data In. MATCH will then go invalid t_{ACH} after the address changes.

The MK41H80 starts a Write Cycle with stable addresses (see Figure 2). $\overline{OE}$ may be in either logic state. $\overline{WE}$ may fall with stable addresses, and must remain low until t_{AW} with a duration of t_{WEW}. Data in must be held valid t_{DS} before and t_{DH} after $\overline{WE}$ goes high. MATCH will be invalid during this cycle.

The MK41H80 begins a Read Cycle with stable addresses and $\overline{WE}$ high (see Figure 3). DQ becomes valid t_{AA} after a valid address, and t_{OEA} after the fall of $\overline{OE}$. DQ outputs become invalid t_{OH} after the address becomes invalid or t_{OEZ} after OE is brought high. Ripple through data access may be accomplished by holding $\overline{OE}$ active low while strobing addresses A_0-A_{11}, and holding $\overline{CLR}$ and $\overline{WE}$ high. The MATCH output will be invalid during the Read cycle.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ±10%)

		-20		-25		-35			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_C	Cycle Time	20		25		35		ns	
t_{CCS}	Compare Command Set Up Time	7		8		10		ns	
t_{CCH}	Compare Command Hold Time	0		0		0		ns	
t_{RCS}	Read Command ($\overline{WE}$) Set Up Time	0		0		0		ns	
t_{RCH}	Read Command ($\overline{WE}$) Hold Time	0		0		0		ns	
t_{AS}	Address Set-up Time	0		0		0		ns	
t_{AW}	Address Stable to End of Write Command ($\overline{WE}$)	16		20		30		ns	
t_{AH}	Address Hold Time after End of Write	0		0		0		ns	
t_{WEW}	Write Command ($\overline{WE}$) to End of Write	16		20		30		ns	
t_{DS}	Data Set Up Time	12		13		14		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{DCA}	Data Compare Access Time		12		15		20	ns	3
t_{ACA}	Address Compare Access Time		20		25		35	ns	3
t_{ACH}	Address Compare Hold Time	5		5		5		ns	3
t_{DCH}	Data Compare Hold Time	3		3		3		ns	3
t_{OEA}	Output Enable ($\overline{OE}$) Access Time		10		12		15	ns	3
t_{OH}	Valid Data Out ($\overline{DQ}$) Hold Time	5		5		5		ns	3
t_{AA}	Address Access Time		20		25		35	ns	3
t_{OEZ}	Output Enable ($\overline{OE}$) to High-Z		7		8		10	ns	4
t_{OEL}	Output Enable ($\overline{OE}$) to Low-Z	2		2		2		ns	4
t_{WEZ}	Write Enable ($\overline{WE}$) to High-Z		8		10		13	ns	4
t_{WEL}	Write Enable ($\overline{WE}$) to Low-Z	5		5		5		ns	4

APPLICATION

The MK41H80 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the MK41H80 can also interface to 5 volt CMOS on all inputs and outputs. Refer to the normalized performance curves that follow.

The MK41H80 compares contents of addressed RAM locations to the current data inputs. A logic one (1) output on the MATCH pin indicates that the input data and the RAM contents match. Conversely, a logic zero (0) on the MATCH pin indicates at least one bit difference between the RAM contents and input data generating a miss.

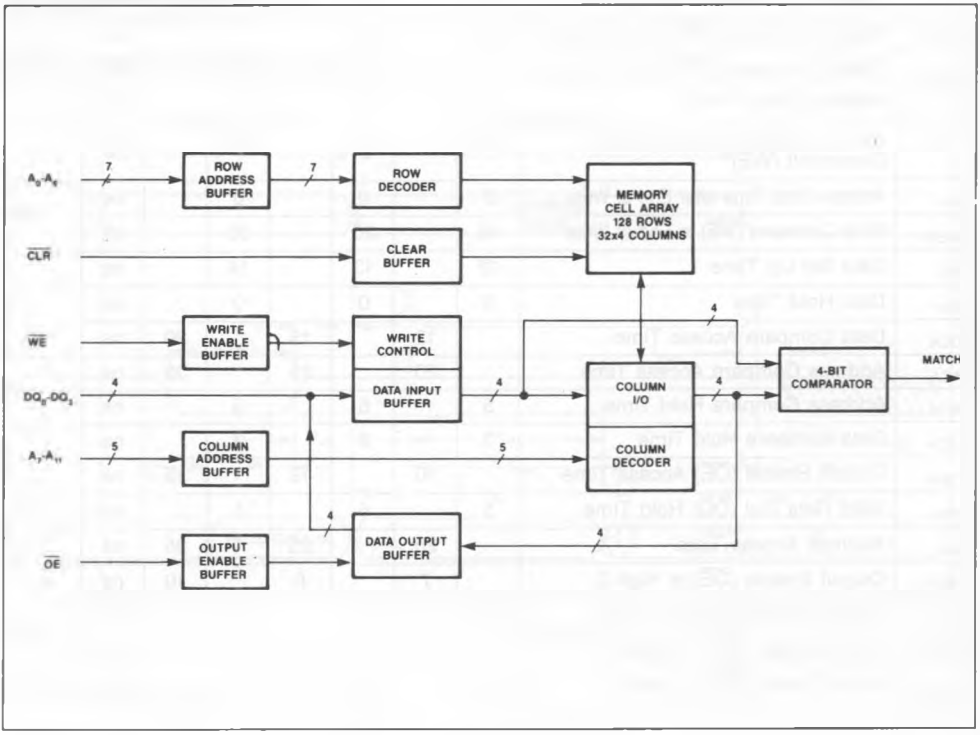
The MATCH output is always at either an active high or low logic level, and does not exhibit a three-state or high impedance characteristic. Since the comparator circuitry is always enabled, metastable data input levels can result in excessive MATCH output activity. Therefore, the use of pull-up or pull-down resistors is recommended on the data bus.

A pull-up resistor is also recommended for the $\overline{CLR}$ input. This will ensure that any low going system noise, coupled onto the input, does not drive $\overline{CLR}$ below V_{IH} minimum specifications.

Because high frequency current transients will be associated with the operation of the MK41H80, power lines inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

FIGURE 4. BLOCK DIAGRAM



FLASH CLEAR CYCLE

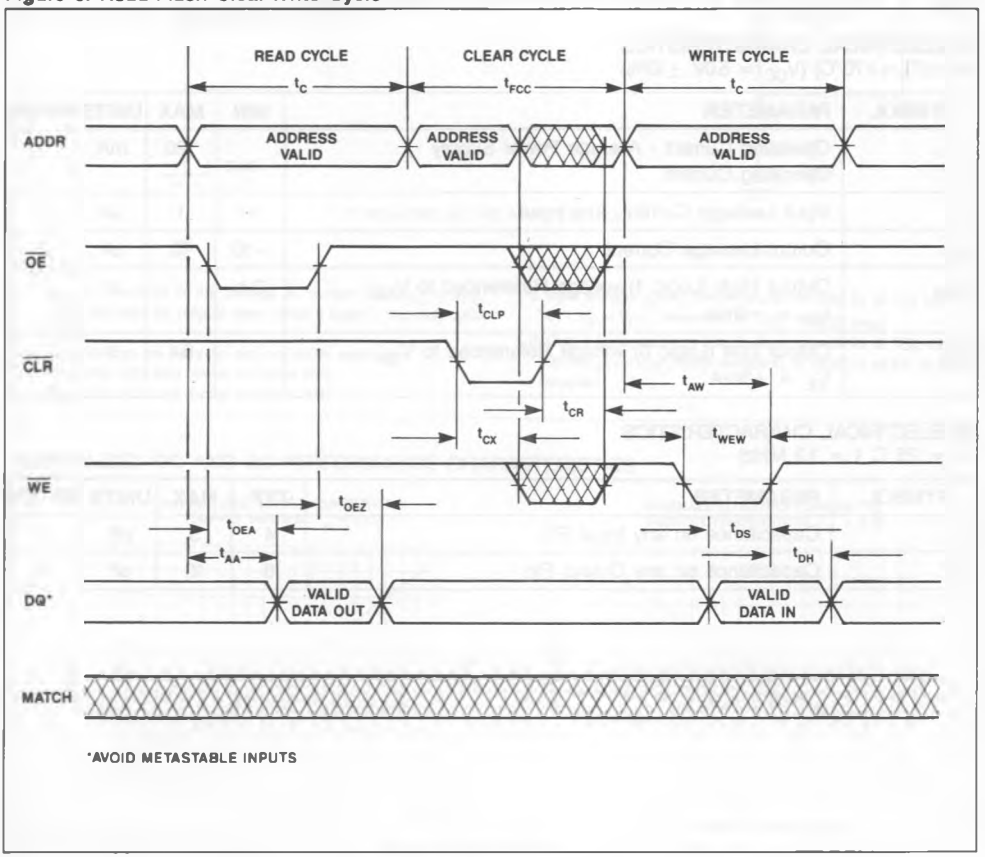
A Flash Clear Cycle begins as $\overline{CLR}$ is brought low (see Figure 5). A Flash Clear sets all 16,384 bits in the RAM to logic zero. Control Inputs will not be recognized from t_{CX} after $\overline{CLR}$ falls to t_{CR} after $\overline{CLR}$ is brought high. $\overline{OE}$ and $\overline{WE}$ are Don't Cares and DQ is High-Z. MATCH will be invalid while $\overline{CLR}$ is low.

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0V ±10%)

		-20		-25		-35			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{FCC}	Flash Clear Cycle Time	40		50		70		ns	
t_{CX}	Clear ($\overline{CLR}$) to Inputs Don't Care	0		0		0		ns	
t_{CR}	End of Clear ($\overline{CLR}$) to Inputs Recognized	0		0		0		ns	
t_{CLP}	Flash Clear ($\overline{CLR}$) Pulse Width	36		44		60		ns	

Figure 5. Read-Flash Clear-Write Cycle



*AVOID METASTABLE INPUTS

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{SS} . . . . . −1.0V to +7.0V
Operating Temperature T_A (Ambient) . . . . . 0°C to +70°C
Storage Temperature (Ceramic) . . . . . −65°C to +150°C
Storage Temperature (Plastic) . . . . . −55°C to +125°C
Power Dissipation . . . . . 1 Watt
Output Current per Pin . . . . . 50 mA

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage (Referenced to V_{SS})	4.5	5.0	5.5	V	
V_{SS}	Ground	0.0	0.0	0.0	V	
V_{IH}	Input High (Logic 1) voltage, All Inputs (Referenced to V_{SS})	2.2		V_{CC} +0.3	V	
V_{IL}	Input Low (Logic 0) voltage, All Inputs (Referenced to V_{SS})	−0.3		0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C) (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Operating Current - Average Power Supply Operating Current		120	mA	1
I_{IL}	Input Leakage Current, Any input	−1	1	µA	5
I_{OL}	Output Leakage Current	−10	10	µA	6
V_{OH}	Output High (Logic 1) voltage Referenced to V_{SS}; I_{OH} = −4mA	2.4		V	
V_{OL}	Output Low (Logic 0) voltage Referenced to V_{SS}; I_{OL} = +8mA		0.4	V	

AC ELECTRICAL CHARACTERISTICS

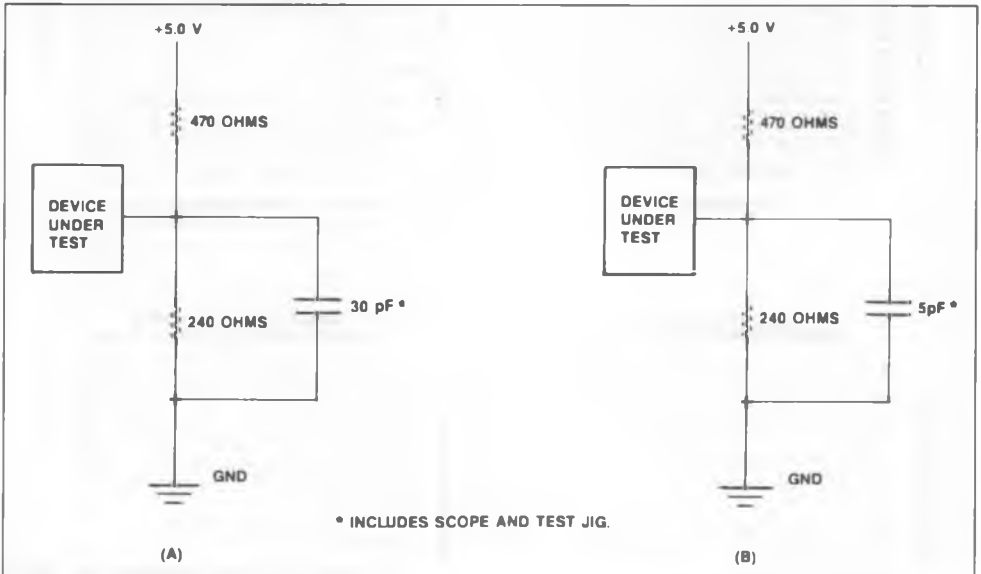
(T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Capacitance on any Input Pin	4	5	pF	2
C_2	Capacitance on any Output Pin	8	10	pF	2

AC TEST CONDITIONS

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input and Output Signal Timing Reference Level	1.5 V
Ambient Temperature	0°C to 70°C
V_{CC}	5.0 V ± 10 percent

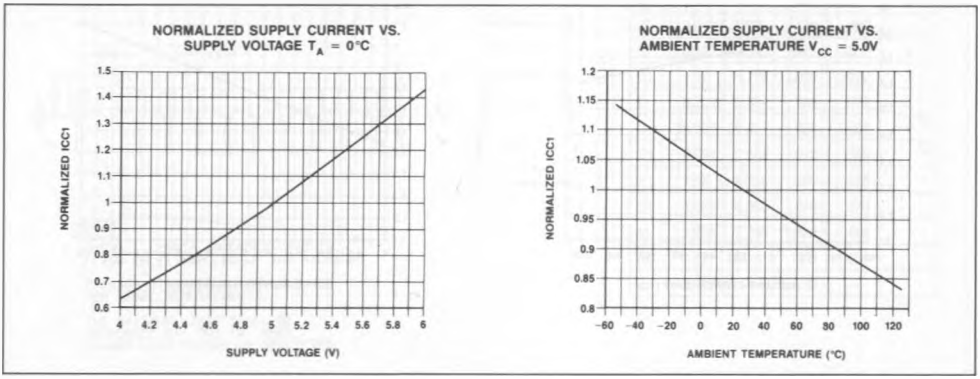
FIGURE 6. OUTPUT LOAD CIRCUITS



NOTES

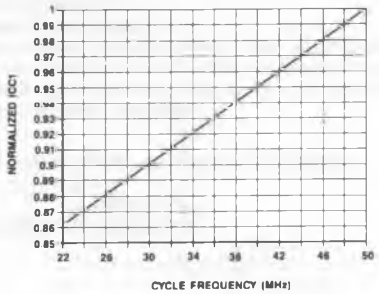
1. I_{CC1} is measured as the average AC current with $V_{CC} = V_{CC}$ (max) and with the outputs open circuit. t cycle = min duty cycle 100%.
2. Capacitances are sampled and not 100% tested.
3. Measured with load shown in Figure 6(A).
4. Measured with load shown in Figure 6(B).
5. Input leakage current specifications are valid for all V_{IN} such that $0V < V_{IN} < V_{CC}$. Measured at $V_{CC} = V_{CC}$ (max).
6. Output leakage current specifications are valid for all DQs such that $0V < V_{OUT} < V_{CC}$. With exception to MATCH which is always enabled.

NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

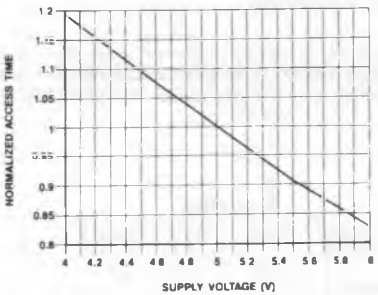


NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

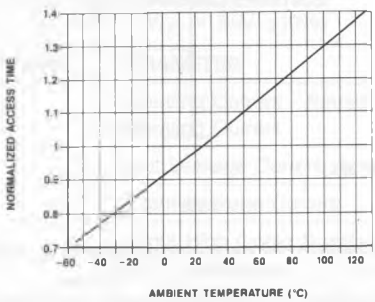
NORMALIZED SUPPLY CURRENT VS. CYCLE TIME V_{CC} = 5.0V T_A = 25°C



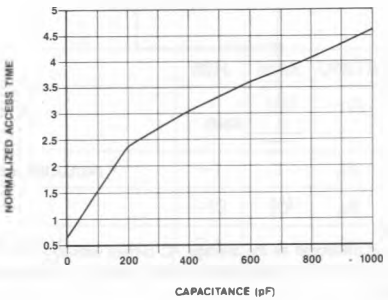
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE T_A = 25°C



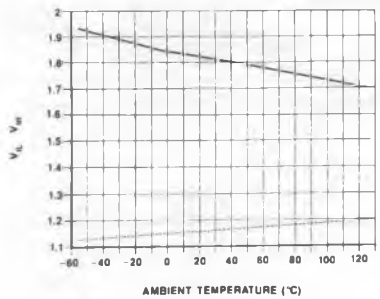
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE V_{CC} = 5.0V



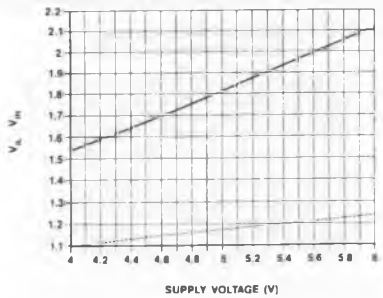
NORMALIZED ACCESS TIME VS. OUTPUT LOADING V_{CC} = 5.0V T_A = 25°C



LOGIC THRESHOLD VOLTAGE VS. AMBIENT TEMPERATURE V_{CC} = 5.0V

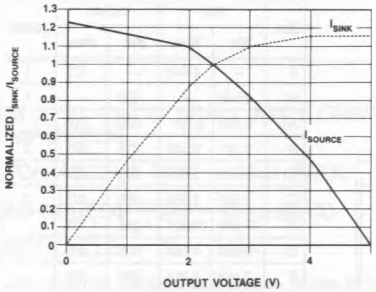


LOGIC THRESHOLD VOLTAGE VS. SUPPLY VOLTAGE T_A = 25°C

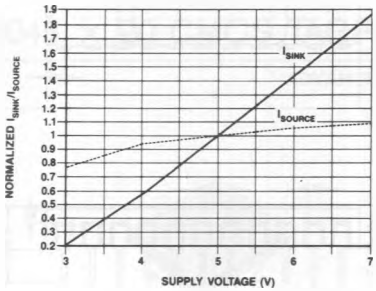


NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

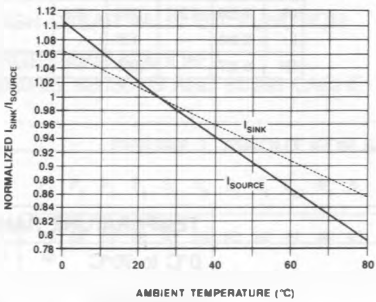
NORMALIZED SOURCE AND SINK CURRENTS VS.
OUTPUT VOLTAGE V_{CC} = 5.0V, T_A = 25°C



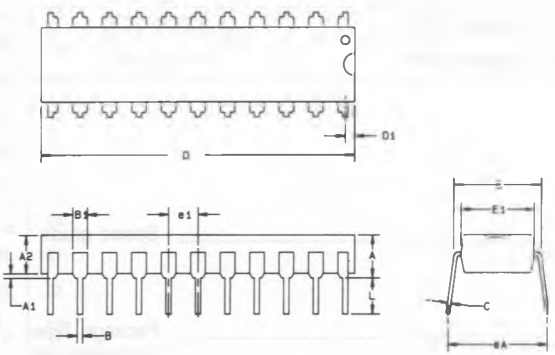
NORMALIZED SOURCE AND SINK CURRENTS VS.
SUPPLY VOLTAGE T_A = 25°C



NORMALIZED SOURCE AND SINK CURRENTS VS.
AMBIENT TEMPERATURE V_{CC} = 5.0V



22 PIN "N" PACKAGE, PLASTIC DIP

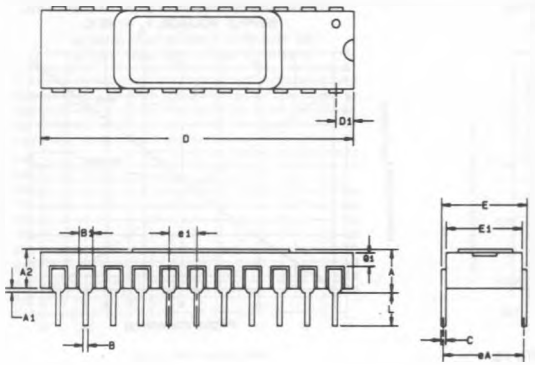


Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	—	5.334	—	.210	2
A1	0.381	—	.015	—	2
A2	3.048	3.556	.120	.140	
B	0.381	0.533	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.008	.012	3
D	25.908	26.67	1.020	1.050	1
D1	0.254	0.635	.010	.025	
E	7.62	8.255	.300	.325	
E1	6.096	6.858	.240	.270	
e1	2.286	2.794	.090	.110	
eA	7.62	10.16	.300	.400	
L	3.048	—	.120	—	

NOTES:

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

22 PIN "P" PACKAGE, SIDE BRAZED CERAMIC DIP



Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	—	4.445	—	.175	1
A1	0.508	—	.020	—	1
A2	2.032	2.794	.080	.110	
B	0.381	0.533	.015	.021	2
B1	0.965	1.447	.038	.057	
C	0.203	0.304	.008	.012	2
D	27.559	28.321	1.085	1.125	
D1	0.889	1.651	.035	.065	
E	7.493	8.255	.295	.325	
E1	7.112	7.874	.280	.310	
e1	2.286	2.794	.090	.110	
eA	7.366	9.271	.290	.365	
L	3.048	—	.120	—	
Q1	0.127	—	.005	—	

NOTES

1. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
2. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED

ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK41H80N-20	20 ns	22 pin Plastic DIP	0°C to 70°C
MK41H80N-25	25 ns	22 pin Plastic DIP	0°C to 70°C
MK41H80N-35	35 ns	22 pin Plastic DIP	0°C to 70°C
MK41H80P-20	20 ns	22 pin Ceramic DIP	0°C to 70°C
MK41H80P-25	25 ns	22 pin Ceramic DIP	0°C to 70°C
MK41H80P-35	35 ns	22 pin Ceramic DIP	0°C to 70°C