

73,728-BIT
 8K X 9 CMOS FAST SRAM

ADVANCE DATA

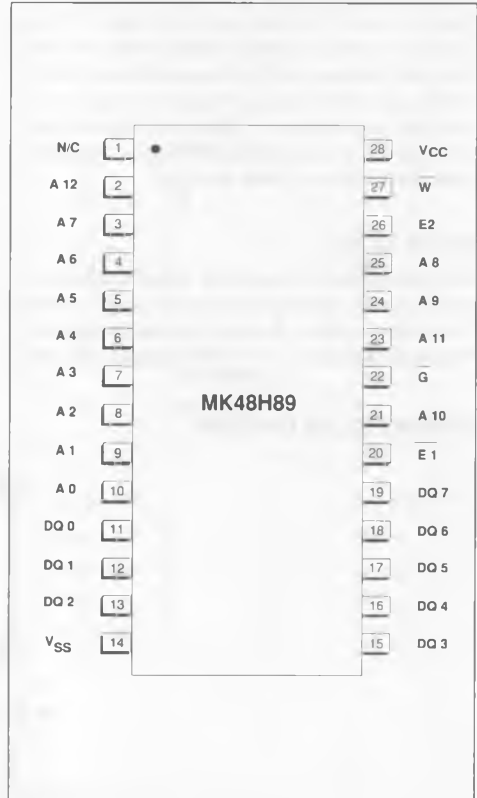
- BYTEWYDE 8K X 9 CMOS FSRAM
- FAST ACCESS TIMES, 20,25,35NS MAX.
- EQUAL ACCESS AND CYCLE TIMES
- LOW V_{CC} DATA RETENTION 2 VOLTS
- THREE STATE OUTPUT
- STANDARD 28-PIN PACKAGE IN 300 MIL PLASTIC DIP

DESCRIPTION

The MK48H89 is a 73,728-bit static RAM, organized as 8K X 9 bits. It is fabricated using SGS-Thomson's low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single + 5V ± 10% supply, and all inputs and outputs are TTL compatible.

The MK48H89 has a Chip Enable power down feature which sustains an automatic standby mode whenever either Chip Enable goes inactive (\bar{E}_1 goes high or E_2 goes low). An Output Enable (\bar{G}) pin provides a high speed tristate control, allowing fast read/write cycles to be achieved with the common-I/O data bus. Operational modes are determined by device control inputs W, \bar{G} , \bar{E}_1 and E_2 , as summarized in the truth table.

PIN CONNECTION



PIN NAMES

A ₀ -A ₁₂	Address Inputs
DQ ₀ -DQ ₈	Data I/O ₀₋₈
\bar{E}_1	Chip Enable 1, Active Low
E_2	Chip Enable 2, Active High
\bar{G}	(OE) Output Enable
W	Write/read Enable
V _{cc} , V _{ss}	+5V, GND

MK48H89 TRUTH TABLE

W	\bar{E}_1	E_2	\bar{G}	MODE	DQ	POWER
X	H	X	X	Deselect	Hi-Z	Standby
X	X	L	X	Deselect	Hi-Z	Standby
H	L	H	H	Read	Hi-Z	Active
H	L	H	L	Read	Q _{OUT}	Active
L	L	H	X	Write	D _{IN}	Active

READ MODE

The MK48H89 is in the Read mode whenever Write Enable (W) is high with Output Enable (G) low, and both Chip Enables (E1 and E2) are active. This provides access to data from nine of 73,728 locations in the static memory array, specified by the 13 address inputs. Valid data will be available at the nine Output pins within t_{AVOQ} after the last stable address, providing G is low, E1 is low, and E2 is high. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{E1LQV} , t_{E2HQV} , or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{E1LQX} , t_{E2HQX} , and t_{GLQX} , but data lines will always be valid at t_{AVQV} .

concurrency of both Chip Enables being active with W low. Therefore, address setup times are referenced to Write Enable and both Chip Enables as t_{AVWL} , t_{AVE1L} and t_{AVE2H} respectively, and is determined to the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of E1, W, or the falling edge of E2.

If the Output is enabled (E1 = low, E2 = high, G = low), then W will return the outputs to high impedance within t_{WLOZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DQVWH} to the rising edge of Write Enable, or to the rising edge of E1 or the falling edge of E2, whichever occurs first, and remain valid t_{WHDX} .

WRITE MODE

The MK48H89 is in the Write mode whenever the W and E1 pins are low, with E2 high. Either Chip Enable pin or W must be inactive during Address transitions. The Write begins with the

MK48H89 BLOCK DIAGRAM

