MOSTEK

4096 x 1-BIT STATIC RAM

Processed to MIL-STD-883, Method 5004, Class B

MKB4104 (P/J/E)-84/85

FEATURES

- Extended operating temperature range ($-55°C \leq T_A \leq 125°C$)
- Combination static storage cells and dynamic control circuitry for truly high performance

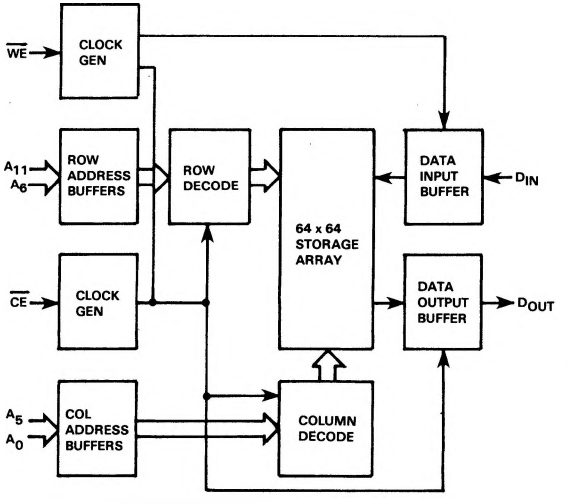
Part Number	Access Time	Cycle Time
4104(J)-84	250ns	385ns
4104(J)-85	300ns	510ns

- Average power dissipation less than 150mW
- Standby power dissipation less than 53mW
- Single +5V power supply (5% tolerance)
- Fully TTL compatible
  Fanout: 2 - Standard TTL
  2 - Schottky TTL
  12 - Low Power Schottky TTL
- Standard 18 pin DIP
- Leadless chip carrier (E package) available for high density applications
- Ruggedized for use in severe military environments

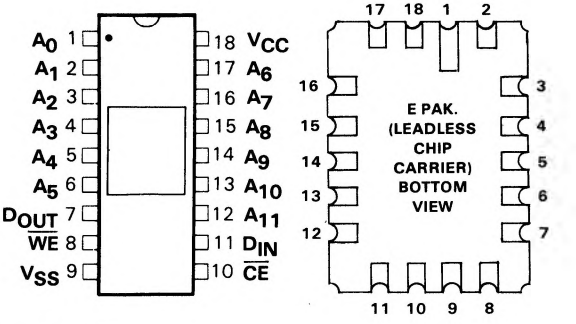
DESCRIPTION

The Mostek MKB4104 is a high performance static random access memory organized as 4096 one bit words. The MKB4104 combines the best characteristics of static and dynamic memory techniques to achieve a TTL compatible, 5 volt only, high performance, low power memory device. It utilizes advanced circuit design concepts and an innovative state-of-the-art N-channel silicon gate process specially tailored to provide static data storage with the performance (speed and power) of dynamic RAMs. Since the storage cell is static the device may be stopped indefinitely with the $\overline{CE}$ clock in the off (Logic 1) state.

FUNCTIONAL DESCRIPTION



PIN CONNECTIONS



PIN NAMES

A0-A11	Address Inputs	V_{SS}	Ground
$\overline{CE}$	Chip Enable	V_{CC}	Power (+5V)
D_{IN}	Data Input	$\overline{WE}$	Write Enable
D_{OUT}	Data Output		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature T_A (Ambient) ..... -55°C to +125°C
Storage Temperature (Ambient)(Ceramic) ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

($-55°C \leq T_A \leq +125°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.4		7.0	V	1
V_{IL}	Logic "0" Voltage All Inputs	-1.0		.65	V	1

DC ELECTRICAL CHARACTERISTICS

($-55°C \leq T_A \leq +125°C$) ($V_{CC}$ = 5.0 volts ± 5%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		27	mA	2
I_{CC2}	Standby V_{CC} Power Supply Current		10	mA	3
I_{IL}	Input Leakage Current (Any Input)	-10	10	μA	4
I_{OL}	Output Leakage Current	-10	10	μA	3,5
V_{OH}	Output Logic "1" Voltage I_{OUT} = -500μA	2.4		V	11
V_{OL}	Output Logic "-" Voltage I_{OUT} = 5mA		0.4	V	11

AC ELECTRICAL CHARACTERISTICS

($-55°C \leq T_A \leq +125°C$) ($V_{CC}$ = +5.0 volts ± 5%)

SYM	PARAMETER	MIN	TYP	MAX	NOTES
C_I	Input Capacitance		4pF	6pF	14
C_O	Output Capacitance		7pF	7pF	14

NOTES:

1. All voltages referenced to V_{SS}.
2. I_{CC1} is related to precharge and cycle times. Guaranteed maximum values for I_{CC1} are at minimum cycle time.
3. Output is disabled (open circuit), $\overline{CE}$ is at logic 1.
4. All device pins at 0 volts except pin under test at $0 \leq V_{IN} \leq 5.5V$ (V_{CC} 5V)
5. $0V \leq V_{OUT} \leq$ 5.5V (V_{CC} 5V)
6. During power up, $\overline{CE}$ and $\overline{WE}$ must be at V_{IH} for minimum of 2ms after V_{CC} reaches 4.75V, before a valid memory cycle can be accomplished.
7. Measured with load circuit equivalent to 2 TTL loads and CL 100pF.
8. If $\overline{WE}$ follows after $\overline{CE}$ by more than t_{WS}, then data out may not remain open circuited.
9. Determined by user. Total cycle time cannot exceed t_{CF} max.
10. Data-in set-up time is referenced to the later of the two falling clock edges $\overline{CE}$ or $\overline{WE}$.
11. AC measurements assume t_I 5ns. Timing points are taken at .8V and 2.0V on inputs and .8V and 2.0V on the output. Transition times are also taken between these levels.
12. t_C t_{CL} + t_P + $2t_I$
13. The true level of the output in the open circuit condition will be determined totally by output load conditions. The output is guaranteed to be open circuit within t_{OFF}.
14. Effective capacitance calculated from the equation $C \frac{1\Delta t}{\Delta V}$ with ΔV equal to 3V and V_{CC} nominal.
15. For RMW, t_{CE} t_{AC} + t_{WPL} + 5_{MOD}
16. t_C t_{AC} + t_{WPL} + t_P + $3t_I$ + t_{MOD}

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS[6,11]
($-55°C \leq T_A \leq +125°C$) ($V_{CC}$ = +5.0 Volts ± 5%)

SYM	PARAMETER	MKB4104-84		MKB4104-85		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_C	Read or Write Cycle Time		410	510		ns	12
t_{AC}	Random Access		250		300	ns	7
t_{CE}	Chip Enable Pulse Width	250	5000	300	5000	ns	15
t_P	Chip Enable Precharge Time	150		200		ns	
t_{AH}	Address Hold Time	135		165		ns	
t_{AS}	Address Set-Up Time	0		0		ns	
t_{OFF}	Output Buffer Turn-Off Delay	0	65	0	75	ns	13
t_{WS}	Write Enable Set-Up Time	0		0		ns	8
t_{DHC}	Data Input Hold Time Referenced to CE	210		250		ns	
t_{DHW}	Data Input Hold Time Referenced to WE	90		105			
t_{WW}	Write Enabled Pulse Width	60		90		ns	
t_{MOD}	Modify Time	0	5000	0	5000	ns	9
t_{WPL}	WE to CE Precharge Lead Time	85		105		ns	10
t_{DS}	Data Input Set-Up Time	0		0		ns	
t_{WH}	Write Enable Hold Time	185		225		ns	
t_T	Transition Time	5	50	5	50	ns	
t_{RMW}	Read-Modify-Write Cycle Time	500		620		ns	16
t_{RS}	Read Set-Up Time	0		0		ns	

DESCRIPTION (Continued)

All input levels, including write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) are TTL with a one level of 2.4 volts and a zero level of .65 volts. The push-pull output (no pull-up resistor required) delivers a one level of 2.4V minimum and a zero level of .4 volts maximum. The output has a fanout of 2 standard TTL loads or 12 low power Schottky loads.

The RAM employs an innovative static cell which occupies a mere 2.75 square mils (½ the area of previous cells) and dissipates power levels comparable to CMOS. The static cell eliminates the need for refresh cycles and associated hardware thus allowing easy system implementation.

Power supply requirement of +5V combined with TTL compatibility on all I/O pins permits easy integration into large memory configurations. The single supply reduces capacitor count and permits denser packaging on printed circuit boards. The 5V only supply requirement and TTL compatible I/O makes this part an ideal choice for next generation +5V only microprocessors such as Mostek's Z80. The early write mode ($\overline{WE}$ active prior to $\overline{CE}$) permits common I/O operation, needed for Z80 interfacing, without external circuitry.

Reliability is greatly enhanced by the low power dissipation which causes a maximum junction rise of only 6.6° at 1.6 Megahertz operation. The MKB4104 was designed for the system designer and user who require the highest performance available along with Mostek's proven reliability.

SUPPLEMENTAL DATA SHEET TO BE USED IN CONJUNCTION WITH MOSTEK MK4104(P/N) DATA SHEET