
ML63512A/63514A

**4-Bit Microcontroller with Built-in Level Detector, Melody Circuit, and Comparator,
Operating at 0.9 V (Min.)**

GENERAL DESCRIPTION

The ML63512A/63514A is a CMOS 4-bit microcontroller with built-in level detector and operates at 0.9 V (min.).

The ML63512A/63514A is an M63512 series mask ROM-version product of OLMS-63K family, which employs Oki's original CPU core nX-4/250.

The program memory capacity and data memory capacity of the ML63512A differ from those of the ML63514A.

48-pin TQFP and 64-pin TQFP packages are available for the ML63512A and ML63514A.

FEATURES

- Extensive instruction set
 - 407 instructions
 - Transfer, rotate, increment/decrement, arithmetic operations, comparison, logic operations, mask operations, bit operations, ROM table reference, stack operations, flag operations, jump, conditional branch, call/return, control.
- Wide variety of addressing modes
 - Indirect addressing of four data memory types, with current bank register, extra bank register, HL register and XY register.
 - Data memory bank internal direct addressing mode.
- Processing speed
 - Two clocks per machine cycle, with most instructions executed in one machine cycle.
 - Minimum instruction execution time : 61 μ s (@ 32.768 kHz system clock)
1 μ s (@ 2 MHz system clock)
- Clock generation circuit
 - Low-speed clock : Crystal oscillation or RC oscillation selectable by mask option (30 to 80 kHz)
 - High-speed clock : Ceramic oscillation or RC oscillation selectable by mask option (2 MHz max.)
- Program memory space
 - ML63512A: 4K words
 - ML63514A: 8K words
 - Basic instruction length is 16 bits/1 word
- Data memory space
 - ML63512A: 128 nibbles
 - ML63514A: 256 nibbles

- Stack level
 - Call stack level : 16 levels
 - Register stack level : 16 levels
- I/O ports
 - Input ports: Selectable as input with pull-up resistor/high-impedance input
 - Output ports: N-channel open drain output (can directly drive LEDs)
 - Input-output ports: Selectable as input with pull-up resistor/high-impedance input
Selectable as N-channel open drain output/CMOS output
 - Can be interfaced with external peripherals that use a different power supply than this device uses. (Power to the output port is supplied from V_{DDI} (separate power supply))
 - Number of ports:
 - (For 48-pin packages)
 - Input port : 1 port × 4 bits
 - Output port : 1 port × 4 bits
 - Input-output port : 6 ports × 4 bits
 - (For 64-pin packages and chips)
 - Input port : 1 port × 4 bits
 - Output port : 1 port × 4 bits
 - Input-output port : 9 ports × 4 bits
- Melody output function
 - Melody sound frequency : 529 to 2979 Hz (@ 32.768 kHz)
 - Tone length : 63 varieties
 - Tempo : 15 varieties
 - Melody data : Stored in the program memory
 - Number of output ports : 1 (dedicated pin)
 - Buzzer driver signal output : 4 kHz (@ 32.768 kHz)
- Level detector
 - Conversion time : Approx. 183 μ s (@ 32.768 kHz)
 - Dedicated input pins : 2 pins (switched by software; for the secondary functions of the input ports)
 - Detection level : 12 levels
- Comparator
 - Offset voltage : 50 mV max. ($V_{DD} = 1.5$ V)
 - Comparison time : Approx. 183 μ s (@ 32.768 kHz)
 - Number of channels : 1 (for the secondary functions of the input ports)
- System reset function
 - System reset through RESETB pin (connected to the internal 32 kHz sampling circuit)
(RESETB pin can be pulled up by mask option)
- Power supply backup
 - Backup circuit (voltage multiplier) enables operation at 0.9 V minimum

- Timers and counter
 - 8-bit timer × 2
 - Selectable as auto-reload mode/capture mode/clock frequency measurement mode
 - 15-bit time base counter × 1
 - 1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz, 128 Hz, 256 Hz, 512 Hz, 1 kHz, and 2 kHz signals can be read (@ 32.768 kHz)

- Serial port
 - Mode : Selectable as UART mode/synchronous mode
 - UART communication speed : 2TBCCLK, TBCCLK, 1/2TBCCLK, Timers 0 & 1 overflow
24 kbps Max. (when 2TBCCLK @ 80 kHz selected)
 - Clock frequency in synchronous mode : 30 to 80 kHz (internal clock mode), external clock frequency
 - Data length : 5 to 8 bits

- Interrupt sources
 - External interrupt (4 sources) : Selectable as rising edge/falling edge/both rising and falling edges
 - Internal interrupt (10 sources) : Time base interrupt × 4 (2, 4, 16, and 32 Hz @ 32.768 kHz)
Timer interrupt × 2
Level detector interrupt × 1
Serial port reception interrupt × 1
Serial port transmission interrupt × 1
Melody end interrupt × 1

- Operating temperature
 - 20 to +70°C

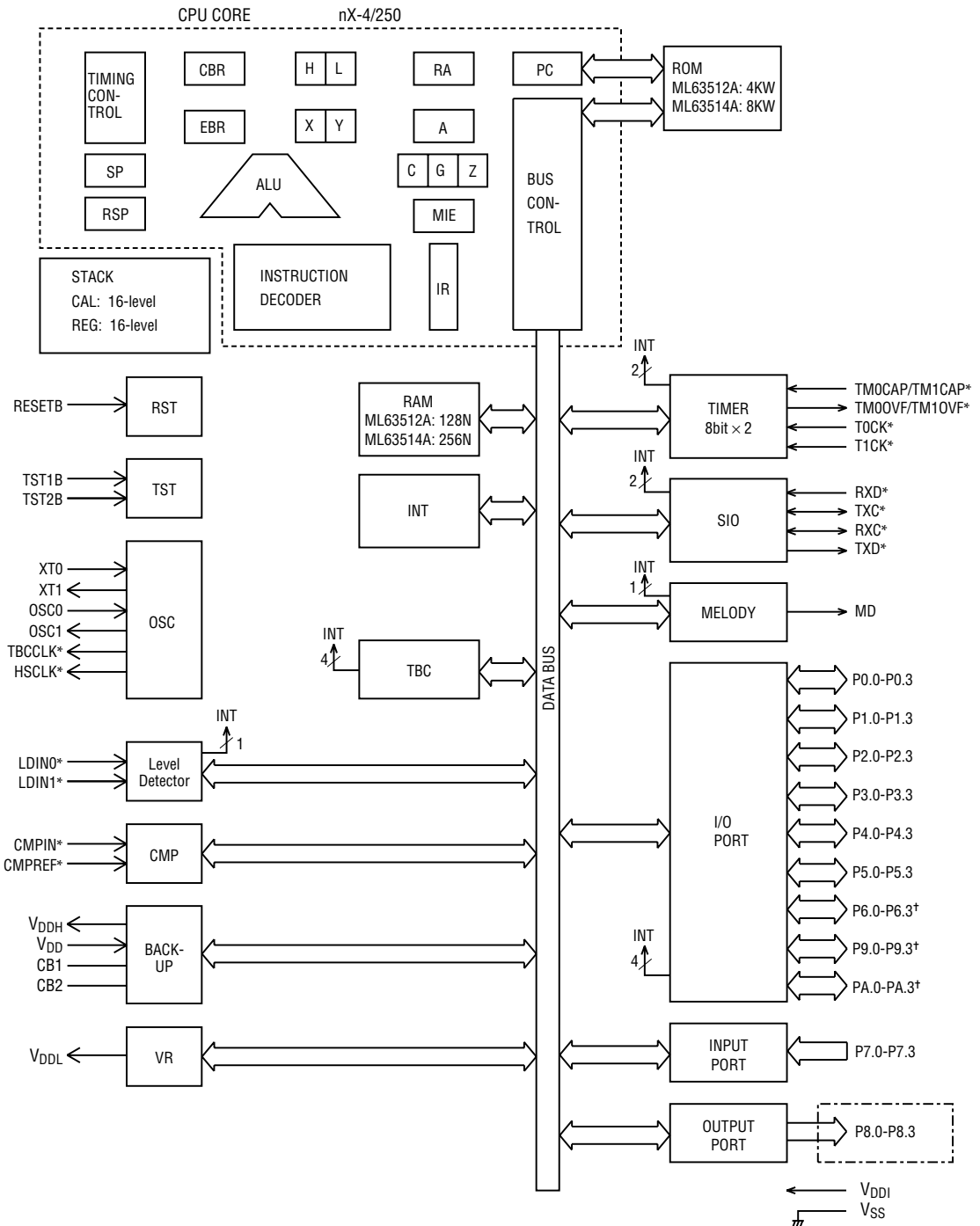
- Supply voltage
 - When backup used : 0.9 to 1.8 V
(Maximum operating frequency 1 MHz)
 - When backup not used : 1.8 to 3.5 V
(Maximum operating frequency 2 MHz; when Level detector or Comparator is used)
1.8 to 5.5 V
(Maximum operating frequency 2 MHz; when Level detector and Comparator are not used)

- Package options:
 - Chip (60 pads) : (Product name: ML63512A-xxxWA, ML63514A-xxxWA)
 - 48-pin plastic TQFP (TQFP48-P-0707-0.50-K) : (Product name: ML63512A-xxxTB, ML63514A-xxxTB)
 - 64-pin plastic TQFP (TQFP64-P-1010-0.50-K) : (Product name: ML63512A-xxxTP, ML63514A-xxxTP)

xxx indicates a code number.

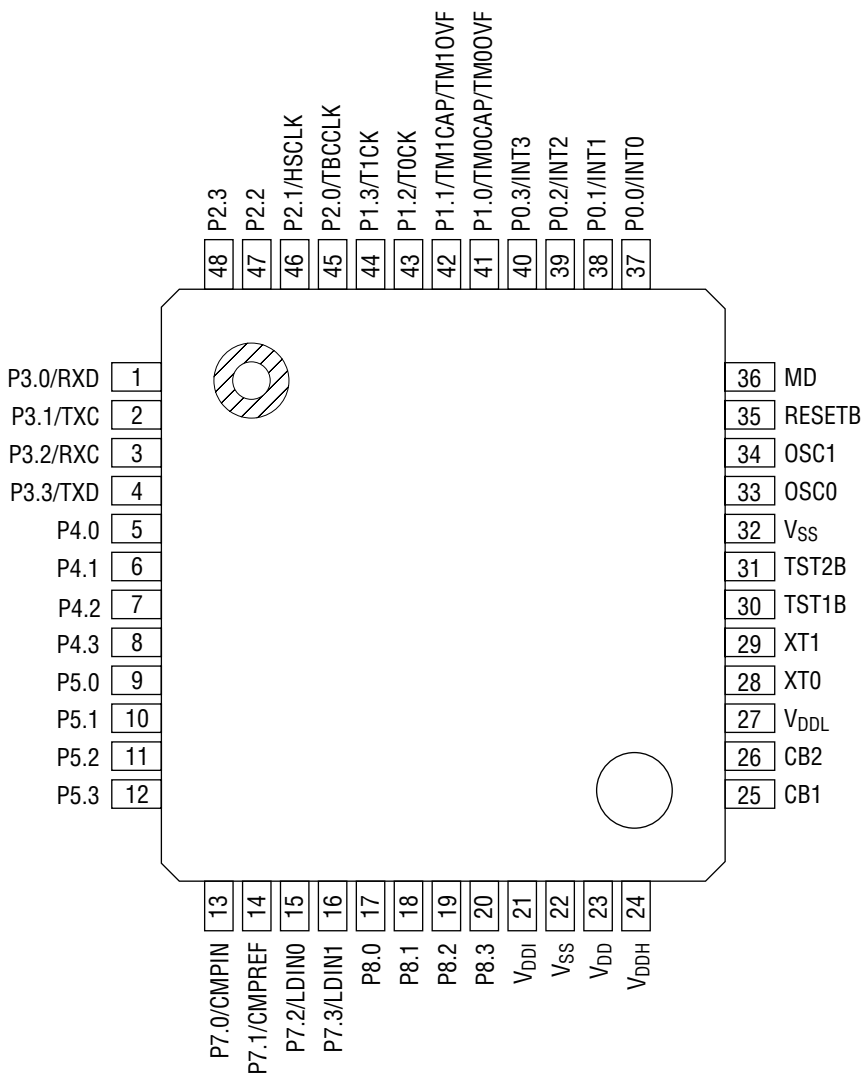
BLOCK DIAGRAM

An asterisk (*) indicates the port secondary function. The power to the circuits corresponding to the signal names inside is supplied from V_{DDI} (power supply for interface).



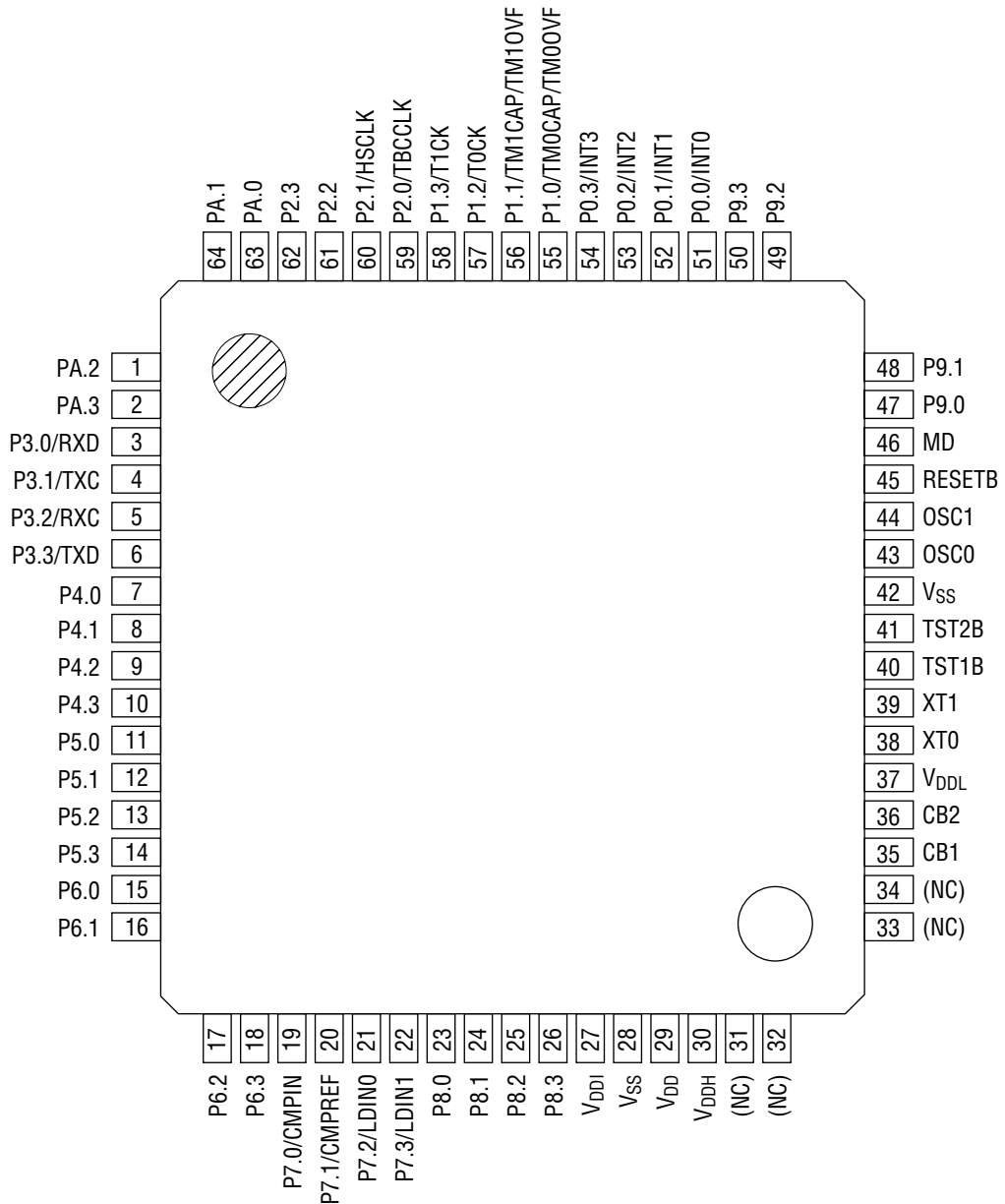
†Port 6 (P6.0 to P6.3), Port 9 (P9.0 to P9.3) and Port A (PA.0 to PA.3) are provided for the 64-pin packages and chips.

PIN CONFIGURATION (TOP VIEW)



48-Pin Plastic TQFP

PIN CONFIGURATION (TOP VIEW) (continued)

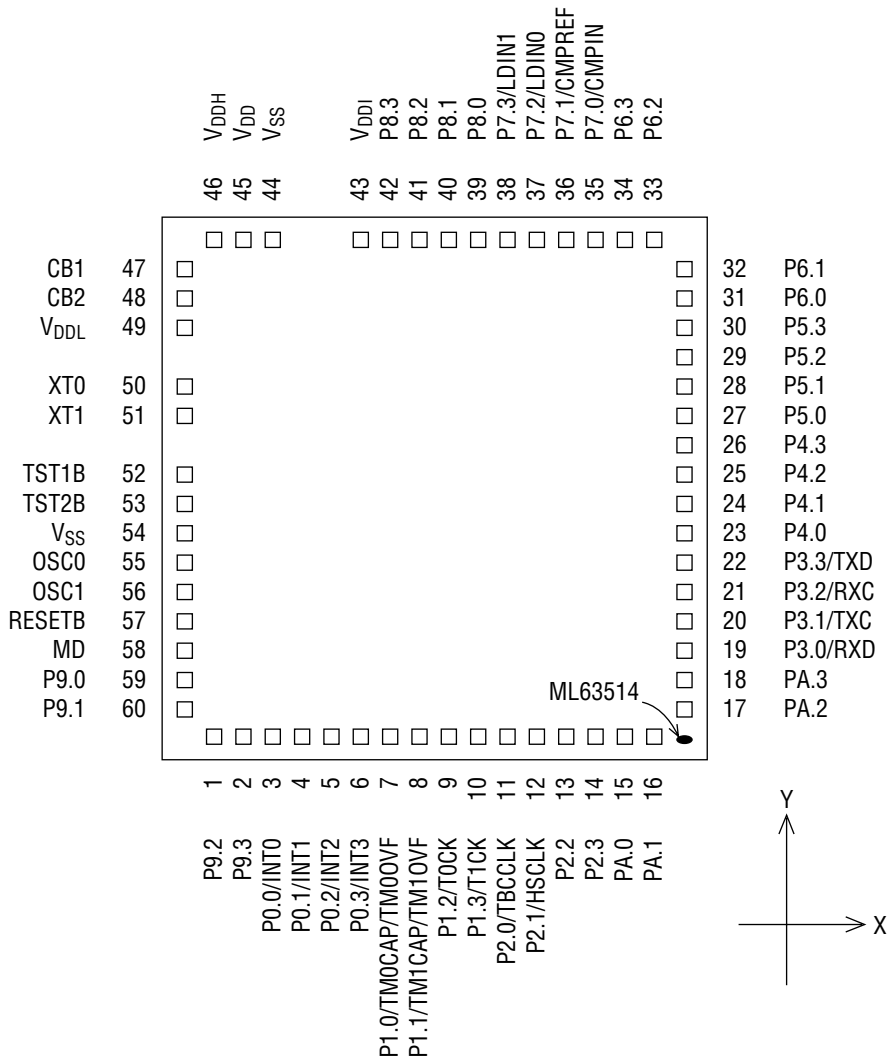


64-Pin Plastic TQFP

Note: Pins marked as (NC) are no-connection pins which are left open.

PAD CONFIGURATION

Pad Layout



Chip Size : 3.51 mm × 3.77 mm
 Chip Thickness : 350 μm (typ.)
 Coordinate Origin : Chip center
 Pad Hole Size : 110 μm × 110 μm
 Pad Size : 120 μm × 120 μm
 Minimum Pad Pitch : 150 μm

Note: The chip substrate voltage is V_{SS}.

Pad Coordinates

Chip center: X = 0, Y = 0

Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)
1	P9.2	-1175	-1717	31	P6.0	1604	1018
2	P9.3	-1018	-1717	32	P6.1	1604	1175
3	P0.0	-862	-1717	33	P6.2	1175	1717
4	P0.1	-705	-1717	34	P6.3	1018	1717
5	P0.2	-548	-1717	35	P7.0	862	1717
6	P0.3	-392	-1717	36	P7.1	705	1717
7	P1.0	-235	-1717	37	P7.2	548	1717
8	P1.1	-78	-1717	38	P7.3	392	1717
9	P1.2	78	-1717	39	P8.0	235	1717
10	P1.3	235	-1717	40	P8.1	78	1717
11	P2.0	392	-1717	41	P8.2	-78	1717
12	P2.1	548	-1717	42	P8.3	-235	1717
13	P2.2	705	-1717	43	V _{DDI}	-392	1717
14	P2.3	862	-1717	44	V _{SS}	-934	1717
15	PA.0	1018	-1717	45	V _{DD}	-1090	1717
16	PA.1	1175	-1717	46	V _{DDH}	-1247	1717
17	PA.2	1604	-1175	47	CB1	-1604	1127
18	PA.3	1604	-1019	48	CB2	-1604	971
19	P3.0	1604	-862	49	V _{DDL}	-1604	814
20	P3.1	1604	-705	50	XT0	-1604	502
21	P3.2	1604	-549	51	XT1	-1604	345
22	P3.3	1604	-392	52	TST1B	-1604	76
23	P4.0	1604	-235	53	TST2B	-1604	-81
24	P4.1	1604	-79	54	V _{SS}	-1640	-236
25	P4.2	1604	78	55	OSC0	-1604	-392
26	P4.3	1604	235	56	OSC1	-1604	-548
27	P5.0	1604	391	57	RESETB	-1604	-705
28	P5.1	1604	548	58	MD	-1604	-862
29	P5.2	1604	705	59	P9.0	-1604	-1018
30	P5.3	1604	861	60	P9.1	-1604	-1175

PIN DESCRIPTIONS

The basic functions of each pin of the ML63512A/63514A are described in Table 1.

A symbol with a slash (/) denotes a pin that has a secondary function.

Refer to Table 2 for secondary functions.

For type, "—" denotes a power supply pin, "I" an input pin, "O" an output pin, and "I/O" an input-output pin.

For pin, "TB" denotes a 48-pin flat package (48TQFP), and "TP" a 64-pin flat package (64TQFP).

Table 1 Pin Descriptions (Basic Functions)

Function	Symbol	Pin No.		Pad No.	Type	Description
		TB	TP			
Power Supply	V _{DD}	23	29	45	—	Positive power supply
	V _{SS}	22, 32	28, 42	44, 54	—	Negative power supply
	V _{DDI}	21	27	43	—	Positive power supply pin for external interface (PORT8 supply)
	V _{DDL}	27	37	49	—	Positive power supply pin for internal logic (internally generated). A capacitor C _I (0.1 μF) should be connected between this pin and V _{SS} .
	V _{DDH}	24	30	46	—	Voltage multiplier pin for power supply backup (internally generated). A capacitor C _H (1.0 μF) should be connected between this pin and V _{SS} .
	CB1	25	35	47	—	Pins to connect a capacitor for voltage multiplier.
	CB2	26	36	48	—	A capacitor (1.0 μF) should be connected between CB1 and CB2.
Oscillation	XT0	28	38	50	I	Low-speed clock oscillation pins. Crystal oscillation or RC oscillation is selected by the mask option.
	XT1	29	39	51	O	If crystal oscillation is selected, connect a crystal between XT0 and XT1, and connect capacitor (C _G) between XT0 and V _{SS} . If RC oscillation is selected, connect external oscillation resistor (R _{CRL}) between XT0 and XT1.
	OSC0	33	43	55	I	High-speed clock oscillation pins. Ceramic oscillation or RC oscillation is selected by the mask option.
	OSC1	34	44	56	O	If ceramic oscillation is selected, connect a ceramic resonator between OSC0 and OSC1, and connect capacitor (C _{LO} , C _{L1}) between OSC0 and V _{SS} , OSC1 and V _{SS} . If RC oscillation is selected, connect external oscillation resistor (R _{CRH}) between OSC0 and OSC1.
Test	TST1B	30	40	52	I	Input pins for testing.
	TST2B	31	41	53	I	A pull-up resistor is internally connected to these pins.

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin No.		Pad No.	Type	Description
		TB	TP			
Reset	RESETB	35	45	57	I	Reset input pin. Setting this pin to "L" level puts this device into a reset state. Then, setting this pin to "H" level starts executing an instruction from address 0000H. An internal or external pull-up resistor is selected by mask option.
Melody	MD	36	46	58	O	Melody output pin (non-inverted output)
Port	P0.0/INT0	37	51	3	I/O	4-bit input-output ports. In input mode, pull-up resistor input or high-impedance input is selectable for each bit. In output mode, N-channel open drain output or CMOS output is selectable for each bit.
	P0.1/INT1	38	52	4		
	P0.2/INT2	39	53	5		
	P0.3/INT3	40	54	6		
	P1.0/ TMOCAP/ TMOOVF	41	55	7	I/O	
	P1.1/ TM1CAP/ TM1OVF	42	56	8		
	P1.2/T0CK	43	57	9		
	P1.3/T1CK	44	58	10		
	P2.0/TBCCLK	45	59	11	I/O	
	P2.1/HSCLK	46	60	12		
	P2.2	47	61	13		
	P2.3	48	62	14		
	P3.0/RXD	1	3	19	I/O	
	P3.1/TXC	2	4	20		
	P3.2/RXC	3	5	21		
	P3.3/TXD	4	6	22		
	P4.0	5	7	23	I/O	
	P4.1	6	8	24		
	P4.2	7	9	25		
	P4.3	8	10	26		
P5.0	9	11	27	I/O		
P5.1	10	12	28			
P5.2	11	13	29			
P5.3	12	14	30			

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin No.		Pad No.	Type	Description
		TB	TP			
Port	P6.0	—	15	31	I/O	4-bit input-output port. In input mode, pull-up resistor input or high-impedance input is selectable for each bit. In output mode, N-channel open drain output or CMOS output is selectable for each bit. Note that these pins are available for a 64-pin package and chip.
	P6.1	—	16	32		
	P6.2	—	17	33		
	P6.3	—	18	34		
	P7.0/CMPIN	13	19	35	I	4-bit input port. Pull-up resistor input or high-impedance input is selectable for each bit.
	P7.1/CMPREF	14	20	36		
	P7.2/LDIN0	15	21	37		
	P7.3/LDIN1	16	22	38		
	P8.0	17	23	39	O	4-bit output port. N-channel open drain output.
	P8.1	18	24	40		
	P8.2	19	25	41		
	P8.3	20	26	42		
	P9.0	—	47	59	I/O	4-bit input-output ports. In input mode, pull-up resistor input or high-impedance input is selectable for each bit. In output mode, N-channel open drain output or CMOS output is selectable for each bit.
	P9.1	—	48	60		
	P9.2	—	49	1		
	P9.3	—	50	2		
PA.0	—	63	15	I/O	Note that these pins are available for a 64-pin package and chip.	
PA.1	—	64	16			
PA.2	—	1	17			
PA.3	—	2	18			

Table 2 shows the secondary functions of each pin of the ML63512A/63514A.

Table 2 Pin Descriptions (Secondary Functions)

Function	Symbol	Pin No.		Pad No.	Type	Description
		TB	TP			
External Interrupt	P0.0/INT0	37	51	3	I	External 0 interrupt input pin. Edge detection can be selected from one of a rising edge, a falling edge, or both rising and falling edges.
	P0.1/INT1	38	52	4	I	External 1 interrupt input pin. Edge detection can be selected from one of a rising edge, a falling edge, or both rising and falling edges.
	P0.2/INT2	39	53	5	I	External 2 interrupt input pin. Edge detection can be selected from one of a rising edge, a falling edge, or both rising and falling edges.
	P0.3/INT3	40	54	6	I	External 3 interrupt input pin. Edge detection can be selected from one of a rising edge, a falling edge, or both rising and falling edges.
Capture	P1.0/TMOCAP	41	55	7	I	Timer 0 (TM0) capture trigger input pin.
	P1.1/TM1CAP	42	56	8	I	Timer 1 (TM1) capture trigger input pin.
Timer	P1.0/TM0OVF	41	55	7	O	Timer 0 (TM0) overflow flag output pin.
	P1.1/TM1OVF	42	56	8	O	Timer 1 (TM1) overflow flag output pin.
	P1.2/T0CK	43	57	9	I	Timer 0 (TM0) external clock input pin.
	P1.3/T1CK	44	58	10	I	Timer 1 (TM1) external clock input pin.
Oscillation Output	P2.0/TBCCLK	45	59	11	O	Low-speed oscillation clock output pin.
	P2.1/HSCLK	46	60	12	O	High-speed oscillation clock output pin.
Serial Port	P3.0/RXD	1	3	19	I	Serial port receive data input pin.
	P3.1/TXC	2	4	20	I/O	Sync serial port clock input-output pin. Transmit sync clock input-output pin when a serial port is used synchronously. Transmit clock output when this device is used as a master processor. Transmit clock input when this device is used as a slave processor.
	P3.2/RXC	3	5	21	I/O	Sync serial port clock input-output pin. Receive sync clock input-output pin when a serial port is used synchronously. Receive clock output when this device is used as a master processor. Receive clock input when this device is used as a slave processor.
	P3.3/TXD	4	6	22	O	Serial port transmit data output pin.
Comparator	P7.0/CMPIN	13	19	35	I	Comparator analog input pin.
	P7.1/COMPREF	14	20	36	I	Comparator reference voltage input pin.
Level	P7.2/LDINO	15	21	37	I	Level detector analog input pin.
Detector	P7.3/LDIN1	16	22	38	I	Level detector analog input pin.

ABSOLUTE MAXIMUM RATINGS(V_{SS} = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage 1	V _{DD}	Ta = 25°C	-0.3 to +5.8	V
Power Supply Voltage 2	V _{DDI}	Ta = 25°C	-0.3 to +5.8	V
Power Supply Voltage 3	V _{DDH}	Ta = 25°C	-0.3 to +5.8	V
Power Supply Voltage 4	V _{DDL}	Ta = 25°C	-0.3 to +5.8	V
Input Voltage 1	V _{IN1}	V _{DD} Input, Ta = 25°C	-0.3 to V _{DD} + 0.3	V
Input Voltage 2	V _{IN2}	V _{DDI} Input, Ta = 25°C	-0.3 to V _{DDI} + 0.3	V
Output Voltage 1	V _{OUT1}	V _{DD} Output, Ta = 25°C	-0.3 to V _{DD} + 0.3	V
Output Voltage 2	V _{OUT2}	V _{DDI} Output, Ta = 25°C	-0.3 to V _{DDI} + 0.3	V
Output Voltage 3	V _{OUT3}	V _{DDH} Output, Ta = 25°C	-0.3 to V _{DDH} + 0.3	V
Storage Temperature	T _{STG}	—	-55 to +150	°C
Power Dissipation	P _D	Ta = 25°C	15	mW

RECOMMENDED OPERATING CONDITIONS

- When backup is used

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T _{op}	—	-20 to +70	°C
Operating Voltage	V _{DD}	—	0.9 to 1.8	V
	V _{DDI}	—	0.9 to 3.5	V
Crystal Oscillation Frequency	f _{XT}	—	30 to 80	kHz
Low-Speed RC Oscillator Frequency	f _{CRL}	R _{CRL} = 1.5 MΩ	32 ±30%	kHz
External High-Speed RC Oscillator Resistance	R _{CRH}	V _{DD} = 0.9 to 1.8 V	100 to 300	kΩ

- When backup is not used

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T _{op}	—	-20 to +70	°C
Operating Voltage	V _{DD}	—	1.8 to 3.5	V
		When Level detector and Comparator are not used	1.8 to 5.5	
	V _{DDI}	—	1.8 to 5.5	
Crystal Oscillation Frequency	f _{XT}	—	30 to 80	kHz
Low-Speed RC Oscillator Frequency	f _{CRL}	R _{CRL} = 1.5 MΩ	32 ±30%	kHz
External High-Speed RC Oscillator Resistance	R _{CRH}	V _{DD} = 1.8 to 5.5 V	15 to 300	kΩ
Ceramic Oscillation Frequency	f _{CM}	V _{DD} = 2.2 to 5.5 V	300k to 1M	Hz
		V _{DD} = 2.7 to 5.5 V	200k to 2M	

ELECTRICAL CHARACTERISTICS

DC Characteristics

- When backup is used

($V_{DD} = V_{DD1} = 1.5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }+70^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit	
Supply Current 1	I_{DD1}	CPU is in HALT state	$T_a = 25^\circ\text{C}$	4.8	5.3	5.8	μA	1
		High-speed oscillation stop	$T_a = -20\text{ to }+50^\circ\text{C}$	—	5.3	9.0		
		Level detector stop	$T_a = -20\text{ to }+70^\circ\text{C}$	—	5.3	15.0		
Supply Current 2	I_{DD2}	CPU operating	$T_a = 25^\circ\text{C}$	12	13	14	μA	
		High-speed oscillation stop	$T_a = -20\text{ to }+50^\circ\text{C}$	—	13	16		
		Level detector stop	$T_a = -20\text{ to }+70^\circ\text{C}$	—	13	24		
Supply Current 3	I_{DD3}	CPU operating at low speed High-speed oscillation stop Level detector active (for a soft duty of about 3%)	—	10	35	μA		
Supply Current 4	I_{DD4}	CPU operating at high speed High-speed RC oscillation $R_{CRH} = 100\text{ k}\Omega$	—	550	750	μA		

- When backup is not used

($V_{DD} = V_{DD1} = 3.0\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }+70^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit	
Supply Current 1	I_{DD1}	CPU is in HALT state	$T_a = 25^\circ\text{C}$	2.1	2.4	2.7	μA	1
		High-speed oscillation stop	$T_a = -20\text{ to }+50^\circ\text{C}$	—	2.4	7.0		
		Level detector stop	$T_a = -20\text{ to }+70^\circ\text{C}$	—	2.4	10.0		
Supply Current 2	I_{DD2}	CPU operating	$T_a = 25^\circ\text{C}$	5	6	7	μA	
		High-speed oscillation stop	$T_a = -20\text{ to }+50^\circ\text{C}$	—	6	9		
		Level detector stop	$T_a = -20\text{ to }+70^\circ\text{C}$	—	6	15		
Supply Current 3	I_{DD3}	CPU operating at low speed High-speed oscillation stop Level detector active (for a soft duty of about 3%)	—	6	25	μA		
Supply Current 4	I_{DD4}	CPU operating at high speed High-speed RC oscillation $R_{CRH} = 100\text{ k}\Omega$	—	410	550	μA		
Supply Current 5	I_{DD5}	CPU operating at high speed High-speed ceramic oscillation (ceramic oscillation, 2 MHz)	—	850	1000	μA		

DC Characteristics (continued)

(V_{DD} = V_{DDI} = 1.5 V, V_{SS} = 0 V, Ta = -20 to +70°C unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V _{DDH} Voltage	V _{DDH}	High-speed clock stop V _{DD} = 1.5 V	2.8	—	3.0	V	1
		High-speed clock oscillation (RC oscillation, R _{CRH} = 100 kΩ)	2	—	—	V	
V _{DDL} Voltage	V _{DDL}	High-speed clock stop	1.0	1.5	2.0	V	
		High-speed clock oscillation	2.0	—	2.7	V	
Crystal Oscillation Start Voltage	V _{STA}	Oscillation start time: within 5 seconds	1.2	—	—	V	
Crystal Oscillation Hold Voltage	V _{HOLD}	—	0.9	—	—	V	
External Crystal Oscillator Capacitance	C _G	—	5	—	25	pF	
Internal Crystal Oscillator Capacitance	C _D	—	20	25	30	pF	
Internal Low-Speed RC Oscillator Capacitance	C _{XT}	—	10	15	20	pF	
Internal High-Speed RC Oscillator Capacitance	C _{OS}	—	8	12	16	pF	
Input Pin Capacitance (P0.0 to P0.3) (P1.0 to P1.3) ⋮ (P7.0 to P7.3) (P9.0 to P9.3) (PA.0 to PA.3)	C _{IN}	—	—	—	5	pF	

DC Characteristics (continued)

(V_{DD} = V_{DDI} = 1.5 V, V_{SS} = 0 V, T_a = -20 to +70°C unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit	
Output Current 1 (P0.0 to P0.3) (P1.0 to P1.3) ⋮ (P6.0 to P6.3) (P9.0 to P9.3) (PA.0 to PA.3) (MD)	I _{OH1}	V _{OH1} = V _{DD} - 0.5 V	V _{DD} = 1.5 V	-2.5	-1.3	-0.2	mA	2
			V _{DD} = 3.0 V	-6.0	-3.5	-1.0	mA	
			V _{DD} = 5.0 V	-8.5	-5.0	-1.5	mA	
	I _{OL1}	V _{OL1} = 0.5 V	V _{DD} = 1.5 V	0.2	1.3	2.5	mA	
			V _{DD} = 3.0 V	1	3	6	mA	
			V _{DD} = 5.0 V	1.5	3.7	8.5	mA	
Output Current 2 (P8.0 to P8.3)	I _{OH2Z}	V _{OH2} = V _{DD}	—	—	1	μA		
	I _{OL2}	V _{OL2} = 0.5 V	V _{DDI} = 1.5 V	3.0	7.5	14.0	mA	
			V _{DDI} = 3.0 V	6	12	20	mA	
V _{DDI} = 5.0 V			8	15	28	mA		
Output Current 3 (OSC1)	I _{OH3R}	V _{OH3R} = V _{DDH} - 0.5 V	V _{DD} = V _{DDH} = 3.0 V	-2.5	-1.5	-0.2	mA	
			V _{DD} = V _{DDH} = 5.0 V	-3.5	-1.8	-0.5	mA	
	I _{OL3R}	V _{OL3R} = 0.5 V	V _{DD} = V _{DDH} = 3.0 V	0.2	1.5	2.5	mA	
			V _{DD} = V _{DDH} = 5.0 V	0.5	1.8	3.5	mA	
	I _{OH3C}	V _{OH3C} = V _{DDH} - 0.5 V	V _{DD} = V _{DDH} = 3.0 V	-300	-160	-60	μA	
			V _{DD} = V _{DDH} = 5.0 V	-400	-240	-100	μA	
	I _{OL3C}	V _{OL3C} = 0.5 V	V _{DD} = V _{DDH} = 3.0 V	60	170	300	μA	
			V _{DD} = V _{DDH} = 5.0 V	100	210	400	μA	
Output Leakage (P0.0 to P0.3) (P1.0 to P1.3) ⋮ (P6.0 to P6.3) (P8.0 to P8.3) (P9.0 to P9.3) (PA.0 to PA.3)	I _{OOH}	V _{OH} = V _{DD}	—	—	1	μA		
	I _{OOL}	V _{OL} = V _{SS}	-1	—	—	μA		

DC Characteristics (continued)

(V_{DD} = V_{DDI} = 1.5 V, V_{SS} = 0 V, T_a = -20 to +70°C unless otherwise specified)

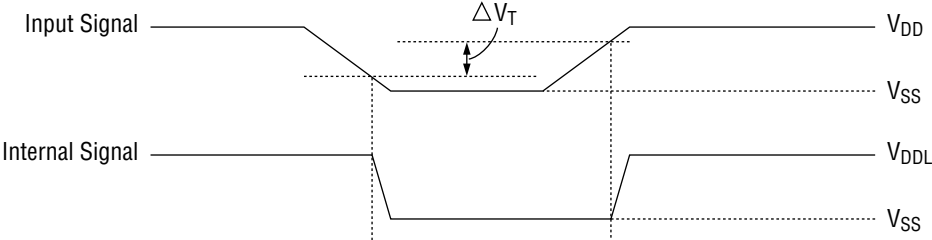
Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit	
Input Current 1 (P0.0 to P0.3) (P1.0 to P1.3) ⋮ (P7.0 to P7.3) (P9.0 to P9.3) (PA.0 to PA.3)	I _{IH1U}	V _{IH1} = V _{DD} (when pulled up)	—	—	1	μA	3	
	I _{IL1U}	V _{IL1} = V _{SS} (when pulled up)	V _{DD} = 1.5 V	-8	-4	-1		μA
			V _{DD} = 3.0 V	-60	-30	-10		μA
			V _{DD} = 5.0 V	-150	-90	-23		μA
	I _{IH1Z}	V _{IH1} = V _{DD} (in a high-impedance state)	—	—	1	μA		
I _{IL1Z}	V _{IL1} = V _{SS} (in a high-impedance state)	-1	—	—	μA			
Input Current 2 (RESETB)	I _{IH2}	V _{IH2} = V _{DD}	—	—	1	μA		
	I _{IL2}	V _{IL2} = V _{SS} (when pulled up)	V _{DD} = 1.5 V	-45	-20	-2		μA
			V _{DD} = 3.0 V	-260	-120	-30		μA
V _{DD} = 5.0 V			-870	-300	-70	μA		
Input Current 3 (OSC0)	I _{IL3}	V _{IL3} = V _{SS} (when pulled up)	V _{DD} = V _{DDH} = 3.0 V	-350	-170	-30	μA	
			V _{DD} = V _{DDH} = 5.0 V	-750	-450	-200	μA	
	I _{IH3R}	V _{IH3} = V _{DDH}	—	—	1	μA		
I _{IL3R}	V _{IL3} = V _{SS}	-1	—	—	μA			
Input Current 4 (TST1B, TST2B)	I _{IH4}	V _{IH4} = V _{DD}	—	—	0.1	μA		
	I _{IL4}	V _{IL4} = V _{SS} (when pulled up)	V _{DD} = 1.5 V	-120	-60	-10	μA	
			V _{DD} = 3.0 V	-600	-350	-100	μA	
V _{DD} = 5.0 V			-1320	-770	-220	μA		

DC Characteristics (continued)

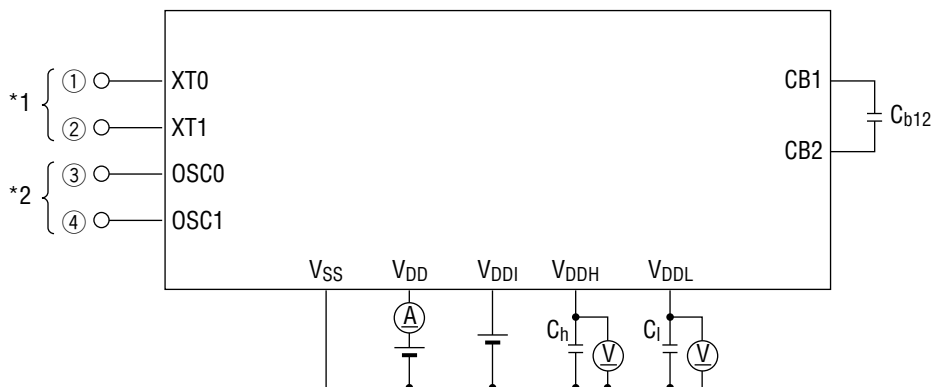
(V_{DD} = V_{DDI} = 1.5 V, V_{SS} = 0 V, T_a = -20 to +70°C unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Voltage 1 (P0.0 to P0.3) (P1.0 to P1.3) ⋮ (P7.0 to P7.3) (P9.0 to P9.3) (PA.0 to PA.3)	V _{IH1}	V _{DD} = 1.5 V	1.2	—	1.5	V	4
		V _{DD} = 3.0 V	2.4	—	3.0	V	
		V _{DD} = 5.0 V	4	—	5	V	
	V _{IL1}	V _{DD} = 1.5 V	0	—	0.3	V	
		V _{DD} = 3.0 V	0	—	0.6	V	
		V _{DD} = 5.0 V	0	—	1	V	
Input Voltage 2 (OSC0)	V _{IH2}	V _{DD} = V _{DDH} = 3.0 V	2.4	—	3.0	V	
		V _{DD} = V _{DDH} = 5.0 V	4	—	5	V	
	V _{IL2}	V _{DD} = V _{DDH} = 3.0 V	0	—	0.6	V	
		V _{DD} = V _{DDH} = 5.0 V	0	—	1	V	
Input Voltage 3 (RESETB) (TST1B, TST2B)	V _{IH3}	V _{DD} = 1.5 V	1.35	—	1.50	V	
		V _{DD} = 3.0 V	2.4	—	3.0	V	
		V _{DD} = 5.0 V	4	—	5	V	
	V _{IL3}	V _{DD} = 1.5 V	0	—	0.15	V	
		V _{DD} = 3.0 V	0	—	0.6	V	
		V _{DD} = 5.0 V	0	—	1	V	
Hysteresis Width (P0.0 to P0.3) (P1.0 to P1.3) ⋮ (P7.0 to P7.3) (P9.0 to P9.3) (PA.0 to PA.3) (RESETB) (TST1B, TST2B)	ΔV _T	V _{DD} = 1.5 V	0.05	0.10	0.30	V	
		V _{DD} = 3.0 V	0.2	0.5	1.0	V	
		V _{DD} = 5.0 V	0.25	1.00	1.50	V	

Hysteresis width

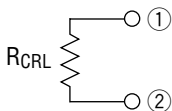


Measuring circuit 1

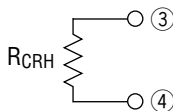


- C_G : 15 pF
- C_{b12}, C_h : 1 μ F
- C_l : 0.1 μ F
- Ceramic Resonator : CSA2.00MG (2 MHz)
 CSB1000J (1 MHz)
 (Murata MFG.-make)
- C_{L0} : 30 pF
- C_{L1} : 30 pF

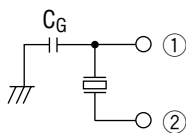
*1 RC oscillator



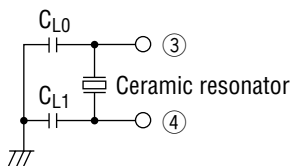
*2 RC oscillator



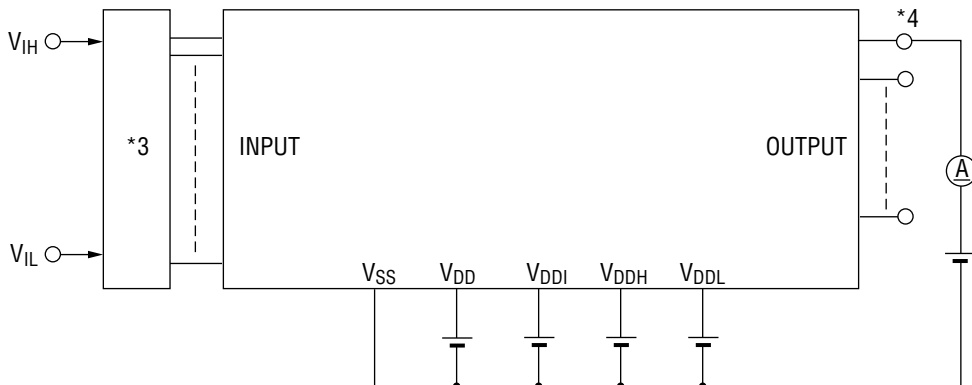
Crystal oscillator



Ceramic oscillator



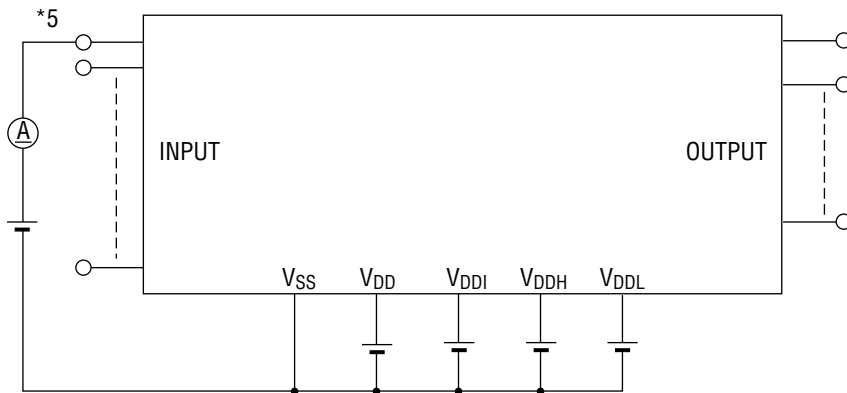
Measuring circuit 2



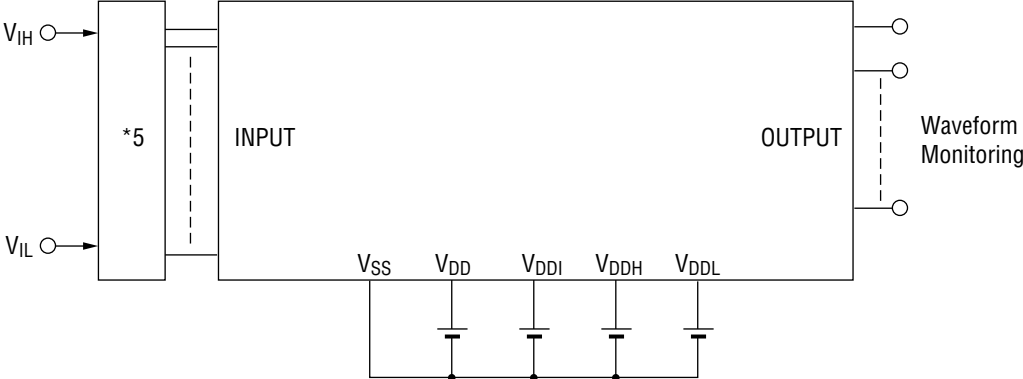
*3 Input logic circuit to determine the specified measuring conditions.

*4 Measured at the specified output pins.

Measuring circuit 3



Measuring circuit 4



*5 Measured at the specified input pins.

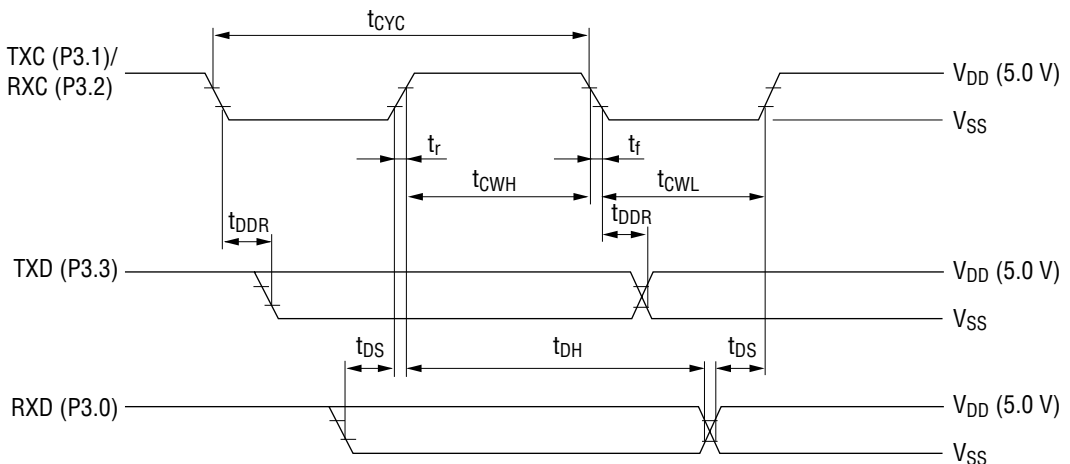
AC Characteristics (Serial Interface, Serial Port)

($V_{DD} = 0.9$ to 5.5 V, $V_{DDH} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, $V_{DDI} = 0.9$ to 5.5 V, $T_a = -20$ to $+70^\circ\text{C}$ unless otherwise specified)

(1) Synchronous Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
TXC/RXC Input Fall Time	t_f	—	—	—	1	μs
TXC/RXC Input Rise Time	t_r	—	—	—	1	μs
TXC/RXC Input "L" Level Pulse Width	t_{CWL}	—	0.8	—	—	μs
TXC/RXC Input "H" Level Pulse Width	t_{CWH}	—	0.8	—	—	μs
TXC/RXC Input Cycle Time	t_{CYC}	—	2	—	—	μs
TXC/RXC Output Cycle Time	$t_{CYC(O)}$	CPU operating at 32.768 kHz	—	30.5	—	μs
TXD Output Delay Time	t_{DDR}	Output load capacitance 10 pF	—	—	0.4	μs
RXD Input Setup Time	t_{DS}	—	0.5	—	—	μs
RXD Input Hold Time	t_{DH}	—	0.8	—	—	μs

Synchronous communication timing
("H" level = 4.0 V, "L" level = 1.0 V)



(2) UART Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit Baud Rate	T_{BRT}	$T_{BRT} = 1/f_{BRT}$ $T_{CR} = 1/f_{OSC}$	$T_{BRT} - T_{CR}$	T_{BRT}	$T_{BRT} + T_{CR}$	s
Receive Baud Rate	R_{BRT}	$R_{BRT} = 1/f_{BRT}$	$R_{BRT} \times 0.97$	R_{BRT}	$R_{BRT} \times 1.03$	s

f_{BRT} : Baud rates (2TBCCLK, TBCCLK, 1/2TBCCLK, Timer 0/1 overflow)

UART communication timing

("H" level = 4.0 V, "L" level = 1.0 V)

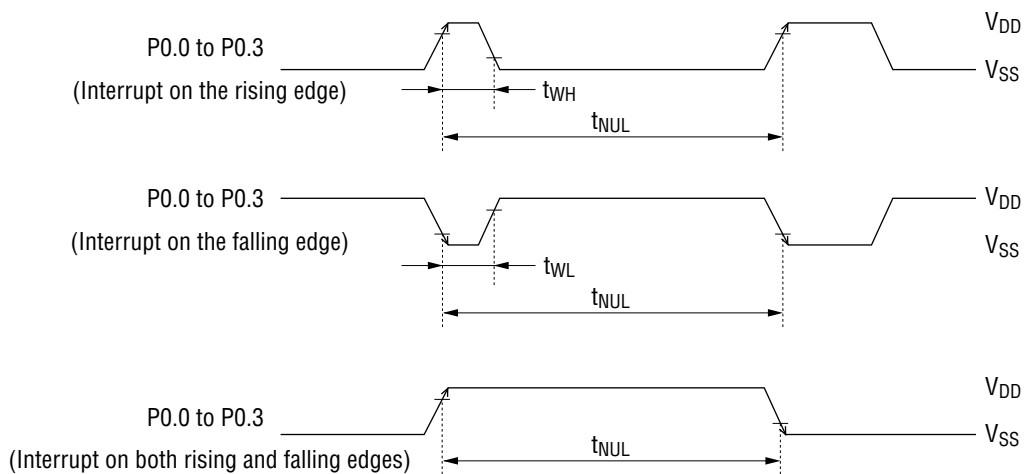


AC Characteristics

($V_{DD} = V_{DDI} = 0.9$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to $+70^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
External Interrupt Enable Pulse Width (Rising Edge)	t_{WH}	—	20	—	—	ns
External Interrupt Enable Pulse Width (Falling Edge)	t_{WL}	—	20	—	—	ns
External Interrupt Disable Time	t_{NUL}	Interrupt enable, MIE = 1 CPU operating under the NOP instruction System clock: 32.768 kHz	13.0	—	65.1	μs

AC characteristics timing



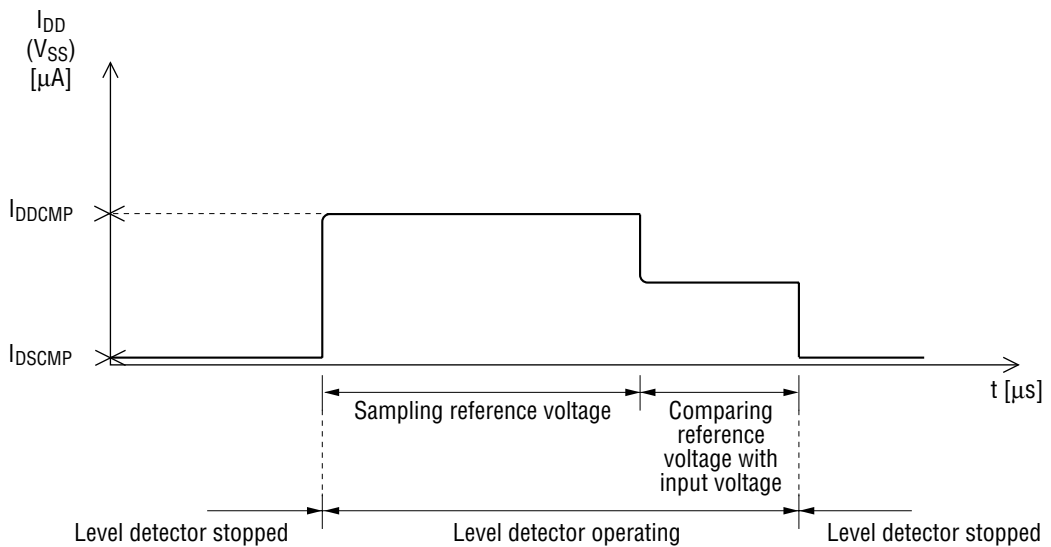
Comparator Electrical Characteristics

($V_{DD} = 0.9\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }+70^\circ\text{C}$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Comparator Offset Voltage	V_{coff}	—	—	—	30	mV	CMPIN CMPREF
Comparator Input Voltage	V_{cin}	—	V_{SS}	—	V_{DD}	V	
Comparator Conversion Time	T_C	System clock: 32.768 kHz	—	183	—	μs	
Comparator Supply Current	I_{DDCMP}	Comparator operating	—	30	90	μA	
	I_{DSCMP}	Comparator stopped	—	—	0.1	μA	

Conceptual diagram of comparator supply current

The conceptual diagram of the comparator supply current I_{DDCMP} and I_{DSCMP} is shown below.



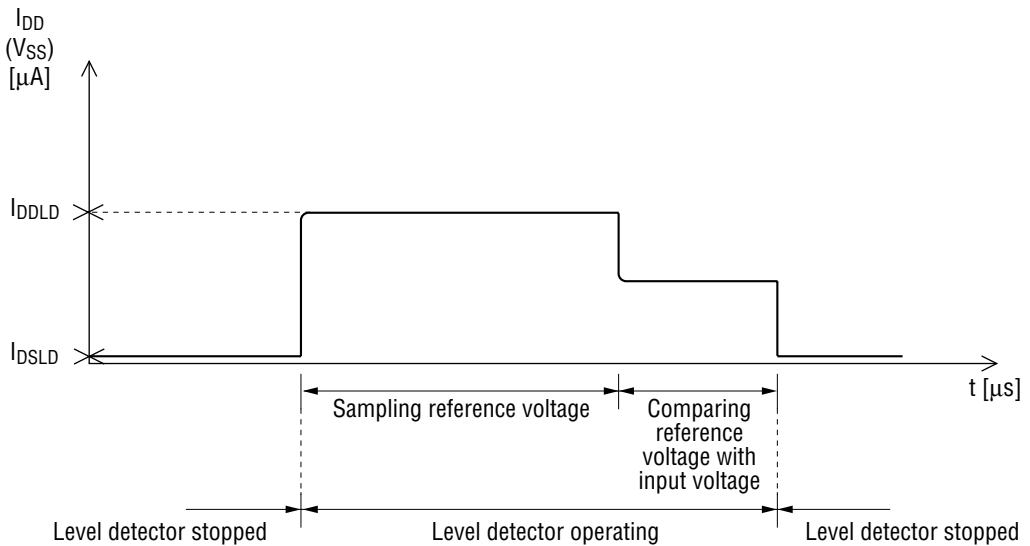
Level Detector Electrical Characteristics

($V_{DD} = 0.9\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }+70^\circ\text{C}$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Level Detector Input Voltage	V_{LD}	—	V_{SS}	—	V_{DD}	V	LDINO, 1
Level Detector Conversion Time	T_C	System clock: 32.768 kHz	—	183	—	μs	
Level Detector Supply Current	$I_{DDL D}$	Level detector operating	—	80	130	μA	
	$I_{DSL D}$	Level detector stopped	—	—	0.1	μA	

Conceptual diagram of level detector supply current

The conceptual diagram of the level detector supply current $I_{DDL D}$ and $I_{DSL D}$ is shown below.



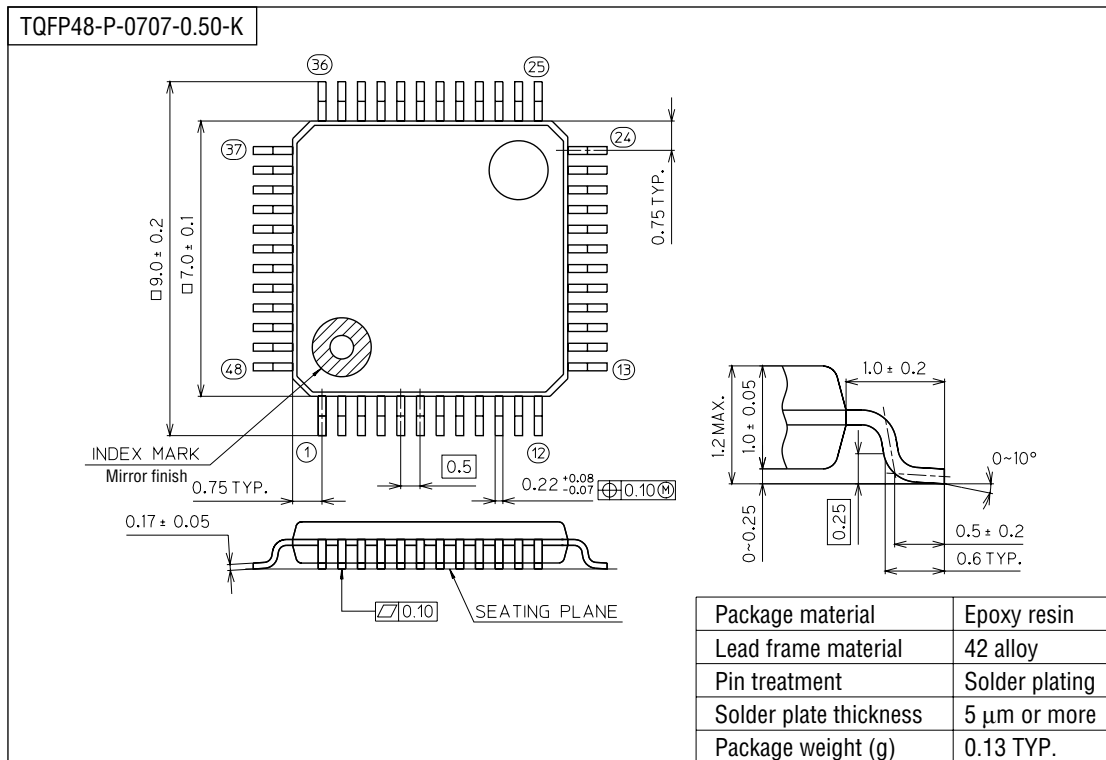
Level Detector Input Levels and Output Codes

($V_{DD} = 0.9$ to 1.8 V: when backup is used, $V_{DD} = 1.8$ to 3.5 V: when backup is not used;
 $V_{SS} = 0$ V, $T_a = -20$ to $+70^\circ\text{C}$)

Input Level [V]		Level Detector Operation State	LDOUT			
Min.	Max.		bit 3	bit 2	bit 1	bit 0
$1440/1500 \times V_{DD}$	V_{DD}	OFF state	1	1	1	1
$1306/1500 \times V_{DD}$	$1366/1500 \times V_{DD}$	ON state	1	0	1	1
$1190/1500 \times V_{DD}$	$1250/1500 \times V_{DD}$		1	0	1	0
$1074/1500 \times V_{DD}$	$1134/1500 \times V_{DD}$		1	0	0	1
$958/1500 \times V_{DD}$	$1018/1500 \times V_{DD}$		1	0	0	0
$842/1500 \times V_{DD}$	$902/1500 \times V_{DD}$		0	1	1	1
$726/1500 \times V_{DD}$	$786/1500 \times V_{DD}$		0	1	1	0
$610/1500 \times V_{DD}$	$670/1500 \times V_{DD}$		0	1	0	1
$494/1500 \times V_{DD}$	$554/1500 \times V_{DD}$		0	1	0	0
$378/1500 \times V_{DD}$	$438/1500 \times V_{DD}$		0	0	1	1
$262/1500 \times V_{DD}$	$322/1500 \times V_{DD}$		0	0	1	0
$146/1500 \times V_{DD}$	$206/1500 \times V_{DD}$		0	0	0	1
V_{SS}	$88/1500 \times V_{DD}$		0	0	0	0

PACKAGE DIMENSIONS

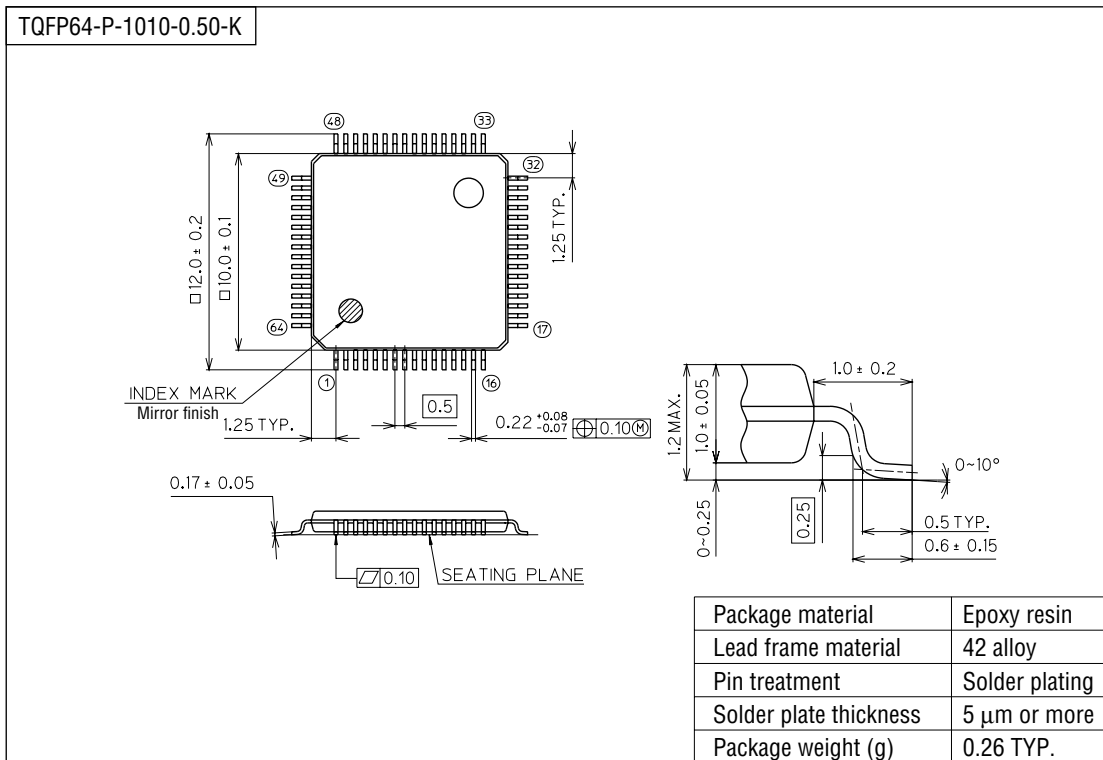
(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)



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