National Semiconductor

MM54C195/MM74C195 4-bit Registers

General Description

The MM54C195/MM74C195 CMOS 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input and a direct overriding clear. The following two modes of operation are possible:

Parallel Load
Shift in direction Q_A towards Q_D

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control of input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited.

Serial shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs allow the first stage to perform as a J-K, D, or T-type flip flop as shown in the truth table.

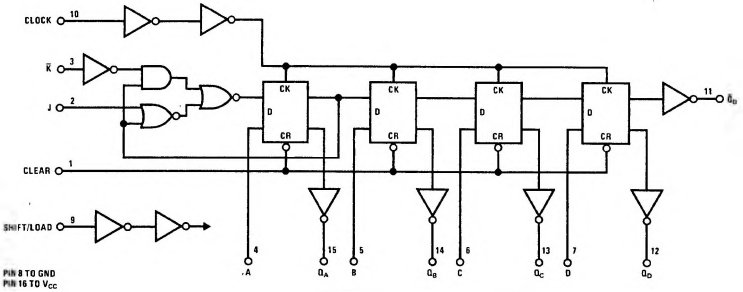
Features

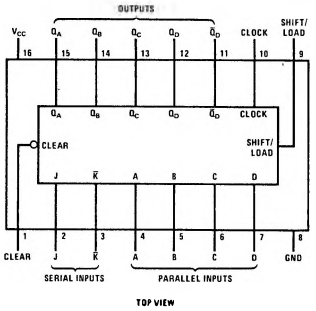
- Medium speed operation — 8.5 MHz (typ.) with 10 V supply and 50 pF load
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power — 100 nW (typ.)
- Tenth power TTL compatible — drive 2 LPTTL loads
- Supply voltage range — 3 V to 15 V
- Synchronous parallel load
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and K inputs to first stage
- Complementary outputs from last stage
- Positive-edge triggered clocking
- Diode clamped inputs to protect against static charge

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Remote metering
- Industrial electronics
- Computers

Schematic and Connection Diagrams





TOP VIEW

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC}+0.3\,V$
Operating Temperature Range	
MM54C195	$-55°C$ to $+125°C$
MM74C195	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation	500 mW
Operating V_{CC} Range	3.0 V to 15 V
Absolute Maximum V_{CC}	18 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics Max./min. limits apply across temperature range, unless otherwise noted.

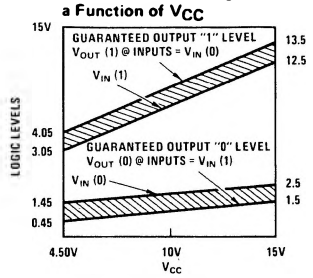
	Parameter	Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0\,V$, $V_{CC}=10\,V$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15\,V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15\,V$		0.05	300	μA
	CMOS/LPTTL Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$	$V_{CC}-1.5$ $V_{CC}-1.5$		 V	V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=-360\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=-360\,\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=360\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=360\,\mu A$			0.4 0.4	V V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE}	Output Source Current	$V_{CC}=5.0\,V$, $V_{IN(0)}=0\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	−1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC}=10\,V$, $V_{IN(0)}=0\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	−8.0			mA
I_{SINK}	Output Sink Current	$V_{CC}=5.0\,V$, $V_{IN(1)}=5.0\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC}=10\,V$, $V_{IN(1)}=10\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	8.0			mA

Truth Table

INPUTS AT t_n		OUTPUTS AT t_{n+1}				
J	$\overline{K}$	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	L	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

Note: H = HIGH LEVEL, L = LOW LEVEL
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse
Q_{An} = State of Q_A at t_n

Guaranteed noise Margin as a Function of V_{CC}



AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or Q	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		150 75	300 130	ns ns
t_{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clear to Q or Q	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		150 50	300 130	ns ns
t_S	Time Prior to Clock Pulse that Data must be Present	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		80 35	200 70	ns ns
t_S	Time Prior to Clock Pulse that Shift/Load must be Present	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		110 60	150 90	ns ns
t_H	Time After Clock Pulse that Data must be Held	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		−10 −5.0	0 0	ns ns
t_W	Minimum Clear Pulse Width ($t_{WL} = t_{WH}$)	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		100 50	200 100	ns ns
t_W	Minimum Clear Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		90 40	130 60	ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	5.0 2.0			μs μs
f_{MAX}	Maximum Input Clock Frequency	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	2.0 5.5	3.0 8.5		MHz MHz
C_{IN}	Input Capacitance	(Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

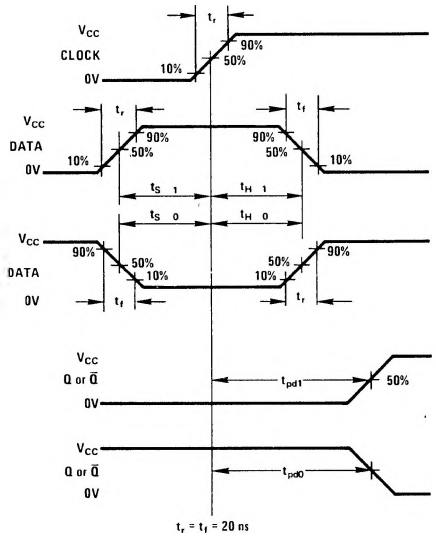
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Switching Time Waveforms

CMOS to CMOS



TTL to CMOS