

# MM54C240/MM74C240 Inverting MM54C244/MM74C244 Non-Inverting Octal Buffers and Line Drivers with TRI-STATE® Outputs

## General Description

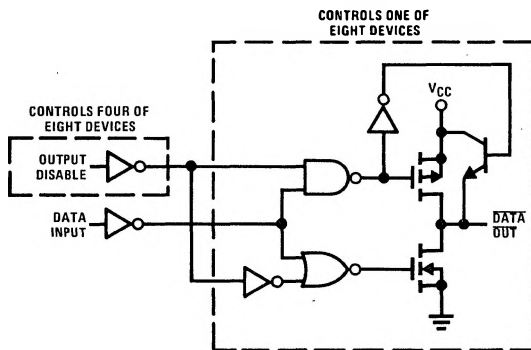
These octal buffers and line drivers are monolithic complementary MOS (CMOS) integrated circuits with TRI-STATE® outputs. These outputs have been specially designed to drive highly capacitive loads such as bus-oriented systems. These devices have a fan-out of 6 low power Schottky loads. A high logic level on the output disable control input G makes the outputs go into the high impedance state. For improved TTL input compatibility see MM74C941.

## Features

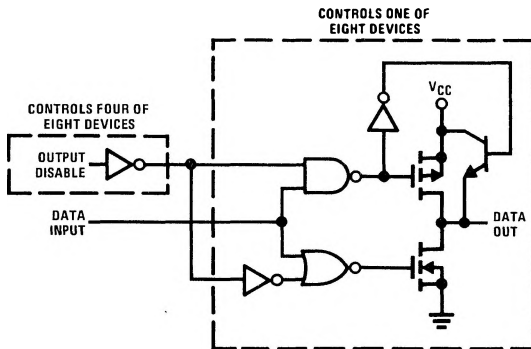
- Wide supply voltage range (3V to 15V)
- High noise immunity (0.45  $V_{CC}$  typ)
- Low power consumption
- High capacitive load drive capability
- TRI-STATE outputs
- Input protection
- TTL compatibility
- 20-pin dual-in-line package
- High speed 25 ns (typ.) @ 10V, 50 pF (MM74C244)

## Logic and Connection Diagrams

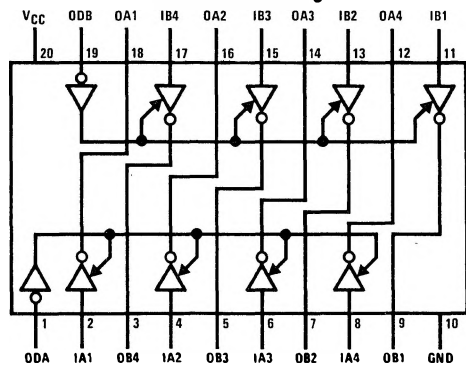
MM54C240/MM74C240



MM54C244/MM74C244

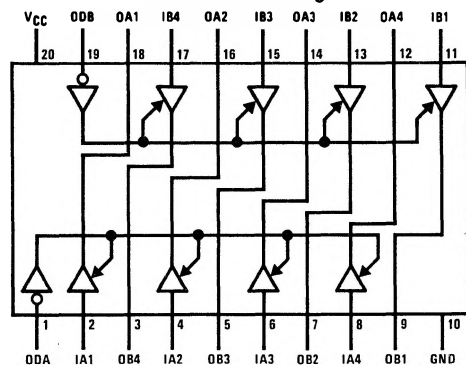


MM54C240/MM74C240  
Dual-In-Line Package



TOP VIEW

MM54C244/MM74C244  
Dual-In-Line Package



TOP VIEW

**Absolute Maximum Ratings** (Note 1)

Voltage at Any Pin	-0.3V to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C240, MM54C244	-55 °C to +125 °C
MM74C240, MM74C244	-40 °C to +85 °C
Storage Temperature Range	-65 °C to +150 °C
Package Dissipation	500 mW
Operating $V_{CC}$ Range	3V to 15V
Absolute Maximum $V_{CC}$	18V
Lead Temperature (Soldering, 10 seconds)	300 °C

**DC Electrical Characteristics**

Min/max limits apply across temperature range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
<b>CMOS TO CMOS</b>					
Logical "1" Input Voltage ( $V_{IN(1)}$ )	$V_{CC} = 5.0V$ $V_{CC} = 10V$	3.5 8.0			V V
Logical "0" Input Voltage ( $V_{IN(0)}$ )	$V_{CC} = 5.0V$ $V_{CC} = 10V$			1.5 2.0	V V
Logical "1" Output Voltage ( $V_{OUT(1)}$ )	$V_{CC} = 5.0V, I_O = -10 \mu A$ $V_{CC} = 10V, I_O = -10 \mu A$	4.5 9.0			V V
Logical "0" Output Voltage ( $V_{OUT(0)}$ )	$V_{CC} = 5.0V, I_O = 10 \mu A$ $V_{CC} = 10V, I_O = 10 \mu A$			0.5 1.0	V V
Logical "1" Input Current ( $I_{IN(1)}$ )	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	$\mu A$
Logical "0" Input Current ( $I_{IN(0)}$ )	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		$\mu A$
Supply Current ( $I_{CC}$ )	$V_{CC} = 15V$		0.05	300	$\mu A$
<b>CMOS/LPTTL INTERFACE</b>					
Logical "1" Input Voltage ( $V_{IN(1)}$ )	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
Logical "0" Input Voltage ( $V_{IN(0)}$ )	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$			0.8 0.8	V V
Logical "1" Output Voltage ( $V_{OUT(1)}$ )	54C, $V_{CC} = 4.5V, I_O = -450 \mu A$ 74C, $V_{CC} = 4.75V, I_O = -450 \mu A$	$V_{CC} - 0.4$ $V_{CC} - 0.4$			V V
	54C, $V_{CC} = 4.5V, I_O = -2.2 mA$ 74C, $V_{CC} = 4.75V, I_O = -2.2 mA$	2.4 2.4			V V
Logical "0" Output Voltage ( $V_{OUT(0)}$ )	54C, $V_{CC} = 4.5V, I_O = 2.2 mA$ 74C, $V_{CC} = 4.75V, I_O = 2.2 mA$			0.4 0.4	V V
<b>OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)</b>					
Output Source Current ( $I_{SOURCE}$ ) (P-Channel)	$V_{CC} = 5.0V, V_{OUT} = 0V$ $T_A = 25^\circ C$	-14.0	-30.0		mA
	$V_{CC} = 10V, V_{OUT} = 0V$ $T_A = 25^\circ C$	-36.0	-70.0		mA
Output Sink Current ( $I_{SINK}$ ) (N-Channel)	$V_{CC} = 5.0V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$	12.0	20.0		mA
	$V_{CC} = 10V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$	48.0	70.0		mA

**AC Electrical Characteristics**  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$ , unless otherwise specified.

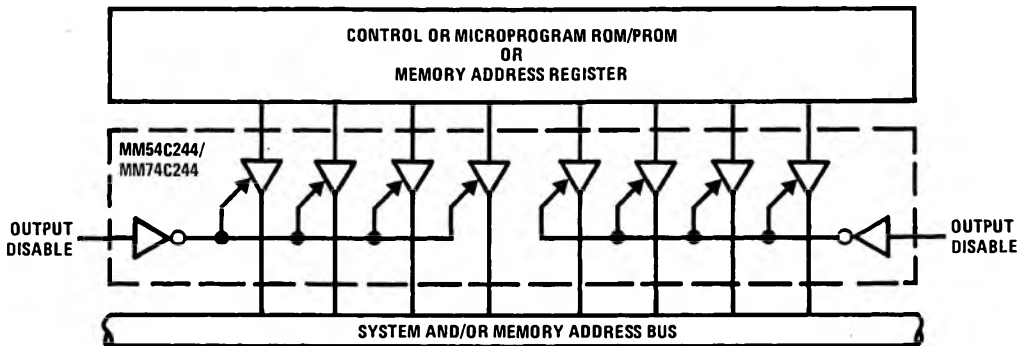
Parameter	Conditions	Min	Typ	Max	Units	
$t_{Pd(1)}$ , $t_{Pd(0)}$ Propagation Delay (Data In to Out) MM54C240/MM74C240	$V_{CC} = 5\text{V}$ , $C_L = 50\text{ pF}$		60	90	ns	
	$V_{CC} = 10\text{V}$ , $C_L = 50\text{ pF}$		40	70	ns	
	$V_{CC} = 5\text{V}$ , $C_L = 150\text{ pF}$		80	110	ns	
	$V_{CC} = 10\text{V}$ , $C_L = 150\text{ pF}$		60	90	ns	
	MM54C244/MM74C244	$V_{CC} = 5\text{V}$ , $C_L = 50\text{ pF}$		45	70	ns
		$V_{CC} = 10\text{V}$ , $C_L = 50\text{ pF}$		25	50	ns
		$V_{CC} = 5\text{V}$ , $C_L = 150\text{ pF}$		60	90	ns
		$V_{CC} = 10\text{V}$ , $C_L = 150\text{ pF}$		40	70	ns
$t_{1H}$ , $t_{0H}$	Propagation Delay Output Disable to High Impedance State (from a Logic Level)	$R_L = 1\text{k}$ , $C_L = 50\text{ pF}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$	45 35	80 60	ns ns	
	$t_H$ , $t_{\bar{H}}$	Propagation Delay Output Disable to Logic Level (from High Impedance State)	$R_L = 1\text{k}$ , $C_L = 50\text{ pF}$ $V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$	50 30	90 60	ns ns
$t_{T(HL)}$ , $t_{T(LH)}$		Transition Time	$V_{CC} = 5\text{V}$ , $C_L = 50\text{ pF}$	45	80	ns
	$V_{CC} = 10\text{V}$ , $C_L = 50\text{ pF}$		30	60	ns	
	$V_{CC} = 5\text{V}$ , $C_L = 150\text{ pF}$		75	140	ns	
	$V_{CC} = 10\text{V}$ , $C_L = 150\text{ pF}$		50	100	ns	
$C_{PD}$	Power Dissipation Capacitance (Output Enabled Per Buffer) MM54C240/MM74C240 MM54C244/MM74C244	(See Note 3)	100		$\mu\text{F}$	
			100		$\mu\text{F}$	
			10		$\mu\text{F}$	
			0		$\mu\text{F}$	
$C_{IN}$	Input Capacitance (Any Input)	$V_{IN} = 0\text{V}$ , $f = 1\text{MHz}$ , $T_A = 25^\circ\text{C}$	10		$\mu\text{F}$	
			10		$\mu\text{F}$	
$C_O$	Output Capacitance (Output Disabled)	$V_{IN} = 0\text{V}$ , $f = 1\text{MHz}$ , $T_A = 25^\circ\text{C}$	10		$\mu\text{F}$	

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** Capacitance is guaranteed by periodic testing.

**Note 3:**  $C_{PD}$  determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

**Typical Application**



Truth Tables

MM54C240/MM74C240

ODA	IA	OA
1	X	Z
1	X	Z
0	0	1
0	1	0

ODB	IB	OB
1	X	Z
1	X	Z
0	0	1
0	1	0

MM54C244/MM74C244

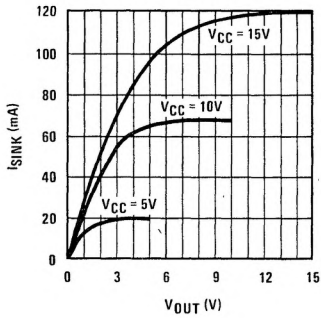
ODA	IA	OA
1	X	Z
1	X	Z
0	0	0
0	1	1

ODB	IB	OB
1	X	Z
1	X	Z
0	0	0
0	1	1

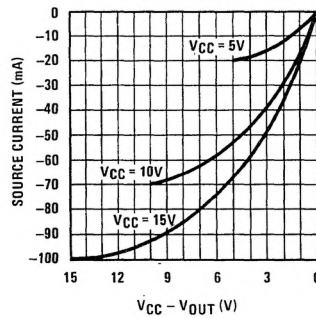
1 = High  
 0 = Low  
 X = Don't Care  
 Z = TRI-STATE

Typical Performance Characteristics

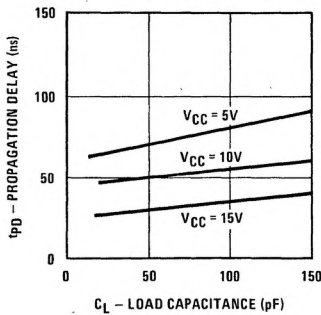
N-Channel Output Drive  
 @ 25°C



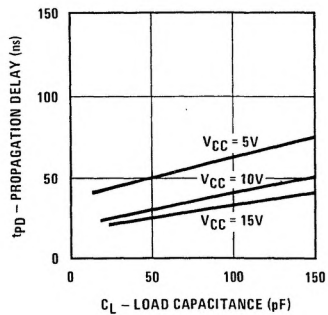
P-Channel Output Drive  
 @ 25°C



MM54C240/MM74C240  
 Propagation Delay Vs.  
 Load Capacitance

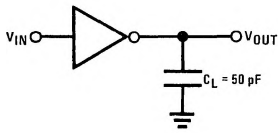


MM54C244/MM74C244  
 Propagation Delay Vs.  
 Load Capacitance

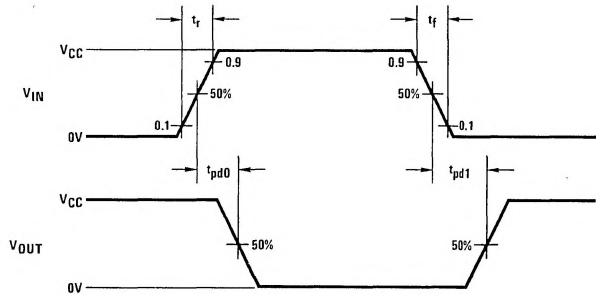


# AC Test Circuits and Switching Time Waveforms

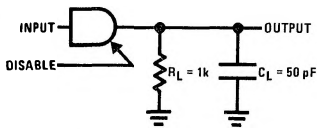
$t_{pd0}, t_{pd1}$



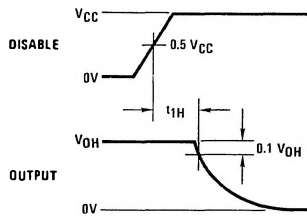
CMOS to CMOS



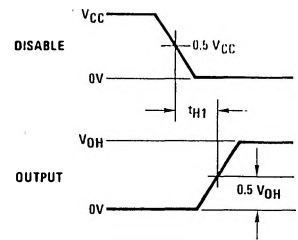
$t_{1H}$  and  $t_{H1}$



$t_{1H}$

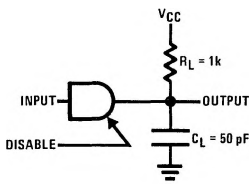


$t_{H1}$

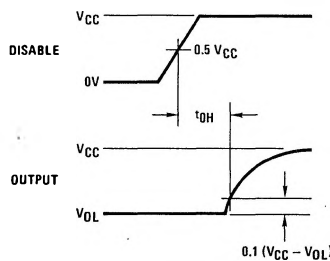


Note:  $V_{OH}$  is defined as the DC output high voltage when the device is loaded with a 1 k $\Omega$  resistor to ground.

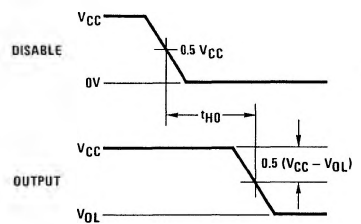
$t_{0H}$  and  $t_{H0}$



$t_{0H}$



$t_{H0}$



Note:  $V_{OL}$  is defined as the DC output low voltage when the device is loaded with a 1 k $\Omega$  resistor to  $V_{CC}$ .

Note: Delays measured with input  $t_r, t_f \leq 20$  ns