MP8251-I

DESCRIPTION

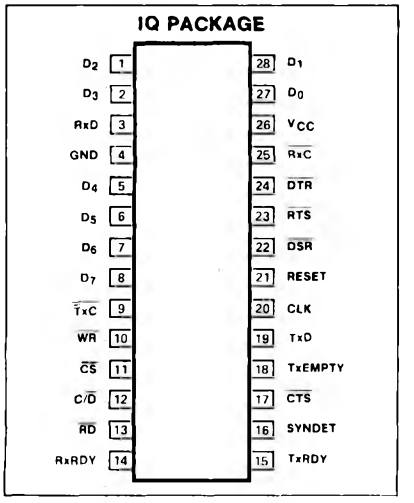
The MP8251 is a programmable Universal Synchronous/Asynchronous Receiver/Transmitter (USART) chip contained in a standard 28-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, functions as a serial data input/output interface in the MP8080A microcomputer family. The functional configuration of the MP8251 is programmed by the system software for maximum flexibility, thereby allowing the system to receive and transmit virtually any serial data communication signal presently in use (including IBM Bisync).

The MP8251 can be programmed to receive and transmit either synchronous or asynchronous serial data. The MP8251 performs serial-to-parallel conversion on data characters received from an input/output device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the MP8251 at any time during the functional operation. Status information reported includes the type and the condition of the transfer operations being performed by the MP8251, as well as any transmission error conditions (parity, overrun, or framing).

FEATURES

- **Synchronous and asynchronous full duplex operations**
- **Synchronous Mode Capabilities**
  - **Selectable 5- to 8-Bit characters**
  - **Internal or external character synchronization**
  - **Automatic sync insertion**
- **Asynchronous mode capabilities**
  - **Selectable 5- to 8-Bit characters**
  - **3 selectable clock rates (1x, 16x or 64x the baud rate)**
  - **Line break detection and generation**
  - **1-, 11/2-, or 2-Stop bit detection and generation**
  - **False start bit detection**
- **Baud rates**
  - **DC to 56k baud (synchronous mode)**
  - **DC to 9.6k baud (asynchronous mode)**
- **Transmission error detection capabilities**
  - **Parity**
  - **Overrun**
  - **Framing**

PIN CONFIGURATION



- **Double buffering of data**
- **TTL compatible**
- **Single TTL clock**
- **Reduces system component count**

PIN DESIGNATION

MNEMONIC	TYPE	NAME AND FUNCTION
$\overline{CS}$	I	**Chip select:** When low (logic 0), the chip is selected. This enables communication between the MP8251 and the MP8080A microprocessor.
$\overline{RD}$	I	**Read:** When low, allows the MP8080A to read data or status information from the MP8251.
$\overline{WR}$	I	**Write:** When low, allows the MP8080A to write data or control words into the MP8251.
C/$\overline{D}$	I	**Control/data:** Used in conjunction with an active RD or WR input (logic 0) to determine overall device operation as indicated below.
RESET	I	**Reset:** When high (logic 1), places the MP8251 in the idle mode. The device remains in this mode until a new set of control words is written into the MP8251 to program its functional definition. Minimum Reset pulse width is 6 t_{CY}.
CLK	I	**Clock:** TTL clock that is used to generate internal timing signals for the MP8251. The minimum frequency of the CLK input is 30 times the receiver/transmitter clock frequency for the synchronous mode, and 4.5 times the receiver/transmitter clock frequency for the asynchronous mode. The CLK input is normally connected to the ϕ_2 (TTL) output of the 8224 Clock Generator and Driver device.
$\overline{DSR}$	I	**Data set ready:** General purpose input whose condition can be tested by the MP8080A using a status read operation. However, a low level DSR input is normally used to test data set ready conditions.
$\overline{CTS}$	I	**Clear to send:** If low when the TxEn bit (D_0) of the command Instruction Control Word (see figure) is set high, enables the MP8251 to transmit serial data.

$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	OPERATION
0	0	0	1	Data character read from MP8251
0	0	1	0	Data character written into MP8251
0	1	0	1	Status information read from MP8251
0	1	1	0	Control word written into MP8251
1	x	x	x	Device not selected

PIN DESIGNATION (Cont'd)

MNEMONIC	TYPE	NAME AND FUNCTION
$\overline{TxC}$	I	**Transmitter Clock:** This clock input controls the rate at which a data character is to be transmitted. The frequency of the TxC input is equal to the baud rate for the synchronous mode, and is a multiple (1x, 16x or 64x) of the baud rate for the asynchronous mode. A portion of the Mode Instruction Word (see figure) selects the value of the baud rate factor when in the asynchronous mode. Transmitter data are clocked out of the MP8251 on the falling edge of the TxC input.
RxD	I	**Receiver data:** Serial data input from a MODEM or an input/output device.
$\overline{RxC}$	I	**Receiver clock:** This clock input controls the rate at which a data character is to be received. The frequency and selection of the RxC input is as described above for the TxC input. Receiver data are clocked into the MP8251 on the rising edge of the RxC input.
V_{CC}		+5V power supply.
GND		**Ground:** 0-V reference.
$\overline{DTR}$	O	**Data terminal ready** General purpose output which can be set to an active low by programming the DTR bit (D_1) of the Command Instruction Control Word. However, a low level DTR output is normally used for data terminal ready or rate select control.
$\overline{RTS}$	O	**Request to send:** General purpose output which can be set to an active low by programming the RTS bit (D_5) of the Command Instruction Control Word. However, the RTS output is normally used for request to send control in the transmit mode.
TxD	O	**Transmitter data:** Composite serial data output to a MODEM or input/output device. The TxD output is held in the marking state (logic 1) upon a Reset operation.
TxRDY	O	**Transmitter ready:** When high, alerts the MP8080A that the transmitter is ready to accept a data character. The TxRDY output, which is automatically reset whenever a character is written into the MP8251, can be used as an interrupt to the system. For polled operation, the condition of the TxRDY signal can be tested by the MP8080A using a status read operation.
TxE	O	**Transmitter empty:** Goes high to indicate the end of a transmit mode. The TxE output is automatically reset whenever a character is written into the MP8251. In the synchronous mode, a high-level TxE output indicates that a character has not been loaded, the transmitter buffer is empty, and the sync character(s) of a data block are soon to be transmitted automatically as fillers.
RxRDY	O	**Receiver ready:** When high, alert the MP8080A that the receiver contains a data character that is ready to be input to the CPU. The RxRDY output, which is automatically reset whenever a character is read from the MP8251, can be used as an interrupt to the system. For polled operation, the condition of the RxRDY signal can be tested by the MP8080A using a status read operation.
D_7-D_0	I/O	**Data bus:** This bus comprises eight Tri-state input/output lines. The bus provides bidirectional communications between the MP8251 and the MP8080A. Data are routed to or from the internal data bus buffer upon execution of an MP8080A OUT or IN instruction, respectively. In addition, control words, command words and status information are transferred through the data bus buffer.
SYNDET	I/O	**Sync detect:** This pin may be used in the synchronous mode only. System software can program SYNDET as either an input or an output. When used as an output (Internal sync detect mode), a high level SYNDET output is automatically reset upon a status read operation by the MP8080A. When used as an input (external sync detect mode) a high level SYNDET causes the MP8251 to start assembling data characters on the falling edge of the next RxC input.

ABSOLUTE MAXIMUM RATINGS*

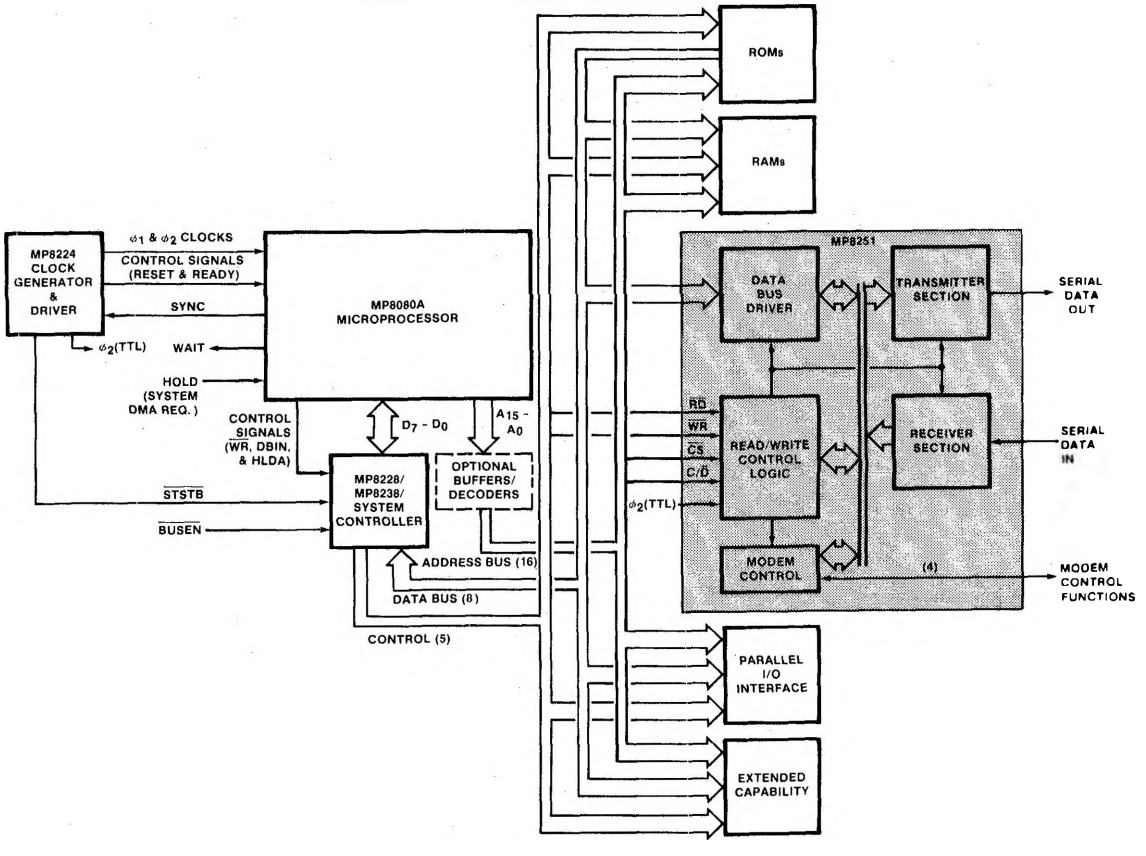
	PARAMETER	RATING	UNIT
T_A	Ambient temperature under bias	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C
	Voltage on any pin with respect to ground	-0.5 to +7	V
P_D	Power dissipation	1	W

*NOTE

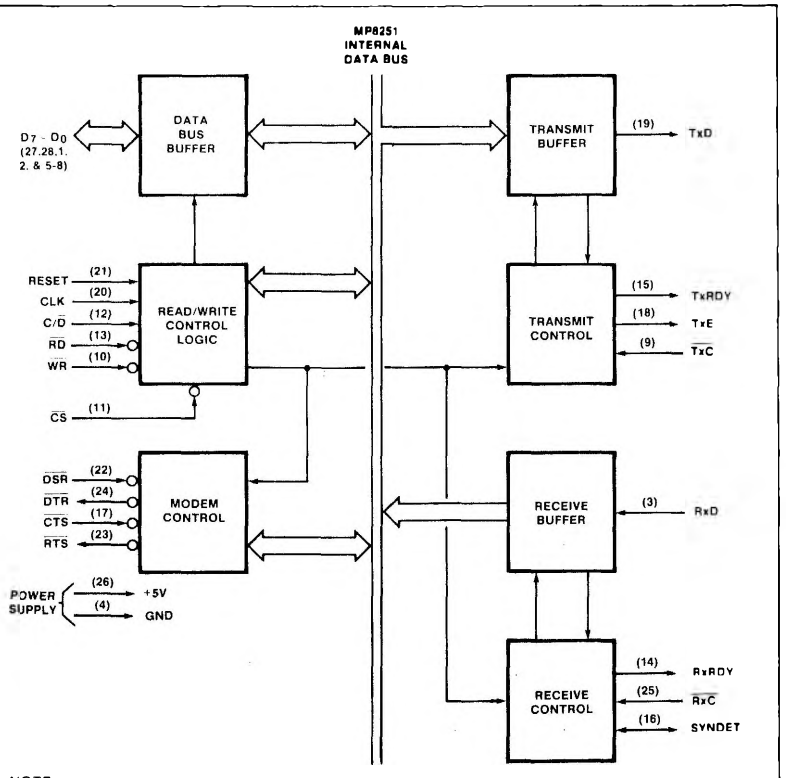
Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

BLOCK DIAGRAMS

MP8080A MICROCOMPUTER FAMILY BLOCK DIAGRAM



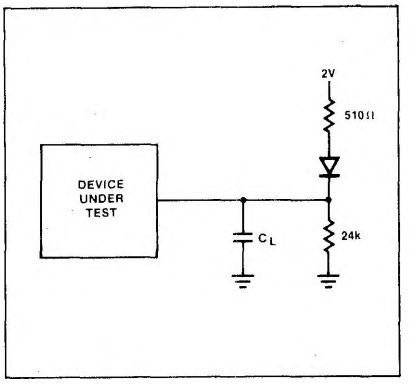
BLOCK DIAGRAMS (Cont'd)

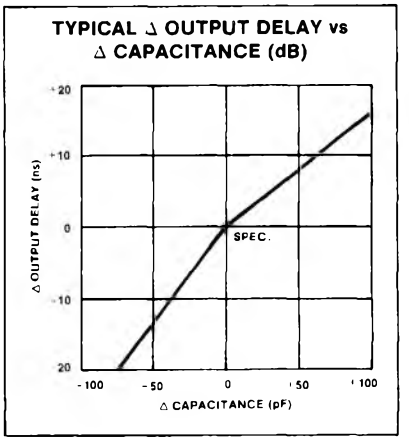


NOTE

Applicable pinout numbers are included within parentheses.

TEST LOAD CIRCUIT





DC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%; GND = 0V.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IH}	High		2.0		V_{CC}	
V_{IL}	Low		-0.5		0.8	
	Output voltage					V
V_{OH}	High	I_{OH} = -100μA	2.4			
V_{OL}	Low	I_{OL} = 1.6mA			0.45	
	Leakage					μA
I_{DL}	Data bus	V_{OUT} = 0.45V			-50	
		V_{OUT} = V_{CC}			10	
I_{IL}	Input	V_{IN} = V_{CC}			10	
I_{CC}	Power supply current			45	80	mA
	Capacitance	T_A = 25°C; V_{CC} = GND = 0V				pF
C_{IN}	Input	f_c = 1MHz			10	
$C_{I/O}$	I/O	Unmeasured pins returned to GND			20	

AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$; $V_{CC} = 5.0V \pm 5\%$; GND = 0V.

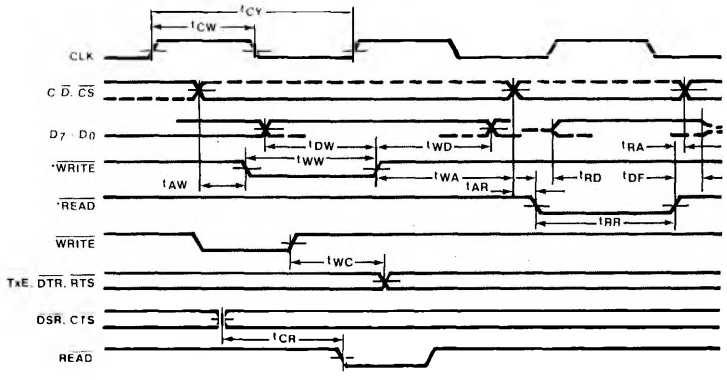
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
BUS PARAMETERS[1]						
Read Cycle						
t_{AR}	Address stable before $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)		50			ns
t_{RA}	Address hold time for $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)		5			ns
t_{RR}	$\overline{READ}$ pulse width		430			ns
t_{RD}	Data delay from $\overline{READ}$	C_L = 100pF			350	ns
t_{DF}	$\overline{READ}$ to data floating	C_L = 100pF			200	ns
		C_L = 15pF	25			ns
t_{RV}	Recovery time between WRITES[2]		6			t_{CY}
Write Cycle						
t_{AW}	Address stable before $\overline{WRITE}$		20			ns
t_{WA}	Address hold time for $\overline{WRITE}$		20			ns
t_{WW}	$\overline{WRITE}$ pulse width		400			ns
t_{DW}	Data set-up time for $\overline{WRITE}$		200			ns
t_{WD}	Data hold time for $\overline{WRITE}$		40			ns
OTHER TIMINGS						
t_{CY}	Clock period[3]		0.420		1.35	μs
$t_{\phi W}$	Clock pulse width		220		0.7t_{CY}	ns
t_R, t_F	Clock rise and fall time		0		50	ns
t_{DTx}	TxD delay from falling edge of $\overline{TxC}$	C_L = 100pF			1	μs
t_{SRx}	Rx data set-up time to sampling pulse	C_L = 100pF	2			μs
t_{HRx}	Rx data hold time to sampling pulse	C_L = 100pF	2			μs
f_{Tx}	Transmitter input clock frequency					
	1x baud rate		DC		56	kHz
	16x and 64x baud rate		DC		520	kHz
t_{TPW}	Transmitter input clock pulse width					
	1x baud rate		12			t_{CY}
	16x and 64x baud rate		1			t_{CY}
t_{TPD}	Transmitter input clock pulse delay					
	1x baud rate		15			t_{CY}
	16x and 64x baud rate		3			t_{CY}
f_{Rx}	Receiver input clock frequency					
	1x baud rate		DC		56	kHz
	16x and 64x baud rate		DC		520	kHz
t_{RPW}	Receiver input clock pulse width					
	1x baud rate		12			t_{CY}
	16x and 64x baud rate		1			t_{CY}
t_{RPD}	Receiver input clock pulse delay					
	1x baud rate		15			t_{CY}
	16x and 64x baud rate		3			t_{CY}
t_{Tx}	TxRDY delay from center of data bit	C_L = 50pF			16	t_{CY}
t_{Rx}	RxRDY delay from center of data bit				20	t_{CY}
t_{IS}	Internal SYNDET delay from center of data bit				25	t_{CY}
t_{ES}	Internal SYNDET set-up time before falling edge of $\overline{RxC}$				16	t_{CY}
t_{TxE}	TxEMPTY delay from center of data bit	C_L = 50pF			16	t_{CY}
t_{WC}	Control delay from rising edge of $\overline{WRITE}$ ($\overline{TxE}$, $\overline{DTR}$, $\overline{RTS}$)				16	t_{CY}
t_{CR}	Control to $\overline{READ}$ set up time ($\overline{DSR}$, $\overline{CTS}$)				16	t_{CY}

NOTES

1. AC timings measured at V_{OH} = 2.0V, V_{OL} = 0.8V, and with test load circuit.
2. This recovery time is for initialization only, when MODE, SYNC1, SYNC2, COMMAND and first DATA BYTES are written into the USART. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.
3. The $\overline{TxC}$ and $\overline{RxC}$ frequencies have the following limitations with respect to CLK: for 1x baud rate, f_{Tx} or $f_{Rx} \leq 1/30\ t_{CY}$) for 16x and 64x baud rate, f_{Tx} or $f_{Rx} \leq 1/4.5\ t_{CY}$)

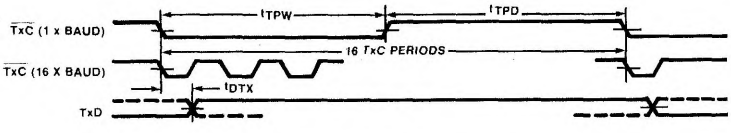
TIMING WAVEFORMS

READ AND WRITE TIMING

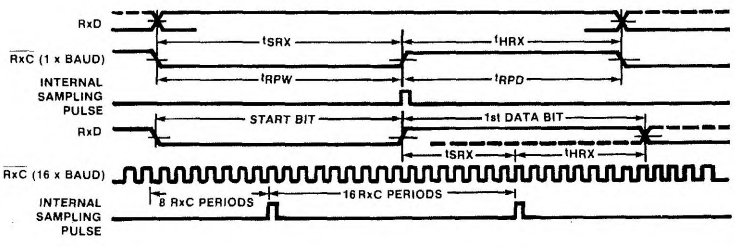


*Write and read pulses have no timing limitation with respect to CLK.

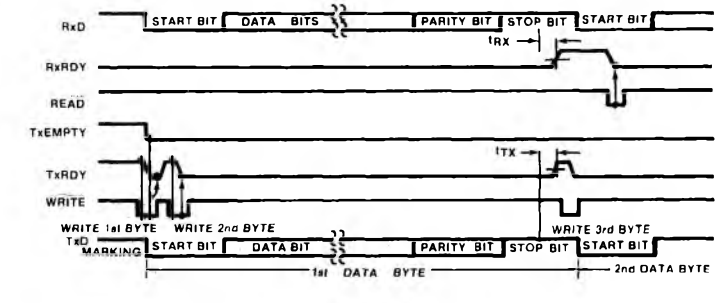
TRANSMITTER CLOCK AND DATA



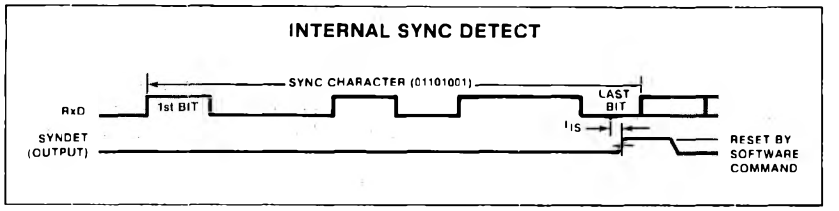
RECEIVER CLOCK AND DATA

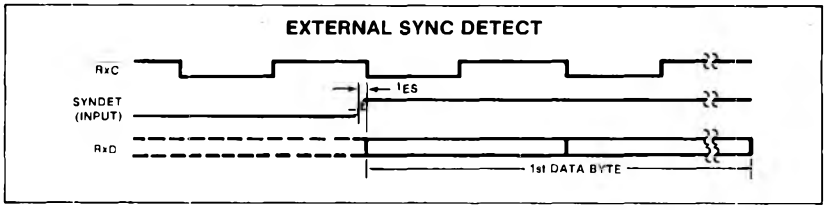


TxRDY AND RxRDY TIMING (ASYNC MODE)

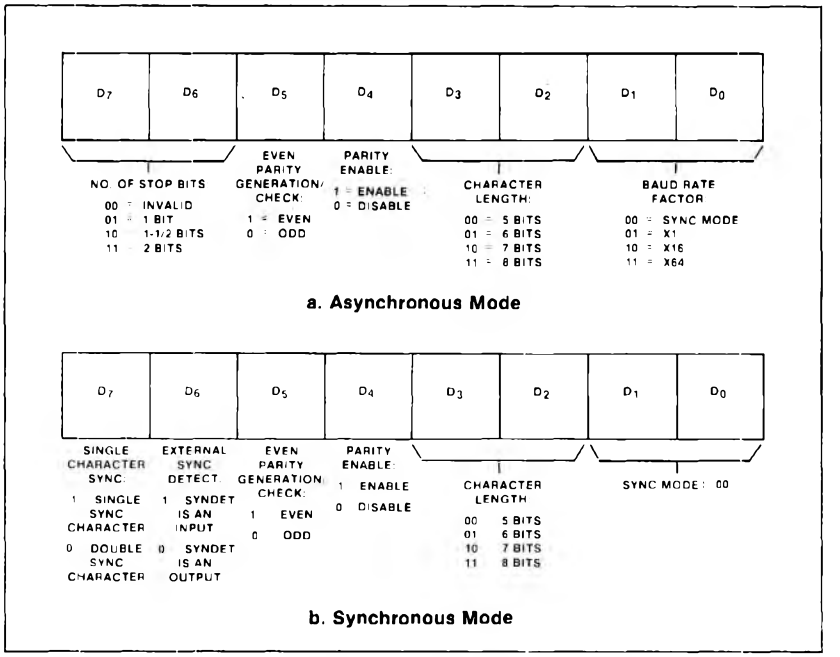


TIMING WAVEFORMS (Cont'd)

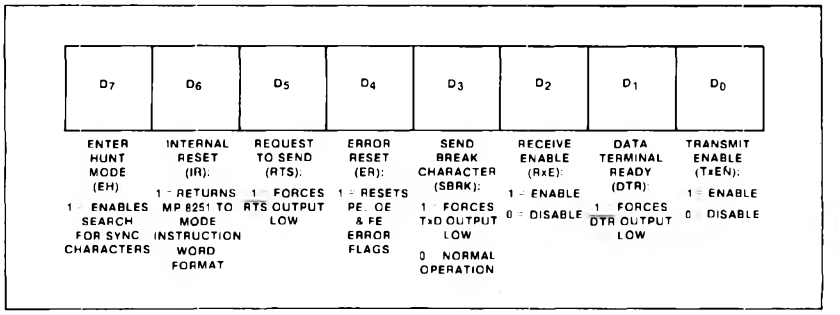




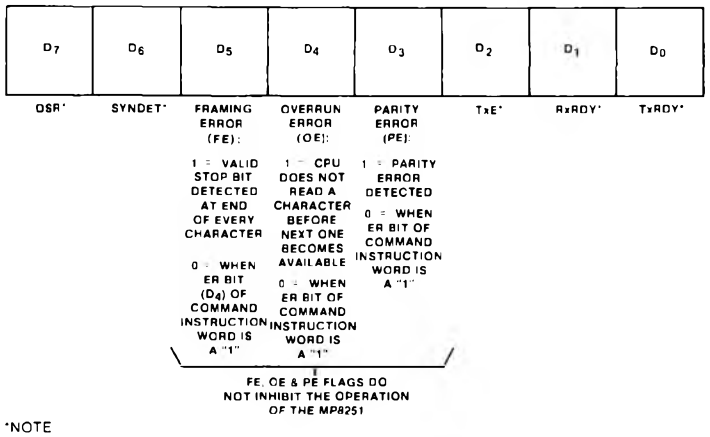
MODE INSTRUCTION CONTROL WORD FORMAT



COMMAND INSTRUCTION CONTROL WORD FORMAT

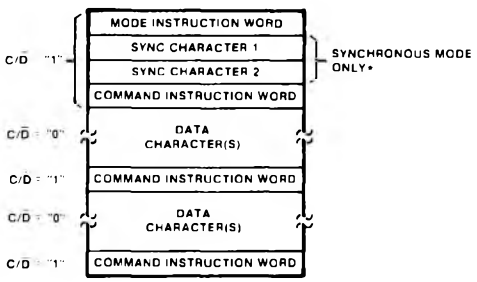


STATUS READ WORD FORMAT



*NOTE
Bits D_0-D_2, D_6 & D_7 have identical meanings to external output pins.

TYPICAL DATA BLOCK TRANSFER



*NOTE
When the mode instruction word has programmed the MP8251 to single sync character (bit D_7 = "1"), sync character 2 is omitted. Both sync characters are omitted in the asynchronous mode.

MP8251 STATUS

The MP8251 has provisions for allowing the programmer to read the status of the device at any time during the functional operation. When the C/$\overline{D}$ input is a high-level, a normal read operation is executed to read this status information. The figure below shows the bits in the Status Read Word format. Since some of the status word bits have identical meaning to external output pins, the MP8251 can be used in a completely polled environment or in an interrupt driven environment.