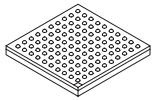
Order Number: MPC9895/D
Rev 0, 04/2003

Product Preview

Low Voltage PLL Intelligent Dynamic Clock (IDCS) Switch

MPC9895

3.3V IDCS AND PLL CLOCK GENERATOR



VF SUFFIX
100 MAPBGA PACKAGE
CASE 1462

The MPC9895 is a 3.3V compatible, PLL based intelligent dynamic clock switch and generator specifically designed for redundant clock distribution systems. The device receives two LVCMOS clock signals and generates 12 phase aligned output clocks. The MPC9895 is able to detect a failing reference clock signal and to dynamically switch to a redundant clock signal. The switch from the failing clock to the redundant clock occurs without interruption of the output clock signal (output clock slews to alignment). The phase bump typically caused by a clock failure is eliminated.

The device offers 12 low skew clock outputs organized into two output banks.

The extended temperature range of the MPC9895 supports telecommunication and networking requirements. The device employs a fully differential PLL design to minimize jitter.

Features

- 12 output LVCMOS PLL clock generator
- 3.3V compatible
- IDCS - on-chip intelligent dynamic clock switch
- Automatically detects clock failure
- Smooth output phase transition during clock failover switch
- 50 - 200 MHz output frequency range
- LVCMOS compatible inputs and outputs
- External feedback enables zero-delay configurations
- Supports networking, telecommunications and computer applications
- Output enable/disable and static test mode (PLL bypass)
- Low skew characteristics: maximum 150 ps[1] output-to-output
- 100 ball MAPBGA package, 1 mm ball pitch
- Ambient temperature range –40°C to +85°C

Functional Description

The MPC9895 is a 3.3V compatible PLL clock driver and clock generator. The clock generator uses a fully integrated PLL to generate clock signals from redundant clock sources. The PLL multiplies the input reference clock signal by 4, 8, 16 or 32. The frequency-multiplied clock drives six bank A outputs and six bank B outputs. Bank A and bank B outputs are phase-aligned. Due to the external PLL feedback, the clock signals of both output banks are also phase-aligned to the selected input reference clock, providing virtually zero-delay capability. The integrated IDCS continuously monitors both clock inputs and indicates a clock failure individually for each clock input. When a false clock signal is detected, the MPC9895 switches to the redundant clock input, forcing the PLL to slowly slew to alignment and not produce any phase bumps at the outputs. Both clock inputs are interchangeable. The automatic switch operation to a restored (fixed) clock signal is also supported. The MPC9895 also provides a manual mode that allows for user-controlled clock switches.

The PLL bypass of the MPC9895 disables the IDCS and PLL-related PLL specifications do not apply. In PLL bypass mode, the MPC9895 is fully static in order to distribute low-frequency clocks for system test and diagnosis. Outputs of the MPC9895 can be disabled (high-impedance state) to isolate the device from the system. Applying output disable also resets the MPC9895. On power-up this reset function needs to be applied for correct operation of the circuitry. Please see the application section for power-on sequence recommendations.

The device is packaged in 100-ball MAPBGA package.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

1. Final specification subject to change

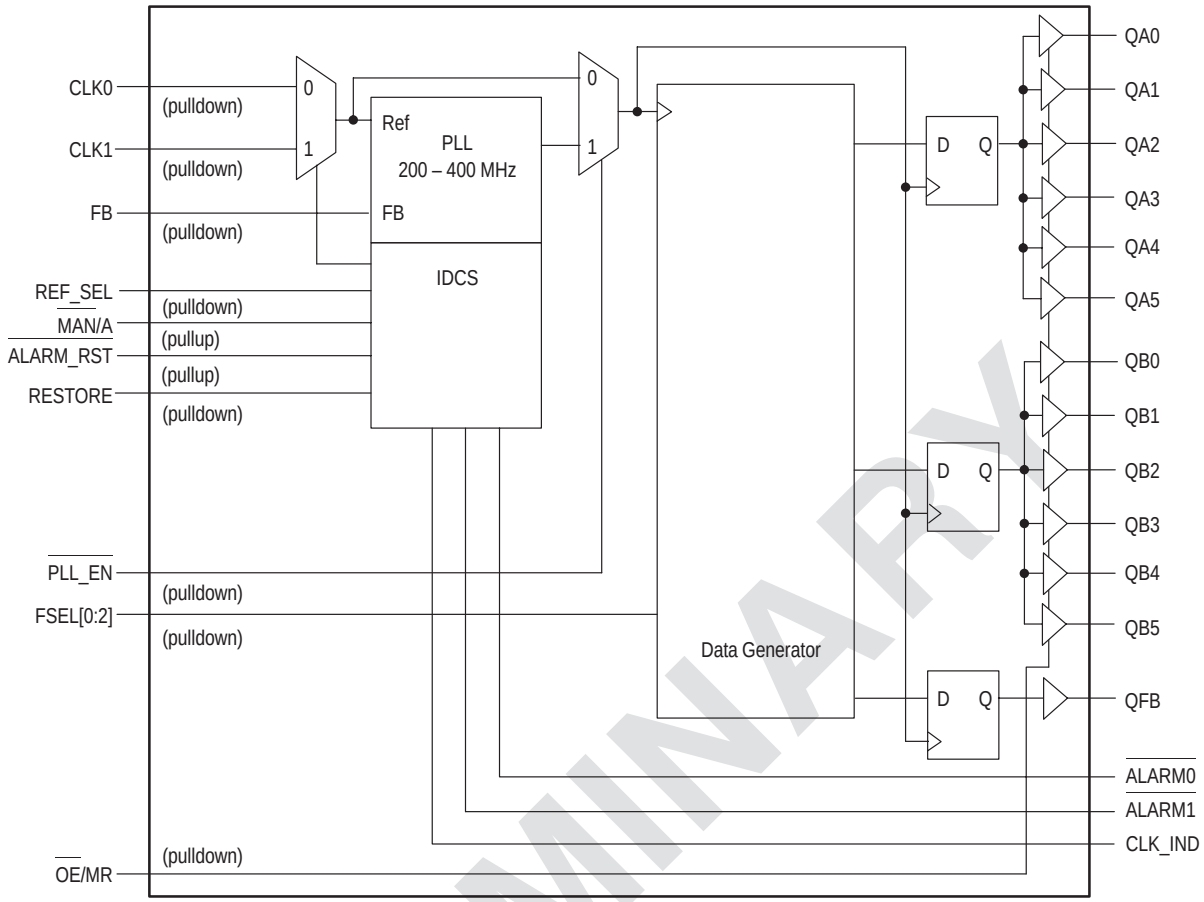


Figure 1. MPC9895 Logic Diagram

Table 1. SIGNAL CONFIGURATIONS

Signal	I/O	Type	Function
CLK0, CLK1	Input	LVCMOS	PLL reference clock inputs
FB	Input	LVCMOS	PLL feedback signal input, connect directly to QFB output
REF_SEL	Input	LVCMOS	Selects the primary reference clock
MAN/A	Input	LVCMOS	Selects switch mode and alarm flag reset
ALARM_RST	Input	LVCMOS	Reset of alarm flags and selected reference clock indicator
RESTORE	Input	LVCMOS	Selects the automatic restore mode
PLL_EN	Input	LVCMOS	Selects PLL or static test mode
FSEL[0:2]	Input	LVCMOS	Clock frequency selection and configuration of clock divider modes
OE/MR	Input	LVCMOS	Output enable/disable, device reset
QA[0:5]	Output	LVCMOS	Bank A clock outputs
QB[0:5]	Output	LVCMOS	Bank B clock outputs
QFB	Output	LVCMOS	Clock feedback output. QFB must be connected to FB for correct operation
ALARM0	Output	LVCMOS	Indicates clock failure on CLK0
ALARM1	Output	LVCMOS	Indicates clock failure on CLK1
CLK_IND	Output	LVCMOS	Indicates currently selected input reference clock
GND	Supply	Ground	Negative power supply
VCC_PLL	Supply	VCC	Positive power supply for the PLL (analog power supply). It is recommended to use an external RC filter for the analog power supply pin VCC_PLL. Please see the application section for details.
VCC	Supply	VCC	Positive power supply for I/O and core

Table 2. FUNCTION TABLE

Control	Default	0	1
Inputs			
PLL_EN	0	PLL enabled. The input to output frequency relationship is according to Table 3 if the PLL is frequency locked.	PLL bypassed and IDCS disabled. The VCO output is replaced by the reference clock signal fref. The MPC9895 is in manual mode.
MAN/A	1	Manual clock switch mode. **IDCS disabled**. Clock failure detection and output flags ALARM0, ALARM1, CLK_IND are enabled. Low-to-high transition: ALARM0, ALARM1 and CLK_IND flags are reset: ALARM0=H, ALARM1=H and CLK_IND=REF_SEL.	Automatic clock switch mode. **IDCS enabled**. Clock failure detection and output flags ALARM0, ALARM1, CLK_IND are enabled. IDCS overrides REF_SEL on a clock failure. IDCS operation requires PLL_EN = 0.
ALARM_RST	1	ALARM0, ALARM1 and CLK_IND flags are reset: ALARM0=H, ALARM1=H and CLK_IND=REF_SEL. ALARM_RST is an one-shot function.	ALARM0, ALARM1 and CLK_IND active
RESTORE	0	RESTORE operation is disabled	The IDCS attempts to automatically restore the primary clock source defined by REF_SEL. This operation requires PLL_EN = 0 and MAN/A=1
REF_SEL	0	Selects CLK0 as the primary clock source	Selects CLK1 as the primary clock source
FSEL[0:2]	00	See Table 3	
OE/MR	0	Outputs enabled (active)	Logic 1: Outputs disabled (high impedance state), reset of data generators and output dividers. The MPC9895 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than two reference clock cycles (CLK0,1). MR/OE does not affect the QFB output.
Outputs (ALARM0, ALARM1, CLK_IND are valid if PLL is locked)			
ALARM0		CLKO failure	
ALARM1		CLK1 failure	
CLK_IND		CLKO is the primary clock, CLK1 is the secondary clock	CLK1 is the primary clock, CLK0 is the secondary clock

Table 3. CLOCK FREQUENCY CONFIGURATION

Name	FSEL0	FSEL1	FSEL2	f_{REF} range [MHz]	QAx and QBx		QFB	M	N
					Ratio	f_{QAX} [MHz]			
M16H	0	0	0	6.25—12.5	$f_{REF} \cdot 16$	100—200	f_{REF}	32	2
M8L	0	1	0	6.25—12.5	$f_{REF} \cdot 8$	50—100	f_{REF}	32	4
M32	1	0	0	3.125—6.25	$f_{REF} \cdot 32$	100—200	f_{REF}	64	2
M16L	1	1	0	3.125—6.25	$f_{REF} \cdot 16$	50—100	f_{REF}	64	4
M8H	0	0	1	12.5—25.0	$f_{REF} \cdot 8$	100—200	f_{REF}	16	2
M4	0	1	1	12.5—25.0	$f_{REF} \cdot 4$	50—100	f_{REF}	16	4
	1	0	1	n/a					
	1	1	1	n/a					

Table 4. 100 BALL MAPBGA SIGNAL ALIGNMENT[a]

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
$\overline{\text{MAN}}$/A	A1	FB	C1	CLK1	E1	VCC_PLL	G1	$\overline{\text{ALARM1}}$	J1
QA5	A2	GND	C2	VCC	E2	GND	G2	VCC	J2
QA4	A3	VCC	C3	VCC	E3	VCC	G3	GND	J3
GND	A4	VCC	C4	GND	E4	GND	G4	VCC	J4
QA3	A5	VCC	C5	GND	E5	GND	G5	VCC	J5
QA2	A6	VCC	C6	GND	E6	GND	G6	GND	J6
VCC	A7	VCC	C7	GND	E7	GND	G7	GND	J7
QA1	A8	VCC	C8	VCC	E8	VCC	G8	VCC	J8
QA0	A9	VCC	C9	GND	E9	GND	G9	VCC	J9
GND	A10	REF_SEL	C10	FSEL0	E10	FSEL2	G10	$\overline{\text{OE}}$/MR	J10
QFB	B1	CLK0	D1	VCC_PLL	F1	$\overline{\text{ALARM0}}$	H1	CLK_IND	K1
VCC	B2	VCC	D2	GND	F2	GND	H2	QB5	K2
GND	B3	VCC	D3	VCC	F3	VCC	H3	QB4	K3
VCC	B4	GND	D4	GND	F4	VCC	H4	GND	K4
VCC	B5	GND	D5	GND	F5	VCC	H5	QB3	K5
GND	B6	GND	D6	GND	F6	VCC	H6	QB2	K6
GND	B7	GND	D7	GND	F7	VCC	H7	VCC	K7
VCC	B8	VCC	D8	VCC	F8	VCC	H8	QB1	K8
VCC	B9	GND	D9	GND	F9	VCC	H9	QB0	K9
$\overline{\text{ALARM\_RST}}$	B10	$\overline{\text{PLL\_EN}}$	D10	FSEL1	F10	RESTORE	H10	GND	K10

a. See “MAPBGA Pin Configurations diagram (Bottom View)” on page 10.

Table 5. GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch–Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 6. ABSOLUTE MAXIMUM RATINGS[a]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.9	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 7. DC CHARACTERISTICS (V_{CC} = 3.3V ± 5%, T_A = –40°C to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input low voltage			0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-24 mA[a]
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL}= 24 mA I_{OL}= 12 mA
Z_{OUT}	Output impedance		14-17		Ω	
I_{IN}	Input Current			±200	µA	V_{IN}=V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current		2	5	mA	V_{CC_PLL} balls
I_{CC}	Maximum Quiescent Supply Current			4	mA	All V_{CC} balls
V_{TT}.	Output termination voltage		V_{CC}÷2		V	

a. The MPC9895 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

Table 8. AC CHARACTERISTICS (V_{CC} = 3.3V ± 5%, T_A = –40°C to +85°C)[a] [b]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	FSEL= 000 FSEL= 010 FSEL= 100 FSEL= 110 FSEL= 001 FSEL= 011	6.25 6.26 3.125 3.125 12.5 12.5		12.5 12.5 6.25 6.25 25.0 25.0	MHz MHz MHz MHz MHz MHZ	PLL locked
f_{MAX}	Maximum Output Frequency	FSEL= 000 FSEL= 010 FSEL= 100 FSEL= 110 FSEL= 001 FSEL= 011	100 50 100 50 100 50		200 100 200 100 200 100	MHz MHz MHz MHz MHz MHz	PLL locked
f_{refDC}	Reference Input Duty Cycle		40		60	%	
tr, tf	CLK0, 1 Input Rise/Fall Time				1.0	ns	0.8 to 2.0V
$t_{(\varnothing)}$	Propagation Delay (static phase offset, CLKx to FB)			±3		ns	PLL locked
Δ t	Rate of period change (phase slew rate)	FSEL=x0x FSEL=x1x		150 300		ps/cycle	MAN/A = 1 MAN/A = 1
N_F	IDCS Switch Delay[c]		1			T	
N_R	IDCS Restore Delay[d]		64			T	
$t_{sk(O)}$	Output-to-output Skew[e]	(within bank) (bank-to-bank)			50 100	ps ps	
DC_O	Output duty Cycle		45	50	55	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time				10	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter				100	ps	
$t_{JIT(PER)}$	Period Jitter				TBD	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter			±2		ns	
BW	PLL closed loop bandwidth[f]	FSEL=0x FSEL=1x		TBD TBD		MHz MHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

a. All AC characteristics are design targets and subject to change upon characterization.
b. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
c. Number of input clock cycles for clock failure detection. T=period of the feedback clock signal.
d. Number of consecutive, valid clock cycles of an input clock signal. T=period of the feedback clock signal.
e. See application section for part-to-part skew calculation.
f. -3dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Definitions

IDCS: Intelligent Dynamic Clock Switch. The IDCS monitors both primary and secondary clock signals. Upon a failure of the primary clock signal, the IDCS switches to a valid secondary clock signal and status flags are set.

Reference clock signal fref: The clock signal that is selected by the IDCS or REF_SEL as the input reference to the PLL.

Manual mode: The reference clock frequency is selected by REF_SEL.

Automatic mode: The reference clock frequency is selected by the internal IDCS logic.

Primary clock: The input clock signal selected by REF_SEL. The primary clock may or may not be the reference clock, depending on switch mode and IDCS status.

Secondary clock: The input clock signal not selected by REF_SEL

Selected clock: The CLK_IND flag indicates the reference clock signal: CLK_IND = 0 indicates CLK0 is the clock reference signal, CLK_IND =1 indicates CLK1 is the reference clock signal.

Clock failure: A valid clock signal that is stuck (high or low) for at least one input clock period (N_F>1). The primary clock and the secondary clock is monitored for failure. Valid clock signals must be within the AC and DC specification for the input reference clock. A loss of clock is detected if as well as the loss of both clocks. In the case of both clocks are lost, the MPC9895 will set the alarm flags and the VCO will run at its lowest frequency. The PLL will not be locked. The MPC9895 has to be reset by OE/MR to recover from this situation, it is recommended to re-apply the startup sequence and to use the manual mode (MAN/A=0) to select the primary clock.

The MPC9895 does not monitor and detect changes in the input frequency.

Automatic mode and IDCS commanded clock switch

$\overline{\text{MAN/A}}$ = 1, IDCS enabled: Both primary and secondary clocks are monitored. The first clock failure is reported by its ALARMx status flag (clock failure is indicated by a logic low). The ALARMx status is flag latched and remains latched until reset by assertion of ALARM_RST (if RESTORE=0) or the input clock is fixed (if RESTORE=1).

If the clock failure occurs on the primary clock, the IDCS attempts to switch to the secondary clock. The secondary clock signal needs to be valid for a successful switch. CLK_IND indicates the reference clock signal. Upon a successful switch, CLK_IND indicates the reference clock, which may now be different as that originally selected by REF_SEL.

Clock restore operation

If the RESTORE input is asserted (RESTORE=1, $\overline{\text{MAN/A}}$ = 1) the IDCS attempts to restore the primary clock after a clock failure. After a successful IDCS-commanded clock switch, REF_SEL is not equal to CLK_IND. The IDCS continues to monitor the primary and secondary clock. If the primary clock becomes valid for at least 64 consecutive cycles (N_R>64), the IDCS attempts to switch back to the primary clock (restore the primary clock).

Upon a successful clock restore operation, the primary clock is the reference clock, CLK_IND will be equal to REF_SEL and the ALARMx flags are cleared.

If REF_SEL is equal to the CLK_IND flag (no clock failure occurred) the IDCS does not change the selected input clock. Deassertion of RESTORE disables the clock restore option and the clock selection must be reset manually.

Manual mode

$\overline{\text{MAN/A}}$ = 0, IDCS disabled: PLL functions normally and both clocks are monitored. The reference clock signal will always be the clock signal selected by REF_SEL and will be indicated by CLK_IND. The clock restore feature is disabled in manual mode.

Clock output transition

A clock switch, either in automatic or manual mode, follows the next negative edge of the newly selected reference clock signal. The feedback and newly selected reference clock edge will start to slew to alignment at the next positive edge of both signals. Output runt pulses are eliminated.

Reset

ALARM_RST is asserted by a negative edge. It generates a one-shot reset pulse that clears both ALARMx latches and the CLK_IND latch. If both CLK0 and CLK1 are invalid or fail when ALARM_RST is asserted, both ALARMx flags will be latched after one FB signal period and CLK_IND will be latched (L) indicating CLK0 is the reference signal. While neither ALARMx flag is latched (ALARMx = H), the CLK_IND can be freely changed with REF_SEL.

OE/MR: Reset the data generator and output disable.

MAN/A: The rising edge of OE/MR resets ALARMx and CLK_IND as ALARM_RST does.

Acquiring frequency lock (startup sequence)

1. On startup, OE/MR must be asserted to reset the output dividers. The IDCS should be disabled (MAN/A=0) and RESTORE should be logic low (disable restore option) during startup. REF_SEL selects the primary clock.
2. Release OE/MR and the PLL will attempt to gain lock if the primary clock is present. PLL lock requires the specified lock time.
3. Enable the IDCS automatic mode ($\overline{\text{MAN/A}}$=1). The rising edge of the MAN/A signal clears the alarm flags and CLK_IND. The IDCS will now report clock failures by asserting ALARMx flags.
4. Enable the restore option (RESTORE=1) if needed.

Power Supply Filtering

The MPC9895 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the VCC_PLL (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9895 provides separate power supplies for the output buffers (V_{CC}) and the

phase-locked loop (VCC_PLL) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the VCC_PLL pin for the MPC9895. Figure 2. illustrates a typical power supply filter scheme. The MPC9895 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CC_PLL} current (the current sourced through the VCC_PLL pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 3.0V must be maintained on the VCC_PLL pin. The resistor R_F shown in Figure 2. "VCC_PLL Power Supply Filter" must have a resistance of 9-10Ω to meet the voltage drop criteria.

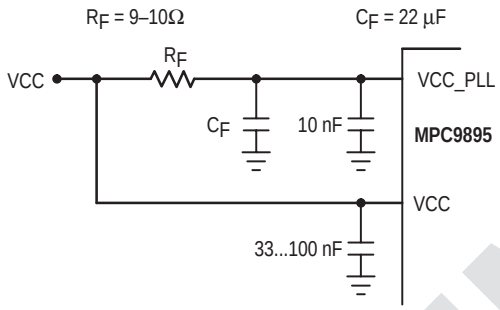


Figure 2. VCC_PLL Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 2. "VCC_PLL Power Supply Filter", the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9895 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC9895 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9895 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3. "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9895 clock driver is effectively doubled due to its capability to drive multiple lines.

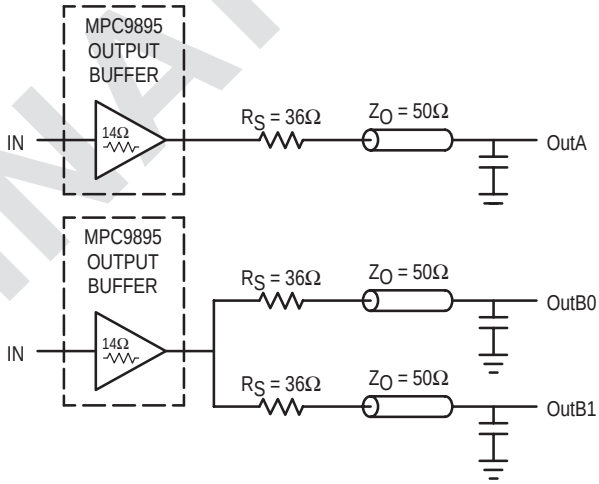


Figure 3. Single versus Dual Transmission Lines

The waveform plots in Figure 4. "Single versus Dual Line Termination Waveforms" show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9895 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9895. The output waveform in Figure 4. "Single versus Dual Line Termination Waveforms" shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\Omega \,||\, 50\Omega$$
$$R_S = 36\Omega \,||\, 36\Omega$$
$$R_0 = 14\Omega$$
$$V_L = 3.0 (25 \div (18+17+25)$$
$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

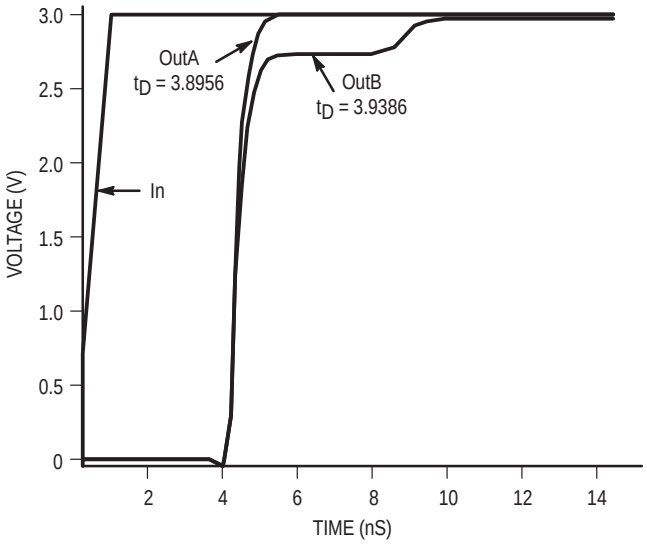
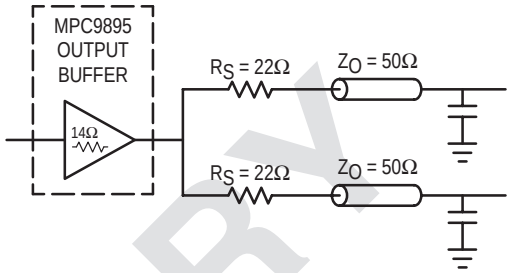


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5. “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



14Ω + 22Ω || 22Ω = 50Ω || 50Ω
25Ω = 25Ω

Figure 5. Optimized Dual Line Termination

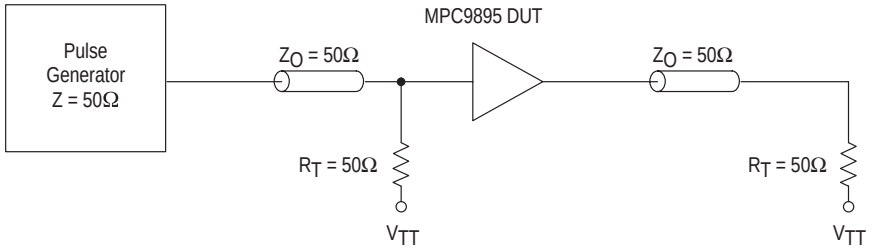
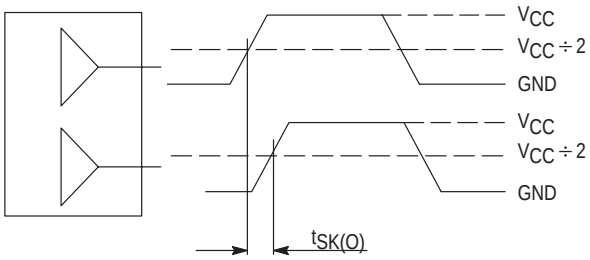


Figure 6. CLK0, CLK1 MPC9895 AC test reference



The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 7. Output–to–output Skew $t_{SK(O)}$

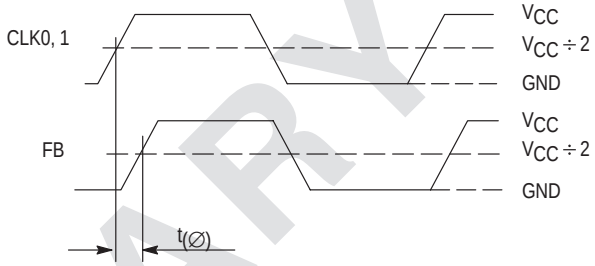
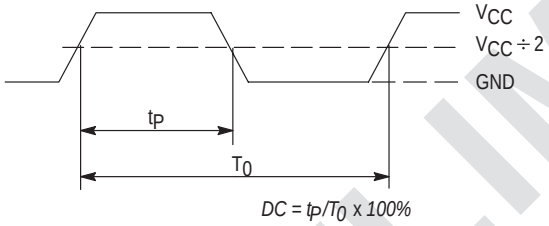
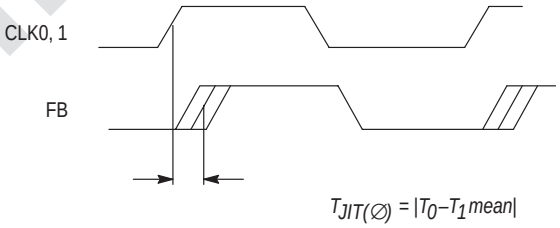


Figure 8. Propagation delay ($t_{(\varnothing)}$, static phase offset) test reference



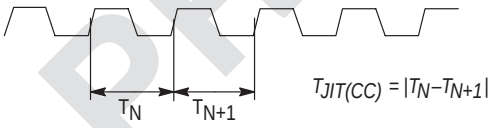
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 9. Output Duty Cycle (DC)



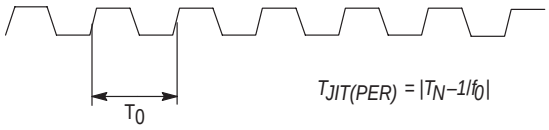
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 10. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 11. Cycle–to–cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 12. Period Jitter

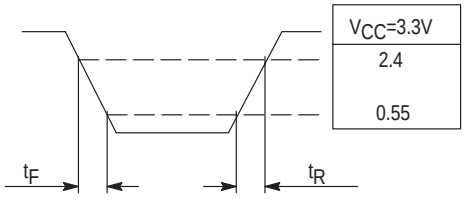


Figure 13. Output Transition Time Test Reference

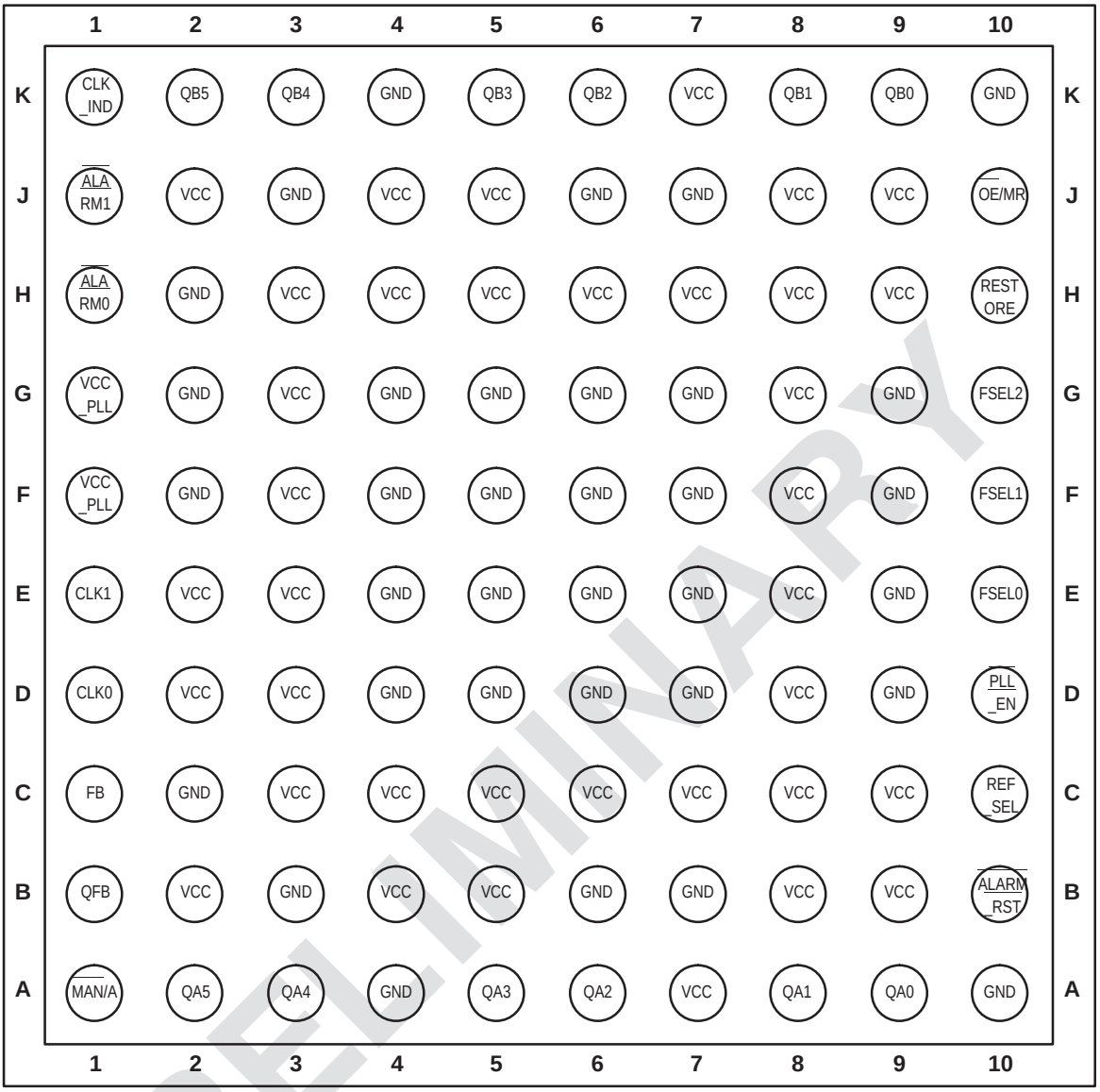
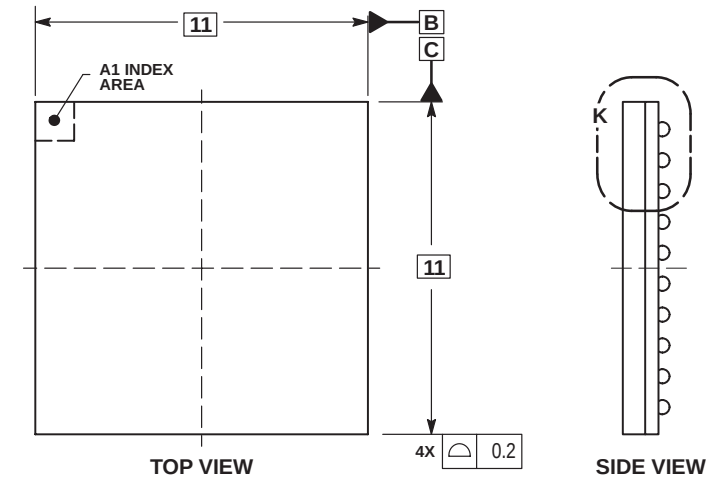


Figure 14. MAPBGA Pin Configurations (Bottom View)

OUTLINE DIMENSIONS

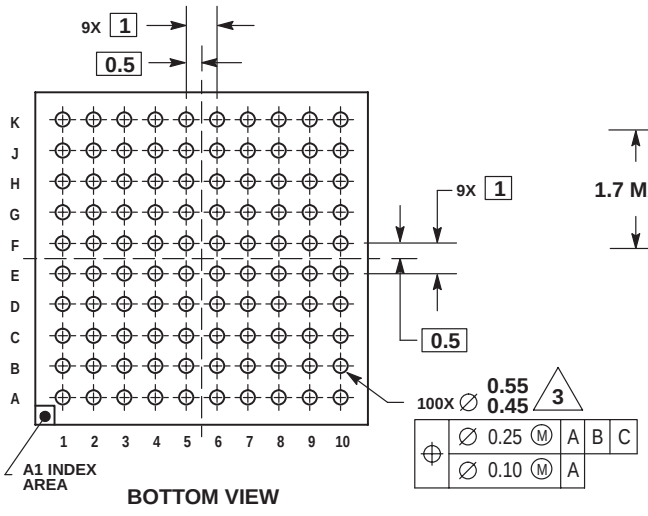
VF SUFFIX
100–LEAD MAP BGA PACKAGE
CASE 1462-01
ISSUE O



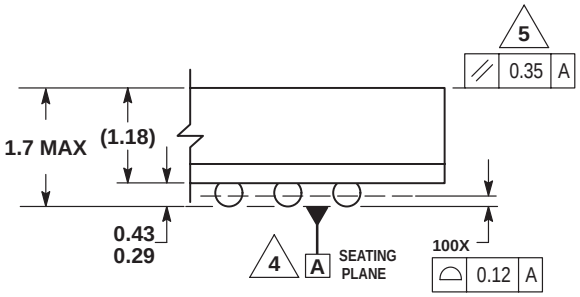
TOP VIEW

SIDE VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGING



BOTTOM VIEW



DETAIL K
ROTATED 90 °CLOCKWISE

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