Freescale Semiconductor
Product Brief

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MSC8251/MSC8252 Product Brief

One and Two Core DSPs

The MSC8251 and MSC8252 devices are fourth generation of Freescale DSP devices that target voice, medical, defense, and general applications. The DSPs build upon the proven success of the previous StarCore-based DSPs and are designed to support mathematically intensive algorithms and applications.

Contents

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1 Example Applications

The applications covered in this section are as follows:

- Synthetic instrument
- Radar/Sonar

1.1 Synthetic Instrument

The MSC8251 and MSC8252 DSPs promote easy system building for legacy, transition, and generation system interface requirements through flexible and varied I/O protocol support. The tremendous processing power in these devices make them a perfect fit for a synthetic instrument platform for test and measurement applications. A generic synthetic instrument block diagram is shown in Figure 1.

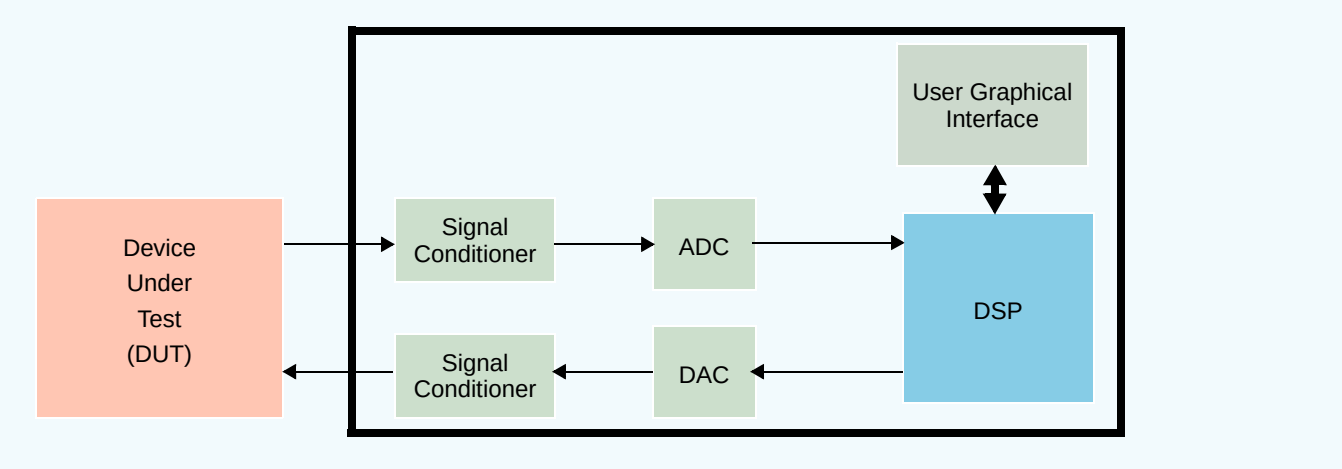

Figure 1. Generic Synthetic Instrument Block Diagram

The synthetic instrument approach can create ideal replacements for numerous legacy general-purpose RF/microwave and baseband stimulus/measurement systems that are fast approaching obsolescence. The architecture is also appropriate for numerous applications including spectrum analysis, surveillance applications such as communication intelligence (COMINT), satellite monitoring, radar/electronic warfare characterization, frequency management, and NIST traceable calibration (microwave power measurement calibration, microwave signal generator calibration, microwave power calibration). The signal analysis portion is performed by DSP-based software that can support any number of standalone instruments.

1.2 Radar/Sonar System

In the system shown in Figure 2, the radar or sonar unit generates reflection data that is conditioned, converted to a digital signal, and processed by the DSP. Because the DSP was designed to support communications infrastructure, it includes the interfaces needed to connect directly to typical networks using Ethernet and serves as the communications processor in the system. Because of its overall computing power, the DSP can also perform display and image processing concurrently with data signal analysis. The other built-in the DSP interfaces (UART, SPI, and I^2C) can be used to connect to display and control interfaces.

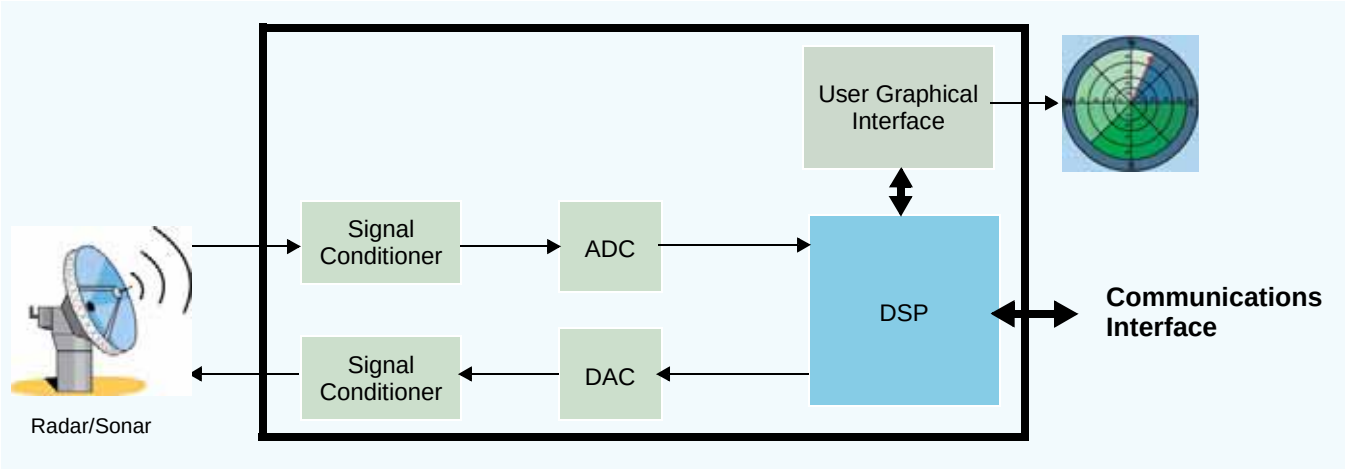

Figure 2. Radar/Sonar Block Diagram

2 Features

The MSC8251 and MSC8252 devices target high-bandwidth, highly computational DSP applications.

2.1 Block Diagram

The DSP devices are highly integrated DSP processors that contain one or two StarCore SC3850 DSP subsystems with 32 Kbyte L1 instruction cache per core, 32 Kbyte L1 data cache per core, 512 Kbyte L2 unified instruction/data cache per core (can be configured as M2 Memory); 1056 Kbyte of shared M3, memory; two DDR memory controllers, two serial RapidIO interfaces; two Gigabit Ethernet controllers; a PCI-Express controller; four 256-channel time-division multiplexing (TDM) interfaces; a 16 bidirectional channels DMA controller; an SPI interface; a UART interface; and an I^2C interface. Each SC3850 DSP core has four ALUs each with a dual 16×16 MAC per ALU and performs at 8000 million multiply accumulates per second (MMACS) at 1 GHz yielding a maximum total performance of 8000 or 16000 MMACS per device.

In each SC3850 core subsystem, the SC3850 core connects to the following:

- 32 Kbyte 8-way level 1 instruction cache (L1 ICache)
- 32 Kbyte 8-way level 1 data cache (L1 DCache)
- 512 Kbyte 8-way level 2 unified instruction/data cache (L2 Cache/M2 Memory)
- Memory management unit (MMU)
- Enhanced programmable interrupt controller (EPIC)
- Debug and profiling unit (DPU)
- Two 32-bit timers

A block diagram of the DSPs is shown in Figure 3. A separate block diagram for the SC3850 DSP core platform is shown in Figure 4.

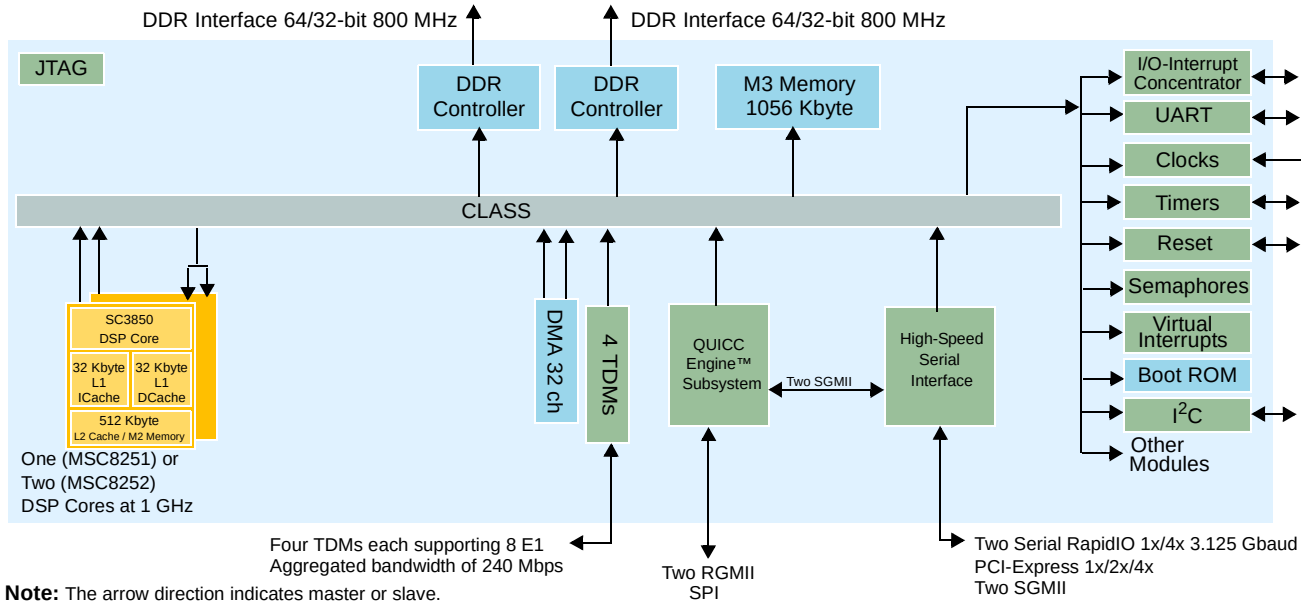

Figure 3. MSC8251/MSC8252 Block Diagram

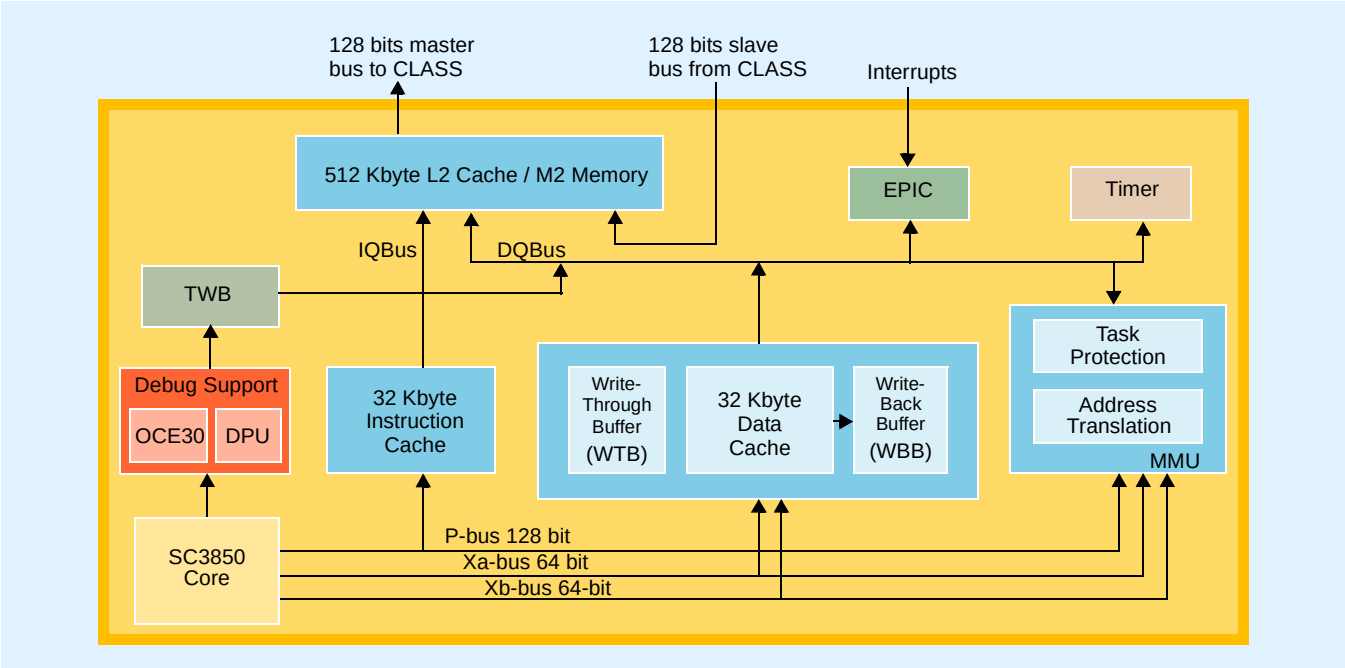

Figure 4. StarCore SC3850 DSP Subsystem Block Diagram

2.2 Critical Performance Metrics

Critical performance metrics include the following:

- Offered with a core frequency of 1 GHz, supports:
  - Eight 16 × 16 or 8 × 8 multipliers, enabling up to 8000 MMACS at 1 GHz with one SC3850 core or up to 16000 MMACS at 1 GHz for two SC3850 cores. A multiply-accumulate operation includes a multiply-add instruction with the associated data move and pointer update. This is double MMACS versus the pervious generation SC3400 DSP core.
  - The cores deliver a performance equivalent to a single core running at 1 GHz (1 core) or 2 GHz (2 core).
- Dual RISC core QUICC Engine subsystem operating at up to 500 MHz provides parallel packet processing independent of the DSP cores, allowing the cores to process data while the RISC engines manage the data flow and packetization.
- Power supplies:
  - Core power: 1 V nominal
  - I/O power: 1.0 V, 1.5 V, 1.8 V, and 2.5 V nominal
- Flip Chip-Plastic Ball Grid Array (FC-PBGA), 783-ball, 1 mm pitch, 29 mm × 29 mm

2.3 Device Level Features

This multicore DSP delivers a high level of performance and integration, combining one or two fully programmable StarCore DSP cores, each running at up to 1 GHz. An internal RISC-based QUICC Engine subsystem supports multiple networking protocols to guarantee reliable data transport over packet networks while significantly offloading such processing from the DSP cores. The DSPs embed large internal memory and supports a variety of advanced interface types, including two RapidIO interfaces, two gigabit Ethernet interfaces for network communications, a PCI-Express controller, two DDR controllers for a high-speed, industry-standard memory interface, and multichannel TDM interfaces.

2.4 Module Level Features

Module level features include the following:

- StarCore DSP subsystem. The DSP subsystem includes:
  - StarCore SC3850 core
    - Running at up to 1 GHz
    - Up to 8000 16-bit or 8-bit MMACS. A MAC operation includes a multiply-accumulate command with the associated data moves and a pointer update.
    - Backwards binary compatible with the SC140 and SC3400 architectures.
    - Data Arithmetic and Logic Unit (DALU) containing 4 ALUs, each capable of performing 2 16×16 multiply accumulate operations, effectively doubling the performance of convolution-based kernels relative to the SC3400 core
    - New instructions double the performance of complex and extended precision multiplication.
    - Address Generating Unit (AGU) containing 2 Address Arithmetic Units (AAU)
    - Up to six instructions executed in a single clock cycle: 4 DALU and 2 AGU instructions
    - Variable-length Execution Set (VLES) execution model.
    - 16 data registers, 40 bits each; 27 address registers, 32 bits each.
    - Hardware support for fractional and integer data types.
    - Four hardware loops with near-zero cycle overhead
    - Very rich 16-bit wide orthogonal instruction set.
    - Application specific instructions for Viterbi and Multimedia.
    - Special SIMD (Single instruction, multiple data) instructions working on 2-word or 4-byte operands packed in a register, enabling to perform 2 to 4 operations per instruction (8 to 16 operations per VLES)
    - New dedicated instructions accelerate FFTs, enabling a 40% cycle count reduction and improved SNR
    - User and Supervisor privilege levels, supporting a protected software model
    - New instructions and features to improve control code performance
    - Precise exceptions for memory accesses enabling good RTOS support and Soft Error corrections
    - Branch Target Buffer (BTB) for acceleration of change of flow operations
  - L1 ICache:
    - 32 Kbytes
    - 8 ways with 16 lines of 256 bytes per way
    - Multi-task support

  - Real-time support through locking flexible boundaries
  - Line pre-fetch capability
  - Software coherency support
  - Software pre-fetch support by core instructions
- L1 DCache:
  - 32 Kbytes
  - 8 ways with 16 lines of 256 bytes per way
  - Capable of serving two data accesses in parallel (XA, XB)
  - Multi-task support
  - Real-time support through locking flexible boundaries
  - Software coherency support
  - Writing policy programmable per memory segment as either writeback or writethrough
  - 0.25 Kbytes Write-Back Buffer (WBB)
  - Six 64-bit entry WTB
  - Line pre-fetch capability
  - Software pre-fetch, synchronize, and flush support by core instructions
- Unified L2 Cache/M2 Memory:
  - 512 Kbyte
  - 8 ways with 1024 indexes and a 64 byte line
  - Physically addressed
  - Dynamically configured as a DMA accessible M2 Memory
  - Maximum user flexibility for real time support through address partitioning of the cache
  - Support various write policies and methods to reduce cache inclusiveness
  - Multichannel, two dimensional software pre-fetch support
  - Software coherency support with seamless transition from L1 cache coherency operation.
- Memory management unit (MMU):
  - Highly flexible memory mapping capability
  - Provides virtual to physical address translation
  - Provides task protection
  - Supports multitasking
  - Supports precise interrupts, which enable an open RTOS.
- Debug and Profiling Unit (DPU) block:
  - Supports the debugging and profiling of the platform in cooperation with the OCE Block
  - Supports various breakpoint and event counting options
  - Supports real-time tracing to the main memory with the Trace Write Buffer (TWB)
- Extended programmable interrupt controller (EPIC)
  - 256 interrupts
  - 32 priority levels with NMI support
- Two general-purpose 32-bit timers
- Low-power design with the following modes of operation:
  - Wait processing state for peripheral operation
  - Stop processing state
  - Power down processing state
- ECC/EDC support.

- Chip-level arbitration and switching system (CLASS)

  - A full fabric that arbitrates between the DSP cores and other CLASS masters to the core M2 memory, shared M3 memory, DDR SDRAM controllers, and the device configuration control and status registers (CCSRs).
  - High bandwidth.
  - Non-blocking allows parallel accesses from multiple initiators to multiple targets.
  - Fully pipelined.
  - Low latency.
  - Per target arbitration highly optimized to the target characteristics using prioritized round-robin arbitration.
  - Reduces data flow bottlenecks and enables high-bandwidth internal data transfers.
- Internal memory. The DSP internal memory space includes:
  - 32 Kbyte L1 ICache per core.
  - 32 Kbyte L1 DCache per core.
  - 512 Kbyte unified L2 Cache/M2 Memory per core.
  - 1056 Kbyte shared M3 memory. 1024 Kbyte of M3 memory can be turned off to save power, if necessary, which reduces the M3 memory size to 32 Kbyte.
  - 96 Kbyte boot ROM accessible from the cores.
- Clocks
  - Three input clocks:
    - Global input clock.
    - Two differential input clocks (one per each serial RapidIO PLL).
  - Five PLLs:
    - Three system PLLs
    - Two serial RapidIO PLLs.
  - Clock ratios selected during reset via reset configuration pins.
  - Clock modes user-configurable after reset.
- Two DDR Controllers, each supporting:
  - Up to 400 MHz clock rate (800 MHz data rate).
  - Supports both DDR2 and DDR3 devices
  - Programmable timing supporting both DDR2 and DDR3 SDRAM (but not simultaneously)
  - Support for a 64-bit data interface (72 bits including ECC), up to 800 MHz data rate, for DDR2 and DDR3
  - Support for a 32-bit data interface (40 bits including ECC), up to 800 MHz data rate, for DDR2 and DDR3
  - Full ECC support for single-bit error correction and multi-bit error detection up to the maximum specified data rates for DDR2 and DDR3
  - Two banks of memory via two chip selects. Each chip select supports up to 1 Gbytes, the sum of the memory cannot exceed 1 Gbyte total (2 Gbyte total for the two controllers).
  - DRAM chip configurations from 64 Mbits to 4 Gbits with x8/x16 data ports
  - Support burst lengths of 4 beats for DDR2 devices
  - Support burst lengths of 4 (burst chop) and On the Fly for DDR3 devices
  - Sleep mode support for self-refresh SDRAM
  - On-die termination support
  - Supports auto refreshing

- Support for SODIMMs

- High-Speed Serial Interface (HSSI)
  - Serial RapidIO® Subsystem
    - Two serial RapidIO ports supporting 1x/4x operation up to 3.125 Gbaud with a RapidIO messaging unit and two RapidIO DMA units.
    - Each 1x/4x serial RapidIO endpoint operates at 1.25/2.5/3.125 Gbaud and complies with the following parts of Specification 1.2 of the RapidIO trade association interconnect specification:
      - Part I (input and output logical specifications)
      - Part II (message passing logical specification)
      - Part III (common transport specification)
      - Part VI (physical layer 1x LP-serial specification)
      - Part VIII (error management extension specification)
    - Each serial RapidIO port supports read, write, messages, doorbells, and maintenance accesses:
      - Small and large transport information field only
      - All priorities flow
      - Pass-through between the two ports that allows cascading devices using the serial RapidIO and enabling message/data path between the two serial RapidIO ports without core intervention. A message/data that is not designated for the specific device passes through it to the next device.
    - RapidIO Messaging Unit supports:
      - Two outbound message queues
      - Two inbound message queues
      - One outbound doorbell queue
      - One inbound doorbell queue
      - One inbound port-write queue
    - Each RapidIO DMA unit supports:
      - Four high-speed/high-bandwidth channels accessible by local and remote masters
      - Basic DMA operation modes (direct, simple chaining)
      - Extended DMA operation modes (advanced chaining and stride capability)
      - Programmable bandwidth control between channels
      - Up to 256 bytes for DMA sub-block transfers to maximize performance over the RapidIO interface
      - Three priority levels supported for source and destination transactions
  - PCI-Express Controller
    - Complies with the *PCI Express™ Base Specification, Revision 1.0a*
    - Supports root complex (RC) and endpoint (EP) configurations
    - 32- and 64-bit address support
    - x4, x2, and x1 link support
    - Supports accesses to all PCI Express memory and I/O address spaces (requestor only)

  - Supports posting of processor-to-PCI Express and PCI Express-to-memory write
  - Supports strong and relaxed transaction ordering rules
  - PCI Express configuration registers (type 0 in EP mode, type 1 in RC mode)
  - Baseline and advanced error reporting support
  - One virtual channel (VC0)
  - 256-byte maximum payload size (MAX_PAYLOAD_SIZE)
  - Supports three inbound general-purpose translation windows and one configuration window
  - Supports four outbound translation windows and one default window
  - Supports eight non-posted and four posted PCI Express transactions
  - Supports up to six priority 0 internal platform reads and eight priority 0 to 2 internal platform writes. (The maximum number of outstanding transactions at any given time is eight.)
  - Credit-based flow control management
  - Supports PCI Express messages and interrupts

- DMA Controller
  - 32 unidirectional channels, providing up to 16 memory-to-memory channels.
  - Buffer descriptor programing model.
  - Up to 1024 buffer descriptors per channel direction provide a total of 32 Kbyte buffer descriptors. Buffer descriptors can reside in M2 or DDR memories.
  - Priority-based time-multiplexing between channels, using four internal priority groups with round-robin arbitration between channels on equal priority group.
  - Earliest deadline first (EDF) priority scheme that assures task completion on time.
  - Flexible channel configuration with all channels supporting all features.
  - A flexible buffer configuration, including:
    - Simple buffers
    - Cyclic buffers
    - Single address buffers (I/O device).
    - Incremental address buffers
    - Chained buffers
    - 1D to 4D buffers, optimized for video applications
    - 1D or 2–4D complex buffers, a combination of buffer types
  - Two external DMA request (DREQ) and two $\overline{\text{DONE}}$ signal lines that allow an external device to trigger DMA transfers.
  - High bandwidth
  - Optimized for DDR SDRAM
- TDM
  - Backward-compatible with the MSC8102/MSC812x/MSC814x TDM interface
  - All the four TDM modules together support up to 1K time-slots for receive and 1K time-slots for transmit
  - Up to four independent TDM modules:
    - *Independent receive and transmit mode*. Independent transmitter and receiver. Transmitter input clock, output data, and frame sync can be configured as either input or output. Up to 256 transmit channels and up to 256 receive channels. Receiver input clock, input data, and input frame sync.

  - *Shared sync and clock mode*. Two receive and two transmit links share the same clock and frame sync. The sync can be configured as either input or output. Up to 128 transmit channels and 128 receive channels.
  - *Shared data link*. Up to four full-duplex data links can operate as either transmit or receive. All links have the same clock and frame sync. Each link supports up to 128 channels.
- Word size of 2, 4, 8, or 16-bit. All the channels share the same size.
- Hardware A-law/μ-law conversion
- Up to 62.5 Mbps data rate per TDM module
- Up to 16 Mbyte per channel buffer (granularity 8 bytes), where A/μ law buffer size has double size (16-byte granularity)
- Separate or shared interrupts for receive and transmit with two programmable receive and two programmable transmit thresholds for double buffering
- Each channel can be programmed as active or inactive
- Support either 0.5 ms (4 frames) or 1 ms (8 frames) latency
- Glueless interface to E1/T1 framers

- The QUICC Engine subsystem includes dual RISC processors and 48-Kbyte multi-master RAM to handle the Ethernet and SPI interfaces, thus off loading the tasks from the cores. The three communication controllers support:
  - Two Ethernet controllers supporting Gigabit operation
  - SPI controller
- Ethernet Controllers
  - Two Ethernet physical interfaces, each of which supports:
    - 1000 Mbps SGMII protocol using a 4-pin SerDes interface
    - 1000 Mbps RGMII protocol
  - MAC-to-MAC connection in all modes
  - Full-duplex operations
  - Full-duplex flow control feature (**IEEE** Std. 802.3x™)
  - Receive flow control frames
  - Detection of all erroneous frames as defined by **IEEE** Std. 802.3®-2002
  - Multi-buffer data structure
  - Diagnostic modes: Internal and external loopback mode and echo mode
  - Serial management interface MDC/MDIO
  - Transmitter network management and diagnostics
  - Receiver network management and diagnostics
  - VLAN Support
  - **IEEE** Std. 802.1p/Q™ QoS
  - Eight Tx/Rx queues
  - Queuing decision for IP/MAC/UDP filtering based on MAC destination addresses, IP destination address, and UDP destination port
  - Programmable maximum frame length
  - Enhanced MIB statistics
  - Optional shift of data buffer by two bytes for L3 header alignments
  - Extended features
    - IP header checksum verification and calculation

  - Parsing of frame headers and adding a frame control block at the frame head, containing L3 and L4 information for CPU acceleration

- Serial peripheral interface (SPI)
  - Four-signal interface (SPIMOSI, SPIMISO, SPICLK and SPISEL)
  - Full-duplex operation
  - Works with 32-bit data characters, or with a range from 4-bit to 16-bit data characters
  - Supports back-to-back character transmission and reception
  - Supports master or slave SPI mode
  - Supports multiple-master environment
  - Continuous transfer mode for automatic scanning of a peripheral
  - Maximum clock rate is (QUICC Engine clock)/8 in master mode and (QUICC Engine clock)/4 in slave mode (not in back-to-back operation)
  - Independent programmable baud rate generator
  - Programmable clock phase and polarity
  - Local loopback capability for testing
  - Open-drain outputs support multimaster configuration
  - Communication with Ethernet PHY for configuration and status (MIIMCOM-MII management communication protocol)
  - Multi-MIIMCOM environment with up to 32 PHYs
  - Programmable clock gap between two characters in master mode
  - Controlled by the DSP cores and the QUICC Engine RISC processors according to user configuration.
- I/O Interrupt Concentrator consolidates all chip maskable interrupt and non-maskable interrupt sources and routes them to $\overline{\text{INT\_OUT}}$, $\overline{\text{NMI\_OUT}}$, and the cores.
- UART
  - Bit rate up to 6.25 Mbps
  - Two signals for transmit data and receive data
  - Full-duplex operation
  - Standard mark/space non-return-to-zero (NRZ) format
  - 13-bit baud rate selection
  - Programmable 8-bit or 9-bit data format
  - Separately enabled transmitter and receiver
  - Programmable transmitter output polarity
  - Separate receiver and transmitter interrupt requests
  - Receiver framing error detection
  - Hardware parity checking
  - 1/16 bit-time noise detection
  - Single-wire and loop operations
- Timers
  - Two general-purpose 32-bit timers for RTOS support per SC3850 core
  - Four TMR modules, each with four 16-bit timers; cascadable timers; count up/down; programmable count modulo; count once or repeatedly; counters are preloadable; compare registers can be preloaded; counters can share available inputs; separate prescaler for each

counter; each counter has capture and compare capability; any of the following clock sources: system clock, TDM clock input, or external clock input
  - Eight software watchdog timer (SWT) modules
- Eight programmable hardware semaphores, locked by simple write access without need for read-modify-write operation by the DSP core.
- Virtual interrupts
  - Generation of 32 virtual interrupts by a simple write access
  - Generation of virtual $\overline{\text{NMI}}$ by a simple write access
- I^2C interface
  - Two-wire interface
  - Multi-master operational
  - Calling address identification interrupt
  - START and STOP signal generation/detection
  - Acknowledge bit generation/detection
  - Bus busy detection
  - Programmable clock frequency
  - On-chip filtering for spikes on the bus
- General-purpose input/output (GPIO) ports:
  - 32 GPIO ports
  - Each GPIO port can either serve the on-device peripherals or act as a programmable I/O pin
  - Sixteen GPIO pins can be configured as external interrupt inputs
  - All ports are bidirectional
  - All ports are set as GPIO inputs at system reset
  - All port values can be read while the pin is connected to an internal peripheral
  - All ports have open-drain output capability
- Boot interface options:
  - Ethernet
  - Serial RapidIO interface
  - I^2C
  - SPI
- JTAG. Test Access Port (TAP) and Boundary Scan Architecture designed to comply with **IEEE** Std. 1149.1™.
- Reduced power dissipation
  - Very low power CMOS design
  - Low-power standby modes
  - Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)
- Technology: The MSC8251 device is manufactured using CMOS 45 nm SOI technology.

3 Developer Environment

Freescale supplies a complete set of DSP development tools for the MSC8251 device. The tools provide easier and more robust ways for designers to develop optimized DSP systems. Whatever the application targets, the development environment gives the designers everything they need to exploit the advanced capabilities of the MSC8251 architecture.

3.1 Tools

The MSC8251 tool components include the following:

- *Integrated development environment (IDE).* Easy-to-use graphical user interface and project manager for configuring and managing multiple build configurations.
- *C and C++ compiler with in-line assembly.* The developer can generate highly optimized DSP code by exploiting the StarCore multiple-ALU architecture, with parallel fetch sets and high code density.
- *Librarian.* The developer can create application-specific DSP libraries for modularity.
- *Linker.* The developer can efficiently produce executables from object code and partition memory according to the application architecture; the linker supports code overlay.
- *Multicore Debugger.* Seamlessly integrated real-time, non-intrusive, multimode, multicore, and multi-DSP debugger handles highly optimized DSP algorithms. The developer can choose to debug in source code, assembly code, or mixed mode. Supports RTOS-aware debugger.
- *Royalty-free RTOS.* Included with package and includes a graphical user interface (GUI) called Kernel Aware that shows task information, interrupts, and other processing elements.
- *Software Simulator.* Full chip simulation (FCS) that allows the developer to design an application and run it on the simulator before running it on the silicon. FCS is integrated under integrator developer environment (IDE), the simulator provides customers with tools to create projects and debug them as they would on silicon (high speed simultaneous transfers). In addition, there is an SC3850 subsystem performance accurate (PACC) simulator that is approximately 95% cycle accurate.
- *Profiler.* The developer can analyze and identify program design inefficiencies.
- *High Speed Run Control*. USB TAP high speed host-target interface allows users to program in Flash memory, ROM, and cache.
- *Host Platform Support*. Microsoft Windows and Solaris.
- *Development Board*. The MSC8156 application development system (ADS) is the development environment for these parts.
- *Kit for MSC8251*. A complete system for developing/debugging real-time hardware and software.

3.2 Application Software

Freescale offers a broad range of DSP applications through its third-party application software partners; these applications target IP telephony, telephony modem, wireless and multimedia transcoding, and wireless base stations. Applications and software modules are listed in **Table 1**.

Table 1. Application Software Modules

Application	Modules
Device Drivers and Example Code	DMA driver, serial RapidIO driver, TDM driver, Ethernet driver, UART driver, security engine, memory allocation, and interrupt handling.
StarCore Libraries	Rich set of StarCore software libraries, including: Math (Part 1 and 2), Signal, Complex vector, Control function, Frequency domain, Filter, Common, Image Processing, Communication, and Matrix.

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