OKI semiconductor

MSM82C88AS/GS

BUS CONTROLLER

GENERAL DESCRIPTION

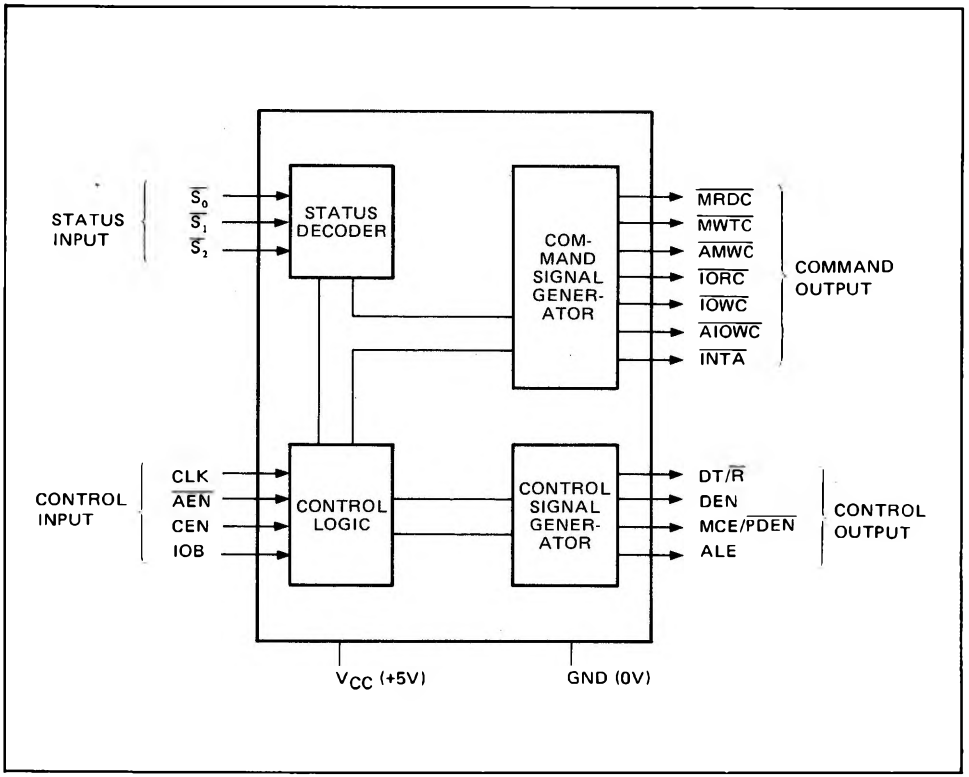
The MSM82C88 is a bus controller for MSM80C86 and MSM80C88 CPU. Based on silicon gate CMOS technology, low-power 16-bit microprocessor system is realized.

The MSM82C88 generates commands control timing signals on reception of status signals from CPU.

FEATURES

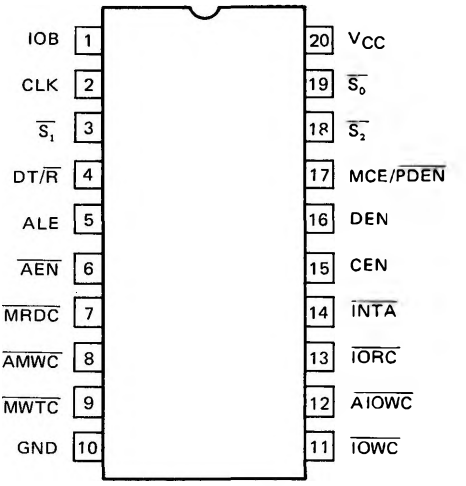
- Silicon gate CMOS technology for low power consumption
- 3 to 6V wide voltage range and single power supply
- –40 to 85°C wide guaranteed operating temperature range
- Advanced write control output
- Three-state command output driver
- System bus mode & I/O bus mode
- 20-pin DIP (MSM82C88AS)
- 24-pin flat package (MSM82C88GS)

CIRCUIT CONFIGURATION

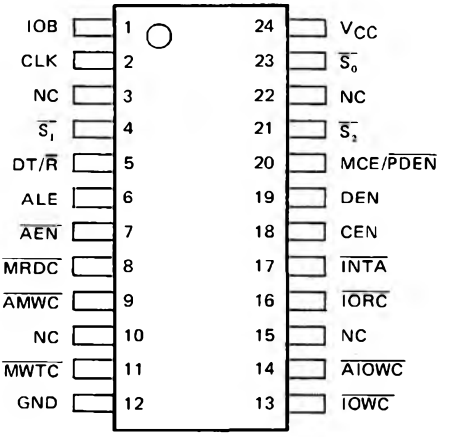


PIN CONFIGURATION

MSM82C88AS (top view)
20-lead DIP



MSM82C88GS (top view)
24-lead plastic flat package



Note: NC pin must not be connected.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits		Unit
			MSM82C88AS	MSM82C88GS	
Power Supply Voltage	V_{CC}	With respect to GND	−0.5 ~ +7		V
Input Voltage	V_{IN}		−0.5 ~ V_{CC} +0.5		V
Output Voltage	V_{OUT}		−0.5 ~ V_{CC} +0.5		V
Storage Temperature	Tstg	—	−55 ~ 150		°C
Power Dissipation	P_D	Ta = 25°C	1.1	0.7	W

OPERATING RANGES

Parameter	Symbol	Limits	Unit
Power Supply Voltage	V_{CC}	3 ~ 6	V
Operating Temperature	T_{OP}	−40 ~ 85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Input Voltage	V_{IL1}	−0.3	—	+0.8	V
"H" Input Voltage	V_{IH1}	3.0	—	V_{CC} +0.3	V
"L" Input Voltage	V_{IL2}	−0.3	—	+0.8	V
"H" Input Voltage	V_{IH2}	2.2	—	V_{CC} +0.3	V

Note: V_{IL1} and V_{IH1} are input voltages for CLK, $\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$.
V_{IL2} and V_{IH2} are input voltages for $\overline{AEN}$, CEN, and IOB.

DC CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, Ta = –40°C to +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
"L" Output Voltage	V_{OL}	Command output I_{OL} = 12mA	–	–	0.45	V	
		Control output I_{OL} = 8mA	–	–	0.45	V	
"H" Output Voltage	V_{OH}	Command output I_{OH} = –5mA	3.7	–	–	V	
		Control output I_{OH} = –1mA	3.7	–	–	V	
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$	–10	–	10	μA	Note 1
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$	–10	–	10	μA	
Status Input Current	I_{LIS}	$0 \leq V_{IN} \leq V_{CC}$	–100	–	10	μA	Note 2
Operation Power Supply Current	I_{CCO}	C_L = 0pF t_{CLCL} = 200ns	–	–	10	mA	
Standby Power Supply Current	I_{CCS}	Note 3	–	–	100	μA	

Note 1. This input leak current is the leak current on input pins except status inputs ($\overline{s_0}$, $\overline{s_1}$, and $\overline{s_2}$).
Note 2. The status input leak current is the leak current at the status inputs ($\overline{s_0}$, $\overline{s_1}$, and $\overline{s_2}$).
Note 3. The measuring conditions for the standby power supply current include the $\overline{s_0}$, $\overline{s_1}$, and $\overline{s_2}$ status inputs being at V_{CC} potential, and the other inputs being at V_{CC} or GND. All output pins are left open.

AC CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, Ta = –40°C to +85°C)

Timing conditions

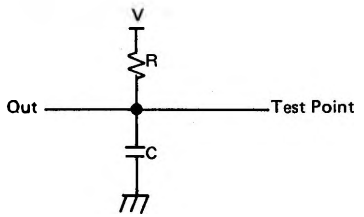
Parameter	Symbol	Min.	Max.	Unit
Clock Cycle	t_{CLCL}	200	–	nS
Clock Low Time	t_{CLCH}	118	–	nS
Clock High Time	t_{CHCL}	65	–	nS
Status Active Setup Time	t_{SVCH}	35	–	nS
Status Inactive Hold Time	t_{CHSV}	10	–	nS
Status Inactive Setup Time	t_{SHCL}	35	–	nS
Status Active Hold Time	t_{CLSH}	10	–	nS

Timing response

Parameter	Symbol	Min.	Max.	Unit	Test Circuit	Remarks
Delay from CLK Leading Edge to DEN, $\overline{PDEN}$ Active	t_{CVNV}	5	45	nS	4	
Delay from CLK Trailing Edge to DEN, $\overline{PDEN}$ Inactive	t_{CVNX}	5	45	nS	4	
Delay from CLK Trailing to ALE Active	t_{CLLH}	–	35	nS	4	
Delay from CLK Trailing Edge to MCE Active	t_{CLMCH}	–	35	nS	4	
Delay from Status Input Falling Edge to ALE Active	t_{SVLH}	–	35	nS	4	
Delay from Status Input Falling Edge to MCE Active	t_{SVMCH}	–	35	nS	4	
Delay from CLK Leading Edge to ALE Inactive	t_{CHLL}	4	35	nS	4	
Delay from CLK Trailing Edge to Command Output Active	t_{CLML}	5	45	nS	3	
Delay from CLK Trailing Edge to Command Output Inactive	t_{CLMH}	5	45	nS	3	
Delay from CLK Leading Edge to DT/$\overline{R}$ Active	t_{CHDTL}	–	50	nS	4	
Delay from CLK Leading Edge to DT/$\overline{R}$ Inactive	t_{CHDTH}	–	35	nS	4	
Delay from $\overline{AEN}$ Leading Edge to Command Enable	t_{AELCH}	–	45	nS	2	
Delay from $\overline{AEN}$ Trailing Edge to Command Disable	t_{AEHCZ}	–	40	nS	1	
Delay from $\overline{AEN}$ Leading Edge to Command Output Active	t_{AELCV}	90	250	nS	3	
Delay from $\overline{AEN}$ to DEN	t_{AEVNV}	–	35	nS	4	
Delay from CEN to DEN, $\overline{PDEN}$	t_{CEVNV}	–	35	nS	4	
Delay from CEN to Command Output	t_{CELRH}	–	$t_{CLML}+20$	nS	3	
Output Rise Time	t_{OLOH}	–	20	nS	3, 4	From 0.8V to 2.2V
Output Fall Time	t_{OHOL}	–	12	nS	3, 4	From 2.2V to 0.8V

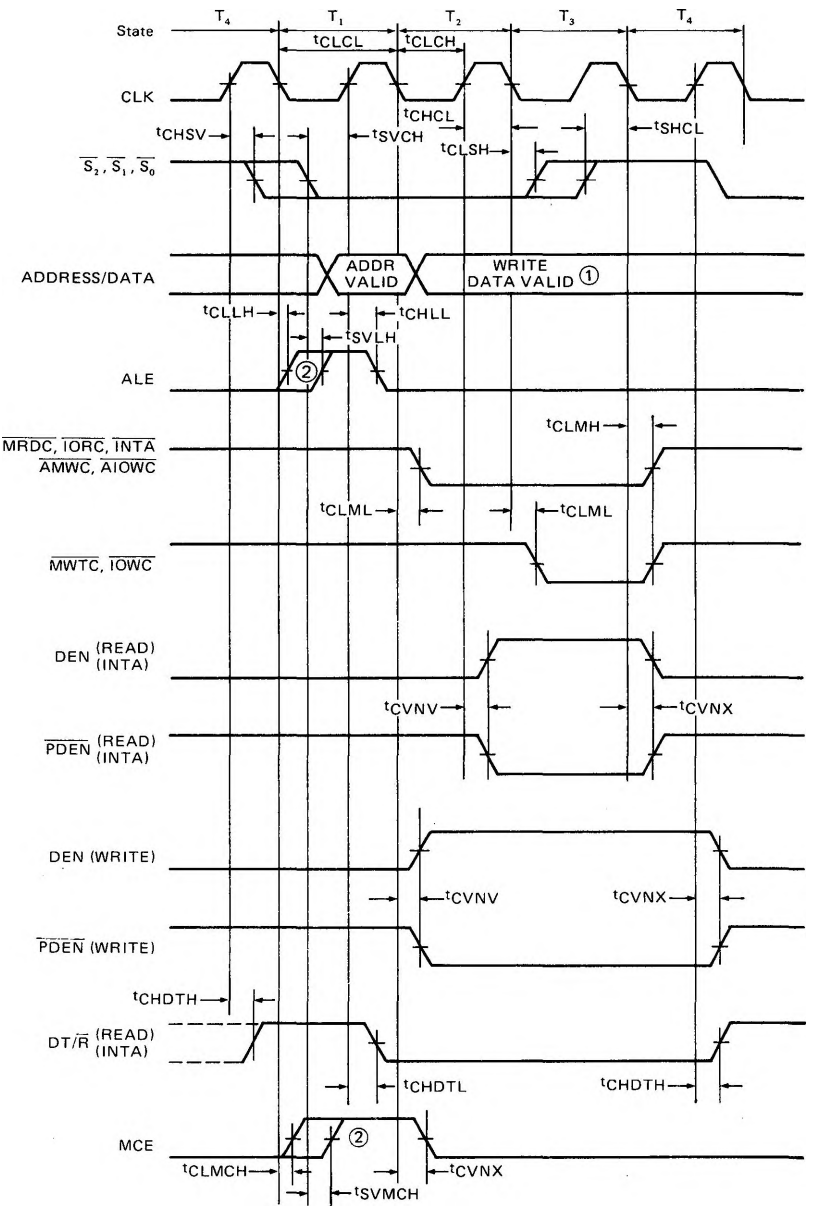
Note: AC timing measurements are made at 1.5V for both logic "1" and "0".
Input rise and fall times are
5 ± 2 nS between 0.8V and 2.2V for $\overline{AEN}$, CEN and IOB.
8 ± 2 nS between 0.8V and 3.0V for $\overline{s_0}$, $\overline{s_1}$, $\overline{s_2}$ and CLK.

Test Circuit



Test Circuit	V(V)	R(Ω)	C(PF)
1	1.5	180	50
2	1.5	300	150
3	2.74	190	150
4	3.34	360	80

TIME CHARTS

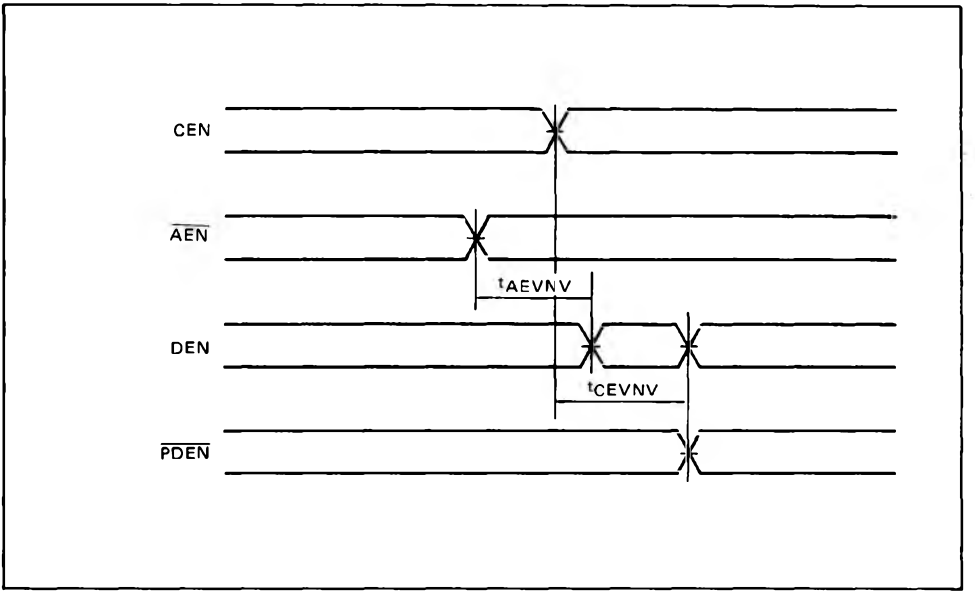


Note 1. The ADDRESS/DATA bus signal is shown for reference purposes.

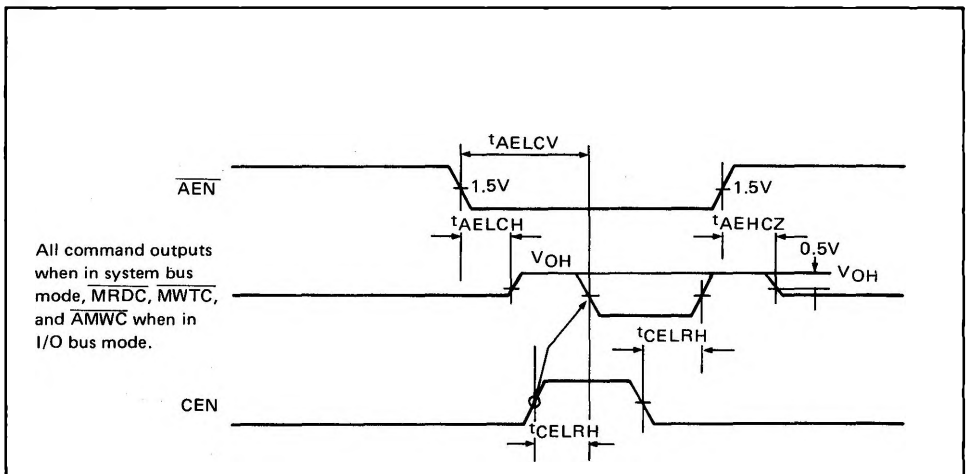
Note 2. The ALE and MCE leading edges are synchronized with the falling edge of CLK or status going active, whichever occurs last.

Note 3. All timing measurements are made at 1.5V unless specified otherwise.

DEN, $\overline{\text{PDEN}}$ Timing



$\overline{\text{AEN}}$ Timing



Note: To control the command and control signal outputs, CEN must be switched to low level before T_2

PIN DESCRIPTION

Pin Name	Input/output	Function
$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$	Input	These pins are input pins for status signals ($\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$), output from the CPU (MSM80C86, 80C88). The MSM82C88 generates commands and control signals after decoding these status signals. And since these pins are connected to internal pull-up resistor, they are set to high level when the CPU status output is at high impedance.
CLK	Input	This pin is input pin for clock signals output from the clock generator (MSM82C84A). The timing of all MSM82C88 output signals is controlled by this clock signal.
ALE	Output	Strobe signal for latching output address from the CPU to address latch. Address latching occurs on the trailing edge of ALE.
DEN	Output	Control signal for setting the data bus transceiver to data enable. The local bus or system bus transceiver is enabled when this signal is high. DEN is switched to low when the CEN input is low.
DT/$\overline{R}$	Output	Control of the direction of data flow in the data bus transceiver. When the CPU is switched to write mode, this signal is high, and when switched to read mode, this signal is low.
$\overline{AEN}$	Input	Address enable signal. • IOB = L (SYSTEM BUS MODE) When the $\overline{AEN}$ input is switched to high level, all command outputs are switched to high impedance status. • IOB = H (I/O BUS MODE) When the $\overline{AEN}$ input is switched to high level, only the $\overline{MRDC}$, $\overline{MWTC}$, and $\overline{AMWC}$ command outputs are switched to high impedance status. When $\overline{AEN}$ is switched from high to low level, high impedance command outputs are not switched to active status (low level) for at least 90 nS, irrespective of the IOB input status.
CEN	Input	Command enable signal. All command outputs, DEN and $\overline{PDEN}$ outputs are switched to inactive status when a low level input is applied to CEN. All command outputs, DEN and $\overline{PDEN}$ outputs are switched to active status when a high level input is applied to CEN.
IOB	Input	I/O bus mode signal. The MSM82C88 is switched to I/O bus mode when a high level input is applied to IOB, and to system bus mode when a low level input is applied.
$\overline{IOWC}$	3-state output	This pin is active-low, and three-state output. This signal is for writing data into the I/O device.
$\overline{AIOWC}$	3-state output	This pin is active-low and three-state output. Although this signal is also used for writing into I/O devices like the I/O write command ($\overline{IOWC}$), it is made active one clock earlier than $\overline{IOWC}$.
$\overline{IORC}$	3-state output	This pin is active-low and three-state output. This signal is for reading data from I/O devices.
$\overline{MWTC}$	3-state output	This pin is active-low and three-state output. This signal is for writing data into memory.
$\overline{AMWC}$	3-state output	This pin is active-low and three-state output. Although this signal is also used for writing into memory like the memory write command ($\overline{MWTC}$), it is made active one cycle earlier than $\overline{MWTC}$.
$\overline{MRDC}$	3-state output	This pin is active-low and three-state output. This signal is for reading data from memory.
$\overline{INTA}$	3-state output	This pin is active-low and three-state output. This signal informs the interrupt controller that the interrupt has been accepted, and then requests output of a vector address onto the data bus.

Pin Name	Input/output	Function
MCE/$\overline{\text{PDEN}}$	Output	This pin has two functions. MCE (IOB = Low) master cascade enable function. This is active-high signal and used to enable a slave PIC (priority interrupt controller) to read the cascade address output on the data bus by the master PIC during an interrupt sequence. $\overline{\text{PDEN}}$ (IOB = High) peripheral data enable function. This is active-low signal and used to enable the data bus transceiver on the I/O bus.

FUNCTION

Command Logic

The command output is decided by decoding status signals ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$) output from the CPU.

These status signals have the following meanings.

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	CPU status	Command output
0	0	0	Interrupt acknowledge	$\overline{\text{INTA}}$
0	0	1	I/O read	$\overline{\text{IORC}}$
0	1	0	I/O write	$\overline{\text{IOWC}}$, $\overline{\text{AIOWC}}$
0	1	1	Halt	–
1	0	0	Instruction fetch	$\overline{\text{MRDC}}$
1	0	1	Memory read	$\overline{\text{MRDC}}$
1	1	0	Memory write	$\overline{\text{MWTC}}$, $\overline{\text{AMWC}}$
1	1	1	Passive	–

I/O Bus Mode (IOB = High)

When an I/O access status signal is received from the CPU in I/O bus mode, one of the I/O commands ($\overline{\text{IORC}}$, $\overline{\text{IOWC}}$, $\overline{\text{AIOWC}}$, $\overline{\text{INTA}}$) corresponding to the status signal becomes active irrespective of the $\overline{\text{AEN}}$ status. At the same time, the $\overline{\text{PDEN}}$ and DT/$\overline{\text{R}}$ outputs which control the data bus transceiver are generated.

As in system bus mode, the memory commands ($\overline{\text{MRDC}}$, $\overline{\text{MWTC}}$, and $\overline{\text{AMWC}}$) are not switched to low level for at least 90 ns after $\overline{\text{AEN}}$ is switched to low level.

System Bus Mode (IOB = Low)

When the bus is usable, MSM82C88 is enabled by the $\overline{\text{AEN}}$ signal from the bus arbiter. Consequently, no command output becomes active unless the $\overline{\text{AEN}}$ signal becomes low. Also note that there is a delay of at least 90 ns before any command output becomes active after the $\overline{\text{AEN}}$ signal is switched to low level.

System bus mode is used when more than one CPU is connected to a single bus, and the bus I/O, memory, etc. are used in common.

Command Outputs

The advanced write commands ($\overline{\text{AIOWC}}$ and $\overline{\text{AMWC}}$) become active one cycle earlier than normal write commands ($\overline{\text{IOWC}}$ and $\overline{\text{MWTC}}$). This prevents the CPU from being switched to an additional period of wait status.

$\overline{\text{INTA}}$ (interrupt acknowledge) is output during the interrupt acknowledge cycle in the same way as $\overline{\text{MRDC}}$ in the read cycle. The purpose of this signal is to inform the device which has requested the interrupt that the interrupt has been accepted, and requests a vector address output on the data bus.

$\overline{\text{MRDC}}$ – Memory read command
$\overline{\text{MWTC}}$ – Memory write command
$\overline{\text{IORC}}$ – I/O read command
$\overline{\text{IOWC}}$ – I/O write command
$\overline{\text{AMWC}}$ – Advanced memory write command
$\overline{\text{AIOWC}}$ – Advanced I/O write command
$\overline{\text{INTA}}$ – Interrupt acknowledge

Control Output

The control output signals are DEN (Data Enable), DT/$\overline{\text{R}}$ (Transmit/Receive), and MCE/$\overline{\text{PDEN}}$ (Master Cascade Enable/Peripheral Data Enable).

DEN signal enables the local bus or system bus, when it is high.

The DT/$\overline{\text{R}}$ signal determines the direction of the data on the local bus or system bus.

The function of the MCE/$\overline{\text{PDEN}}$ pin is switched according to IOB. The $\overline{\text{PDEN}}$ function is selected in I/O bus mode (IOB = high) to provide the I/O or peripheral/system bus data enable signal. When the MCE function is selected in system bus mode (IOB = low), the MCE signal is active (high) level at an interrupt acknowledge status.

The MCE signal is used when a master and slave interrupt controller exists in the system.

ALE (Address Latch Enable)

ALE is generated in each machine cycle to latch the current address to the address latch.

CEN (Command Enable)

This signal is used to enable command outputs. All command outputs become inactive if a low level input is applied to the CEN pin.