OKI semiconductor

MSM83C55-XXRS/GS

2048 x 8 BIT MASK ROM WITH I/O PORTS

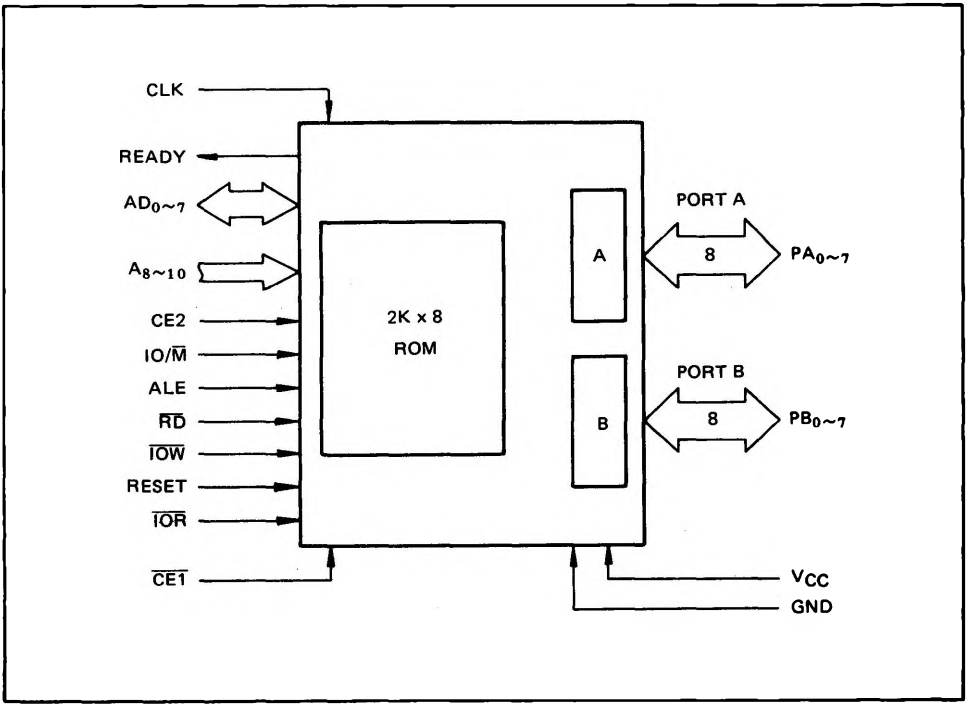
GENERAL DESCRIPTION

MSM83C55 is a combination of MROM and I/O devices used in a microcomputer system. Owing to the adoption of the CMOS silicon gate technology, it operates on a low power supply as small as 100 μA (max.) in the standby current in the chip non-select status. As the ROM is composed of 2048 words x 8 bits and its access time (max.) is 400 ns, it can be applied without using the wait state in the 80C85A system, too. The I/O circuit is composed of 2 universal I/O ports. Each of these I/O ports has 8 port lines and each of these port lines can be programmed as input or output line independently.

FEATURES

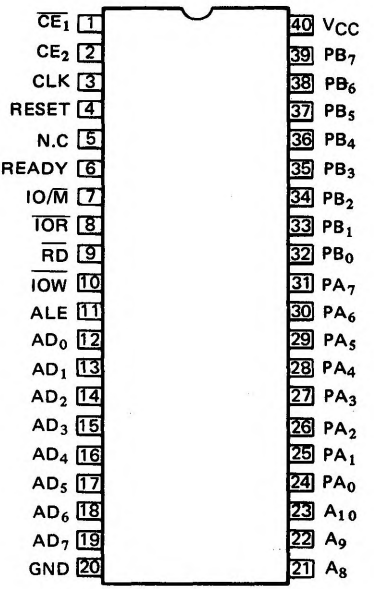
- High speed and low power consumption owing to adoption of silicon gate CMOS
- Composed of 2048 words x 8 bits
- 3 ~ 6 V single power supply
- Address latch circuit incorporated
- Provided with 2 universal 8-bit I/O ports
- TTL Compatible
- Indivisual I/O port line programmable as input or output
- Time division address/data bus
- 40-pin DIP (MSM83C55-xxRS)
- 44-pin flat package (MSM83C55-xxGS)
- Direct interface with MSM80C85A (3MHz)

CIRCUIT CONFIGURATION

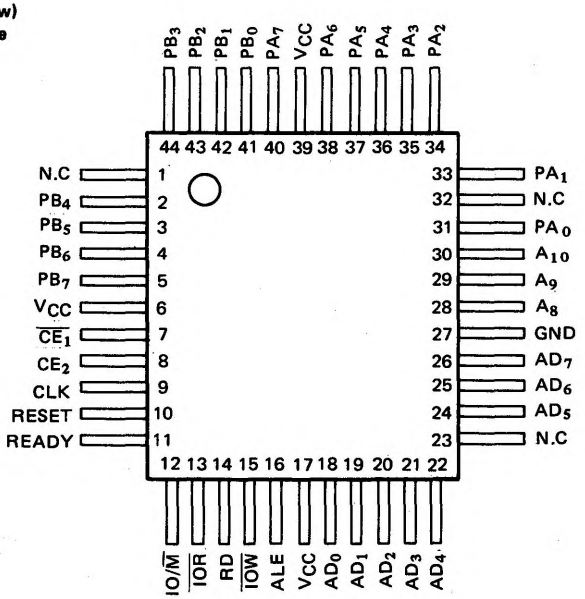


PIN CONFIGURATION

MSM83C55-xxRS (Top View)
40 Lead Plastic DIP



MSM83C55-xxGS (Top View)
44 Lead Plastic Flat Package



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits		Unit
			MSM83C55RS	MSM83C55GS	
Supply Voltage	V_{CC}	With respect to GND	-0.5 to +7		V
Input Voltage	V_{IN}		-0.5 to V_{CC} +0.5		V
Output Voltage	V_{OUT}		-0.5 to V_{CC} +0.5		V
Storage Temperature	Tstg		-55 to +150		°C
Power Dissipation	P_D	Ta=25°C	1.0	0.7	W

OPERATING RANGE

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	3 to 6	V
Operating Temperature	T_{OP}	-40 to +85	°C

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	-40	+25	+85	°C
"L" Input Voltage	V_{IL}	-0.3		+0.8	V
"H" Input Voltage	V_{IH}	2.2		V_{CC} +0.3	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
"L" Output Voltage	V_{OL}	I_{OL}=2mA	V_{CC}=4.5V to 5.5V Ta=-40°C to +85°C			0.45	V
"H" Output Voltage	V_{OH}	I_{OH}=-400μA		2.4			V
		I_{OH}=-40μA		4.2			V
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$		-10		10	μA
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$		-10		10	μA
Supply Current (standby)	I_{CCS}	$\overline{CE1} \geq V_{CC}$-0.2V CE2≦0.2V $V_{IH} \geq V_{CC}$-0.2V $V_{IL} \leqq$0.2V			0.1	100	μA
Average Supply Current (active)	I_{CC}	IO write cycle time: 1 μs				5	mA

AC CHARACTERISTICS

(V_{CC}=4.5V to 5.5V, Ta=-40°C to +85°C)

Parameter	Symbol	Min.	Max.	Unit
Clock Cycle Time	t_{CYC}	320		ns
Clock Pulse Width	T_1	80		ns
Clock Pulse Width	T_2	120		ns
Clock Rise and Fall Time	t_f, t_r		30	ns
Address to Latch Setup Time	t_{AL}	50		ns
Address Hold Time after Latch	t_{LA}	30		ns
Latch to READ/WRITE Control	t_{LC}	100		ns
Valid Data Out Delay from READ Control	t_{RD}		170	ns
Address Stable to Data Out Valid	t_{AD}		400	ns
Latch Enable Width	t_{LL}	100		ns
Data Bus Float after READ	t_{RDF}	0	100	ns
READ/WRITE Control to Latch Enable	t_{CL}	20		ns
READ/WRITE Control Width	t_{CC}	250		ns
Data In to WRITE Setup Time	t_{DW}	150		ns
Data In Hold Time after WRITE	t_{WD}	10		ns
WRITE to Port Output	t_{WP}		400	ns
Port Input Setup Time	t_{PR}	50		ns
Port Input Hold Time	t_{RP}	50		ns
READY Hold Time	t_{PYH}	0	160	ns
Address to READY	t_{ARY}		160	ns
Recovery Time between Controls	t_{RV}	300		ns
Data Out Delay from READ Control	t_{RDE}	10		ns
ALE to Data Out Valid	t_{LD}		350	ns

Note: Timing is measured at V_L = 0.8 V and V_H = 2.2 V for both input and output
Load condition: C_L = 150 pF

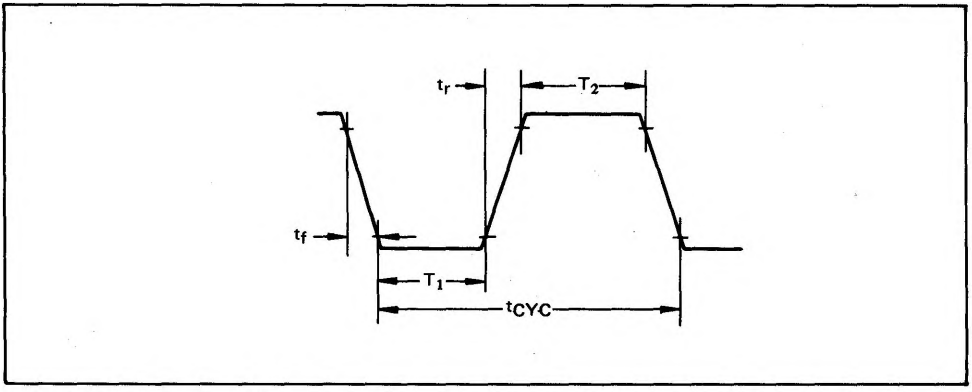


Fig. 1 Clock Signal for MSM83C55

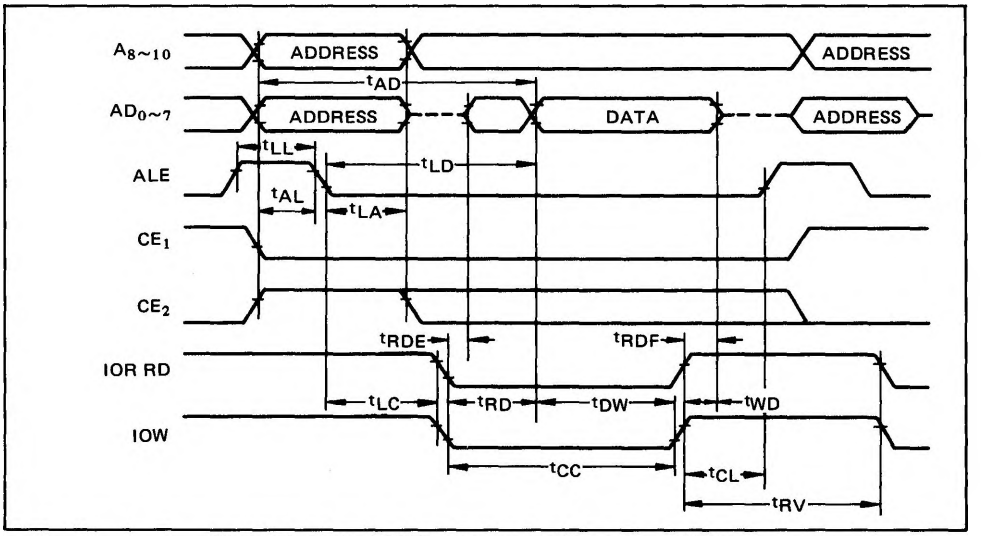


Fig. 2 Timing for ROM Reading and for I/O Reading and Writing

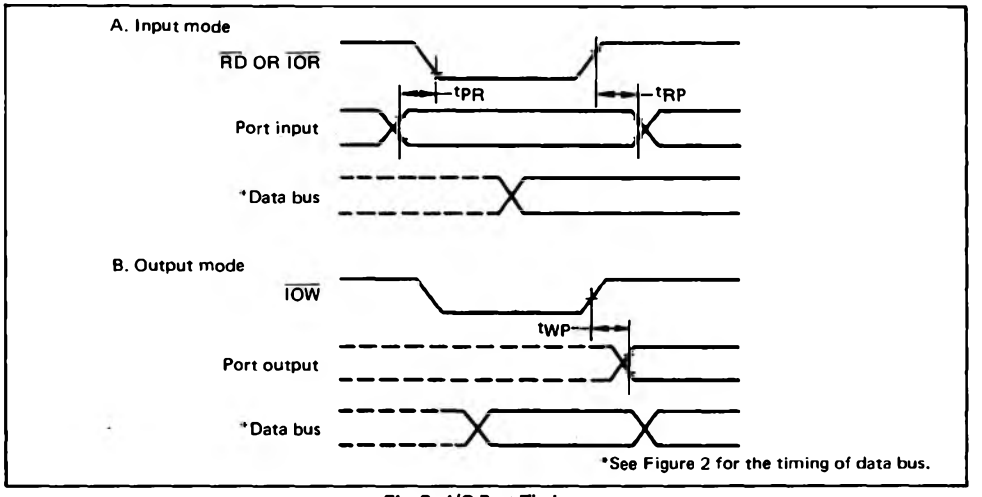


Fig. 3 I/O Port Timing

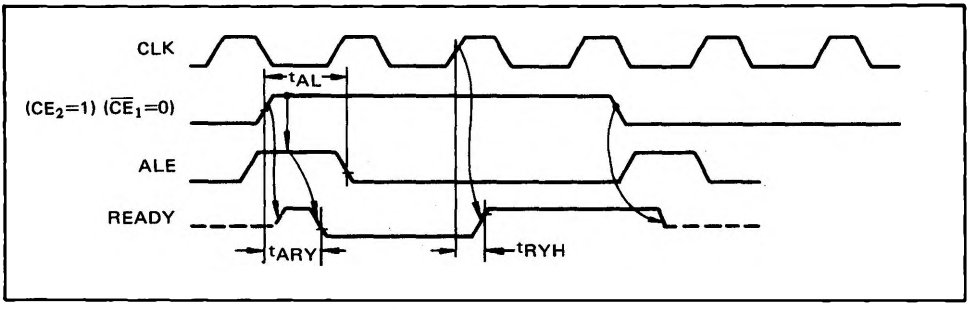


Fig. 4 Wait State Timing (READY = 0)

PIN DESCRIPTION

Pin symbol	Function
RESET	When this signal becomes high level, ports A and B becomes the input mode.
ALE	This pin is used to fetch the AD 0~7, A 8~10, IO/$\overline{M}$, $\overline{CE1}$, and CE2 signals to their respective latch circuits at the fall of the ALE (Address Latch Enable) signal.
$\overline{CE1}$, CE2	When $\overline{CE1}$ fetched to the latch circuit is high level or CE2 is low level, no read nor write operation is performed. The AD 0~7 and READY output signals are made into the floating status.
AD0~7	Three-stake bidirectional address/data bus. This bus fetch 8-bit address information to the latch circuit upon the fall of the ALE signal. When $\overline{CE1}$ in holding is low level and yet CE2 is high level, data is output from chip to bus if RD or IOR is low level and it is fetched from bus to chip if $\overline{IOW}$ is low level.
A8~10	These are high order bits of ROM address and have no relation to I/O operation.
IO/$\overline{M}$	When $\overline{RD}$ is low level, this pin selects I/O port if the IO/$\overline{M}$ in holding is high level or ROM if it is low level.
$\overline{RD}$	If the $\overline{RD}$ is low level, the memory data is output to AD 0~7 when the ROM cycle is selected, but the selected port data is output to the same when the I/O cycle is selected.
$\overline{IOR}$	The port data selected at low level is output to AD 0~7. When turned to the low level, the $\overline{IOR}$ becomes the same function as that when IO/$\overline{M}$ is turned to the high level and $\overline{RD}$ to the low level. When both $\overline{RD}$ and $\overline{IOR}$ become high level, the output of AD 0~7 is made into the floating state.
$\overline{IOW}$	At the low level, the AD 0~7 data is written to the selected port.
CLK	This signal is used to generate the READY signal for the generation of 1 wait cycle built in 83C55.
READY	This signal becomes low level when the ALE is high level and the $\overline{CE1}$ and CE2 are active. It becomes high level at the rise of CLK after the fall of the ALE.
PA0~7	These are universal I/O pins and the input/output is determined by the content of the data direction register. When writing data to port A, make the chip enable active and turn the $\overline{IOW}$ to low level after selecting AD 0, 1 to 0, 0. When reading it, turn the $\overline{IOR}$ to low level instead of $\overline{IOW}$ and IO/$\overline{M}$ to high level.
PB0~7	Same as the operation of PA0~7, excepting that AD0 is selected to 1 and AD1 to 0.
V_{CC}	+5 V power supply
GND	0 V

OPERATIONAL DESCRIPTION

ROM Block

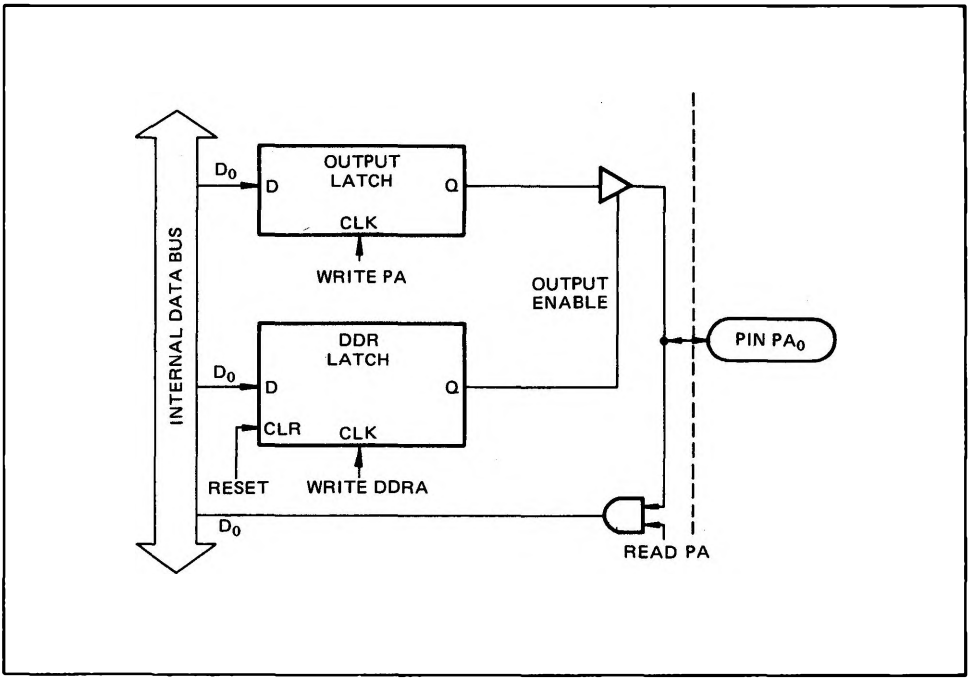
The ROM block in the chip is specified in address by the chip enable and 11-bit address. Upon the fall of the ALE signal, the address and chip enable are fetched in the address latch circuit. When the chip enable is active and IO/$\overline{M}$ is low level, 8-bit content of ROM at the address held in the address latch circuit is transmitted to the bus through the output buffer of AD 0~7 upon the fall of the $\overline{RD}$.

I/O Block

The I/O block in the chip is specified in address by the value of 2-bits of AD 0~1 and chip enable. Two 8-bit data direction registers (DDR) built in MSM83C55 are used to turn corresponding individual port pins to the input mode or output mode. It becomes the input mode when set to 0 and the output mode when set to 1. It is impossible to read the DDR from outside, however.

AD_1	AD_0	Selection
0	0	Port A
0	1	Port B
1	0	Port A data direction register (DDRA)
1	1	Port B data direction register (DDRB)

Upon the fall of $\overline{IOW}$ when the chip enable is active, the AD 0~7 data is written to the I/O port to be determined by the value of AD 0~1 in holding. During this operation, selected side I/O bits are all subject to its influence irrespective of the I/O status and IO/M status. The output level remains unchanged until the $\overline{IOW}$ returns to high level. The data can be read from ports when the chip enable in holding is active and IO/M is high level and yet the $\overline{RD}$ or $\overline{IOR}$ signal falls. In both input and output, the data on the selected side exists on the line of AD 0~7. The function of I/O ports and DDR (data direction register) is shown in the block diagram below:



Writing "0" to the DDR is equivalent to the RESET operation when the port output is made into the High impedance status and the input mode is specified. Note that the data can be written to the ports even if the output pin was already in the high impedance status (input mode) by the DDR. Likewise, it is also possible to read the data once set to those ports.