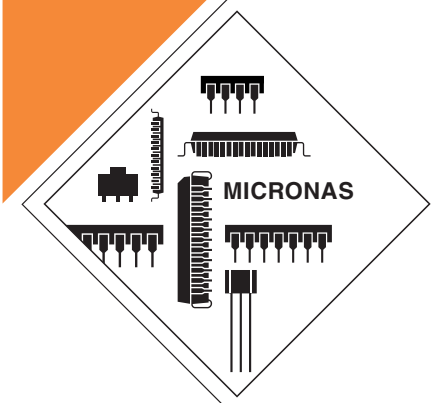


DATA SHEET

MSP 44x8G
Multistandard
Sound Processor Family

Edition June 16, 2003
6251-516-1DS

MICRONAS

Contents

Contents, continued

Contents, continued

Multistandard Sound Processor Family

Release Note: Revision bars indicate significant changes to the previous edition. The hardware and software description in this document is valid for the MSP 44x8G version B3 and following versions.

1. Introduction

The MSP 44x8G family of Multistandard Sound Processors cover the demodulation and stereo decoding of all analog TV-Standards worldwide, as well as the NICAM digital sound standards and FM stereo radio. The full demodulation and decoding, starting with analog sound IF signal in, down to processed analog or digital AF (baseband audio) out, is performed on a single chip. Fig. 1–1 shows a simplified functional block diagram of the MSP 44x8G.

The MSP 44x8G built-in stereo A/D converters offer a S/N ratio of 95 dBA typ. The double stereo D/A converters with analog volume and 0.125 dB steps make use of the Micronas unique multibit Delta-Sigma technology, offering a dynamic range of 95 dBA typically. The DSP processing is performed at a 48 kHz sample rate, maintaining the full audio bandwidth of 20 kHz in all MSP 44x8G signal paths.

The MSP 44x8G has been designed for the usage in hybrid set-top boxes and multimedia applications. It combines the function of a TV stereo decoder together with an Audio I^2S Codec and DSP audio processing features. Its asynchronous I^2S slave interface allows the reception of digital stereo signals with arbitrary sample rates from 5 to 50 kHz. Synchronization is performed by means of a high-quality adaptive sample rate converter. All I^2S input signals are upsampled to 48 kHz.

The MSP 44x8G offers the following automatic functions:

– ASD (Automatic Standard Detection) detects the actual broadcasted TV standard automatically.

– ASS (Automatic Sound Select) switches automatically (without any I2C action) between mono/stereo/bilingual when the broadcast mode changes.

This generation of TV sound processing ICs includes versions for processing the multichannel television sound (MTS) signal conforming to the U.S. standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, Micronas Noise Reduction (MNR) is performed alignment free. Apart from all 2-carrier standards, other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard.

The MSP 44x8G versions are pin and software compatible to other MSP families. Standard selection requires only a single I^2C transmission.

The ICs are produced in submicron CMOS technology and are available in the following packages: PMQFP80-11, PMQFP64-2, and PSDIP64-1.

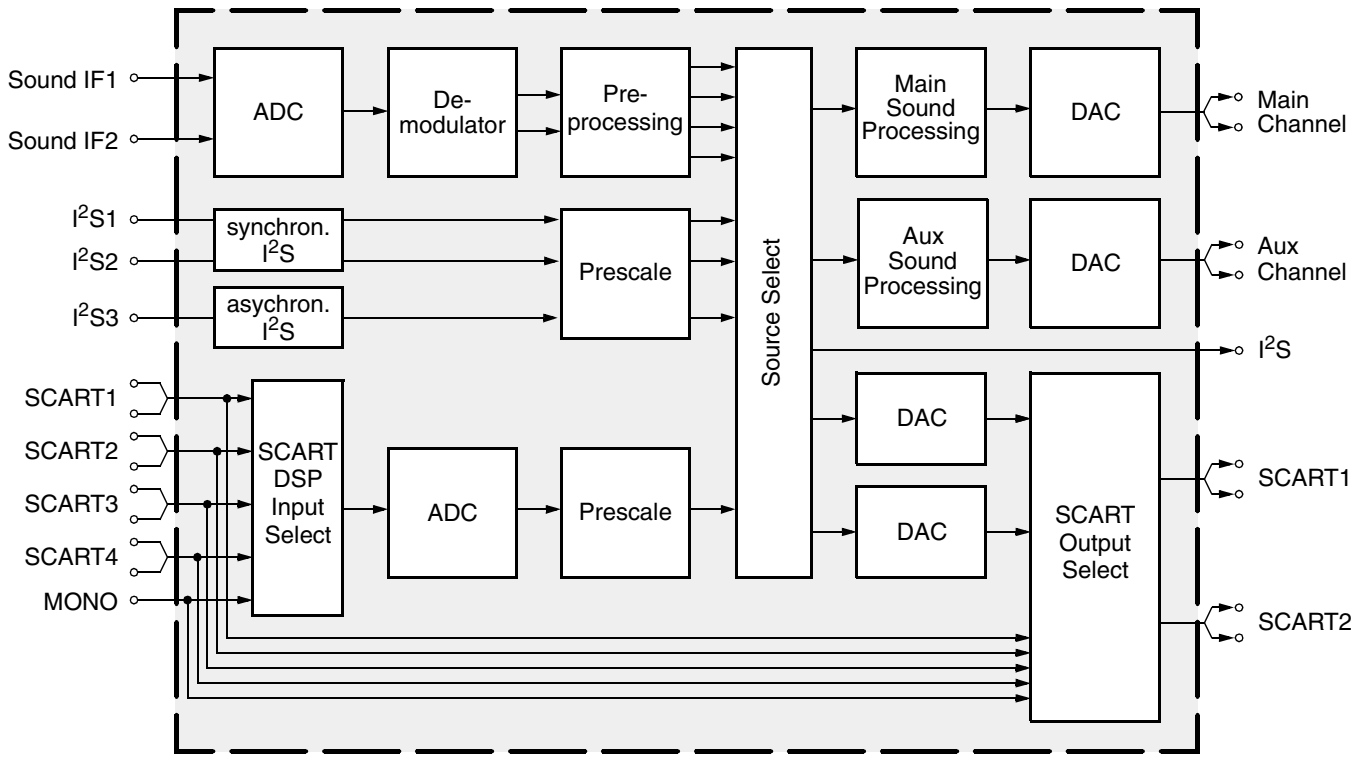


Fig. 1–1: Simplified functional block diagram of the MSP 44x8G

1.1. Features of the MSP 44x8G Family

Feature	4408	4418	4428	4448	4458	4468
Standard Selection with single I^2C transmission	X	X	X	X	X	X
Automatic Standard Detection of terrestrial TV standards	X	X	X	X	X	X
Automatic Sound Selection (mono/stereo/bilingual), new registers MODUS, STATUS	X	X	X	X	X	X
Two selectable sound IF (SIF) inputs	X	X	X	X	X	X
Automatic Carrier Mute function	X	X	X	X	X	X
Interrupt output programmable (indicating status change)	X	X	X	X	X	X
Main/Aux channel with volume	X	X	X	X	X	X
AVC: Automatic Volume Correction	X	X	X	X	X	X
Two channel mixer	X	X	X	X	X	X
Selectable preemphasis for Aux channel	X	X	X	X	X	X
Four Stereo SCART (line) inputs, one Mono input; two Stereo SCART outputs	X	X	X	X	X	X
Complete SCART in/out switching matrix	X	X	X	X	X	X
Two 48kHz I^2S inputs; one ansynchronous 5..50 kHz I^2S input, one 48 kHz I^2S output	X	X	X	X	X	X
All analog Mono Sound carriers including AM-SECAM	X	X	X	X	X	X
Korean FM-Stereo A2 standard	X	X	X	X	X	
All analog FM-Stereo A2 and satellite standards	X	X			X	
Simultaneous demodulation of (very) high-deviation FM-Mono and NICAM		X			X	
Adaptive deemphasis for satellite (Wegener-Panda, acc. to ASTRA specification)	X	X			X	X
ASTRA Digital Radio (ADR) together with DRP 3510A	X	X			X	X
All NICAM standards		X			X	
Demodulation of the BTSC multiplex signal and the SAP channel			X	X	X	
Alignment free digital DBX noise reduction for BTSC Stereo and SAP				X	X	
Alignment free digital Micronas Noise Reduction (MNR) for BTSC Stereo and SAP			X			
BTSC stereo and EIA-J separation significantly better than spec.			X	X	X	
SAP and stereo detection for BTSC system			X	X	X	
Alignment-free Japanese standard EIA-J			X	X	X	
Demodulation of the FM-Radio multiplex signal			X	X	X	

1.2. MSP 44x8G Version List

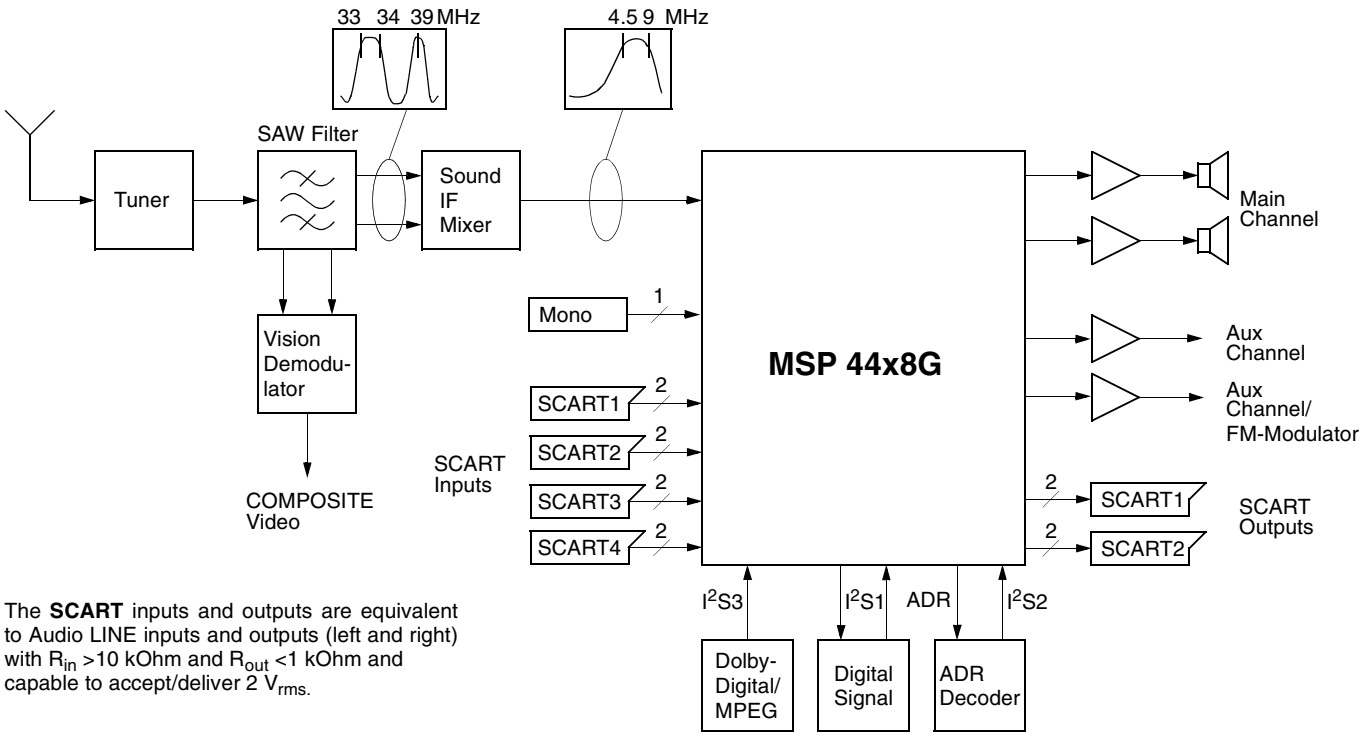
Version	Status	Description
MSP 4408G	not confirmed	FM Stereo (A2) Version
MSP 4418G	available	NICAM and FM Stereo (A2) Version
MSP 4428G	available	NTSC Version (A2 Korea, BTSC with Micronas Noise Reduction (MNR), and Japanese EIA-J system)
MSP 4448G	available	NTSC Version (A2 Korea, BTSC with DBX noise reduction, and Japanese EIA-J system)
MSP 4458G	available	Global Version (all sound standards)
MSP 4468G	not confirmed	Global Mono Version (all sound standards)

1.3. MSP 44x8G Versions and their Application Fields

Table 1–1 provides an overview of TV sound standards that can be processed by the MSP 44x8G family. In addition, the MSP 44x8G is able to handle the terrestrial FM-Radio standard. With the MSP 44x8G, a complete multimedia receiver covering all TV sound standards together with terrestrial and satellite radio sound can be built; even ASTRA Digital Radio can be processed (with a DRP 3510A coprocessor).

Table 1–1: TV Stereo Sound Standards covered by the MSP 44x8G Family (details see Appendix A)

MSP Version	System	Position of Sound Carrier / MHz	Sound Modulation	Color System	Broadcast e.g. in:
4408 4418 4458	B/G	5.5/5.7421875	FM-Stereo (A2)	PAL	Germany
		5.5/5.85	FM-Mono/NICAM	PAL	Scandinavia, Spain
	L	6.5/5.85	AM-Mono/NICAM	SECAM-L	France
	I	6.0/6.552	FM-Mono/NICAM	PAL	UK, Hong Kong
4408 4418 4458	D/K	6.5/5.85	FM-Mono/NICAM	PAL	China, Hungary
		6.5/6.2578125	FM-Stereo (A2, D/K1)	SECAM-East	Slovak. Rep.
		6.5/6.7421875	FM-Stereo (A2, D/K2)	PAL	currently no broadcast
		6.5/5.7421875	FM-Stereo (A2, D/K3)	SECAM-East	Poland
	Satellite	6.5 7.02/7.2 7.38/7.56 etc.	FM-Mono FM-Stereo ASTRA Digital Radio (ADR) with DRP 3510A	PAL	Europe Sat. ASTRA
4418 4428/48 4458	M	4.5/4.724212	FM-Stereo (A2)	NTSC	Korea
		4.5	FM-FM (EIA-J)	NTSC	Japan
		4.5	BTSC-Stereo + SAP	NTSC	USA
	FM-Radio	10.7	FM-Stereo Radio		USA, Europe
4468	all Standards as above but Mono demodulation only				



The **SCART** inputs and outputs are equivalent to Audio LINE inputs and outputs (left and right) with R_{in} >10 kOhm and R_{out} <1 kOhm and capable to accept/deliver 2 V_{rms}.

Fig. 1–2: Typical MSP 44x8G application

2. Functional Description

Note: The **SCART** inputs and outputs are equivalent to Audio LINE inputs and outputs (left and right) with R_{in} >10 kOhm and R_{out} <1 kOhm and capable to accept/deliver 2 V_{rms}.

Note: [1] AVC location is programmable.

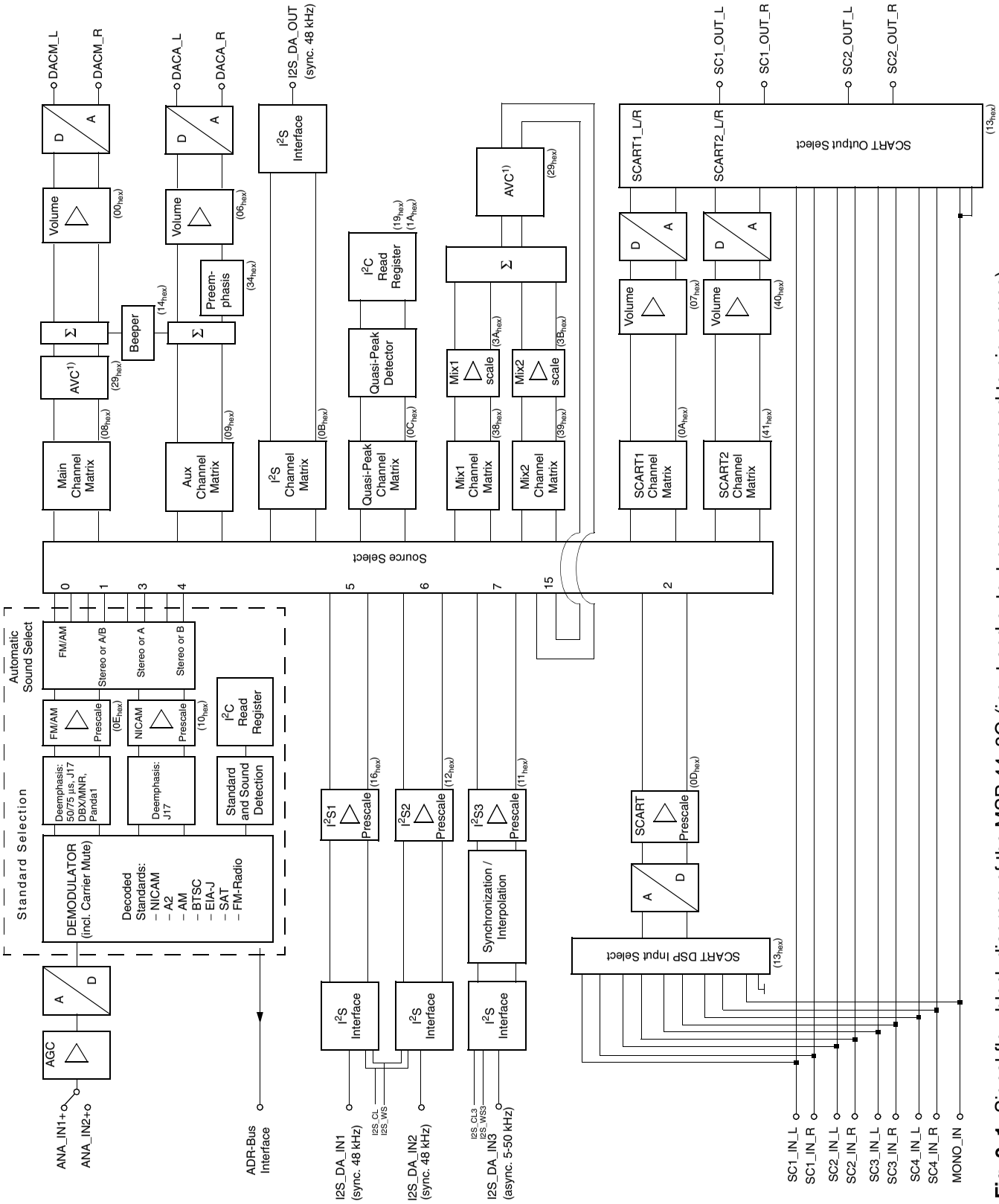


Fig. 2–1: Signal flow block diagram of the MSP 44x8G (input and output names correspond to pin names).

2.1. Architecture of the MSP 44x8G Family

Fig. 2–1 shows a simplified block diagram of the IC. The block diagram contains all features of the MSP 4458G. Other members of the MSP 44x8G family do not have the complete set of features: The demodulator handles only a subset of the standards presented in the demodulator block; NICAM processing is only possible in the MSP 4418G and MSP 4458G.

2.2. MSP 44x8G Sound IF Processing

2.2.1. Analog Sound IF Input

The input pins ANA_IN1+, ANA_IN2+, and ANA_IN– offer the possibility to connect two different sound IF (SIF) sources to the MSP 44x8G. The preselected sound IF signal is fed into an A/D-converter. An analog automatic gain circuit (AGC) allows a wide range of input levels. The highpass filters, formed by the coupling capacitors at pins ANA_IN1+ and ANA_IN2+ (see Section 7.3. “Application Circuit” on page 87), are sufficient in most cases to suppress video components. Some combinations of SAW filters and sound IF mixer ICs, however, show large picture components on their outputs. In this case, further filtering is recommended.

2.2.2. Demodulator: Standards and Features

The MSP 44x8G is able to demodulate all TV-sound standards worldwide including the digital NICAM system. Depending on the MSP 44x8G version, the following demodulation modes can be performed:

A2 Systems: Detection and demodulation of two separate FM carriers (FM1 and FM2), demodulation and evaluation of the identification signal of carrier FM2.

NICAM Systems: (Only possible in the MSP 4418G and MSP 4458G). Demodulation and decoding of the NICAM carrier, detection and demodulation of the analog FM or AM carrier. For D/K-NICAM, the FM carrier may have a maximum deviation of 384 kHz.

Very high deviation FM-Mono: Detection and robust demodulation of one FM carrier with a maximum deviation of 540 kHz.

BTSC-Stereo: Detection and FM demodulation of the aural carrier resulting in the MTS/MPX signal. Detection and evaluation of the pilot carrier, AM demodulation of the (L–R)-carrier and detection of the SAP subcarrier. Processing of DBX noise reduction or Micronas Noise Reduction (MNR).

BTSC-Mono + SAP: Detection and FM demodulation of the aural carrier resulting in the MTS/MPX signal. Detection and evaluation of the pilot carrier, detection and FM demodulation of the SAP subcarrier. Processing of DBX noise reduction or Micronas Noise Reduction (MNR).

Japan Stereo: Detection and FM demodulation of the aural carrier resulting in the MPX signal. Demodulation and evaluation of the identification signal and FM demodulation of the (L–R)-carrier.

FM-Satellite Sound: Demodulation of one or two FM carriers. Processing of high-deviation mono or narrow bandwidth mono, stereo, or bilingual satellite sound according to the ASTRA specification.

FM-Stereo-Radio: Detection and FM demodulation of the aural carrier resulting in the MPX signal. Detection and evaluation of the pilot carrier and AM demodulation of the (L–R)-carrier.

The demodulator blocks of all MSP 44x8G versions have identical user interfaces. Even completely different systems like the BTSC and NICAM systems are controlled the same way. Standards are selected by means of MSP Standard Codes. Automatic processes handle standard detection and identification without controller interaction. The key features of the MSP 44x8G demodulator blocks are

Standard Selection: The controlling of the demodulator is minimized: All parameters, such as tuning frequencies or filter bandwidth, are adjusted automatically by transmitting one single value to the STANDARD SELECT register. For all standards, specific MSP standard codes are defined.

Automatic Standard Detection: If the TV sound standard is unknown, the MSP 44x8G can automatically detect the actual standard, switch to that standard, and respond the actual MSP standard code.

Automatic Carrier Mute: To prevent noise effects or FM identification problems in the absence of an FM carrier, the MSP 44x8G offers a configurable carrier mute feature, which is activated automatically if the TV sound standard is selected by means of the STANDARD SELECT register. If no FM carrier is detected at one of the two MSP demodulator channels, the corresponding demodulator output is muted. This is indicated in the STATUS register.

2.2.3. Preprocessing of Demodulator Signals

The NICAM signals must be processed by a deemphasis filter and adjusted in level. The analog demodulated signals must be processed by a deemphasis filter, adjusted in level, and dematrixed. The correct deemphasis filters are already selected by setting the standard in the STANDARD SELECT register. The level adjustment has to be done by means of the FM/AM and NICAM prescale registers. The necessary dematrix function depends on the selected sound standard and the actual broadcasted sound mode (mono, stereo, or bilingual). It can be manually set by the FM Matrix Mode register or automatically by the Automatic Sound Selection.

2.2.4. Automatic Sound Select

In the Automatic Sound Select mode, the dematrix function is automatically selected based on the identification information in the STATUS register. No I^2C interaction is necessary when the broadcasted sound mode changes (e.g. from mono to stereo).

The demodulator supports the identification check by switching between mono compatible standards (standards that have the same FM mono carrier) automatically and non-audible. If B/G-FM or B/G-NICAM is selected, the MSP will switch between these standards. The same action is performed for the standards: D/K1-FM, D/K2-FM, D/K3-FM, and D/K-NICAM. Switching is only done in the absence of any stereo or bilingual identification. If identification is found, the MSP keeps the detected standard.

In case of high bit-error rates, the MSP 44x8G automatically falls back from digital NICAM sound to analog FM or AM mono.

Table 2–1 summarizes all actions that take place when Automatic Sound Select is switched on.

To provide more flexibility, the Automatic Sound Select block prepares four different source channels of demodulated sound (Fig. 2–2). By choosing one of the four demodulator channels, the preferred sound mode can be selected for each of the output channels (loudspeaker, headphone, etc.). This is done by means of the Source Select registers.

The following source channels of demodulated sound are defined:

– **“FM/AM” channel:** Analog mono sound, stereo if available. In case of NICAM, analog mono only (FM or AM mono).

– **“Stereo or A/B” channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains both languages A (left) and B (right).

– **“Stereo or A” channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains language A (on left and right).

– **“Stereo or B” channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains language B (on left and right).

Fig. 2–2 and Table 2–2 show the source channel assignment of the demodulated signals in case of Automatic Sound Select mode for all sound standards.

Note: The analog primary input channel contains the signal of the mono FM/AM carrier or the L+R signal of the MPX carrier. The secondary input channel contains the signal of the second FM carrier, the L–R signal of the MPX carrier, or the SAP signal.

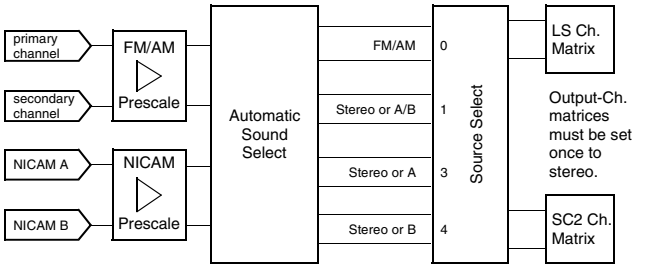


Fig. 2–2: Source channel assignment of demodulated signals in Automatic Sound Select Mode

2.2.5. Manual Mode

Fig. 2–3 shows the source channel assignment of demodulated signals in case of manual mode. If manual mode is required, more information can be found in Section 6.7. “Demodulator Source Channels in Manual Mode” on page 84.

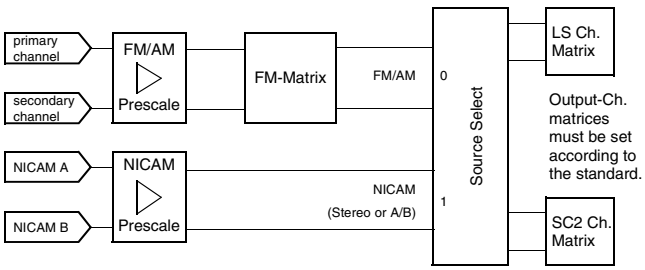


Fig. 2–3: Source channel assignment of demodulated signals in Manual Mode

Table 2–1: Performed actions of the Automatic Sound Selection

Selected TV Sound Standard	Performed Actions
B/G-FM, D/K-FM, M-Korea, and M-Japan	Evaluation of the identification signal and automatic switching to mono, stereo, or bilingual. Preparing four demodulator source channels according to Table 2–2.
B/G-NICAM, L-NICAM, I-NICAM, D/K-NICAM	Evaluation of NICAM-C-bits and automatic switching to mono, stereo, or bilingual. Preparing four demodulator source channels according to Table 2–2.
	In case of bad or no NICAM reception, the MSP switches automatically to FM/AM mono and switches back to NICAM if possible. A hysteresis prevents periodical switching.
B/G-FM, B/G-NICAM or D/K1-FM, D/K2-FM, D/K3-FM, and D/K-NICAM	Automatic searching for stereo/bilingual-identification in case of mono transmission. Automatic and non-audible changes between Dual-FM and FM-NICAM standards while listening to the basic FM-mono sound carrier. Example: If starting with B/G-FM-Stereo, there will be a periodical alternation to B/G-NICAM in the absence of FM-Stereo/Bilingual or NICAM-identification. Once an identification is detected, the MSP keeps the corresponding standard.
BTSC-STEREO, FM Radio	Evaluation of the pilot signal and automatic switching to mono or stereo. Preparing four demodulator source channels according to Table 2–2. Detection of the SAP carrier.
M-BTSC-SAP	In the absence of SAP, the MSP switches to BTSC-stereo if available. If SAP is detected, the MSP switches automatically to SAP (see Table 2–2).

Table 2–2: Sound modes for the demodulator source channels with Automatic Sound Select

			Source Channels in Automatic Sound Select Mode			
Broadcasted Sound Standard	**Selected MSP Standard Code**[3)]	**Broadcasted Sound Mode**	**FM/AM** (source select: 0)	**Stereo or A/B** (source select: 1)	**Stereo or A** (source select: 3)	**Stereo or B** (source select: 4)
M-Korea B/G-FM D/K-FM M-Japan	02 03, 08[1)] 04, 05, 07, 0B[1)] 30	MONO	Mono	Mono	Mono	Mono
		STEREO	Stereo	Stereo	Stereo	Stereo
		BILINGUAL: Languages A and B	Left = A Right = B	Left = A Right = B	A	B
B/G-NICAM L-NICAM I-NICAM D/K-NICAM D/K-NICAM (with high deviation FM)	08, 03[2)] 09 0A 0B, 04[2)], 05[2)] 0C, 0D	NICAM not available or error rate too high	analog Mono	analog Mono	analog Mono	analog Mono
		MONO	analog Mono	NICAM Mono	NICAM Mono	NICAM Mono
		STEREO	analog Mono	NICAM Stereo	NICAM Stereo	NICAM Stereo
		BILINGUAL: Languages A and B	analog Mono	Left = NICAM A Right = NICAM B	NICAM A	NICAM B
BTSC	20, 21	MONO	Mono	Mono	Mono	Mono
		STEREO	Stereo	Stereo	Stereo	Stereo
	20	MONO + SAP	Mono	Mono	Mono	Mono
		STEREO + SAP	Stereo	Stereo	Stereo	Stereo
	21	MONO + SAP	Left = Mono Right = SAP	Left = Mono Right = SAP	Mono	SAP
		STEREO + SAP	Left = Mono Right = SAP	Left = Mono Right = SAP	Mono	SAP
FM Radio	40	MONO	Mono	Mono	Mono	Mono
		STEREO	Stereo	Stereo	Stereo	Stereo

[1)] The Automatic Sound Select process will automatically switch to the mono compatible analog standard.

[2)] The Automatic Sound Select process will automatically switch to the mono compatible digital standard.

[3)] The MSP Standard Codes are defined in Table 3–7 on page 20.

2.3. Preprocessing for SCART and I²S Input Signals

The SCART and I²S inputs need only be adjusted in level by means of the SCART and I²S prescale registers.

2.4. Source Selection and Output Channel Matrix

The Source Selector makes it possible to distribute all source signals (one of the demodulator source channels, SCART, or I²S input) to the desired output channels (Main, Aux, etc.). All input and output signals can be processed simultaneously. Each source channel is identified by a unique source address.

For each output channel, the output channel matrix can be set to sound A, sound B, stereo, or mono.

If Automatic Sound Select is on, the output channel matrix can stay fixed to stereo (transparent) for demodulated signals.

2.4.1. Mixing Unit

Any source can be selected as the input for the two channels of the Mixing unit. The mixer channel matrices and the scaling factors can be programmed separately for each channel.

After adding up both channels, the signal is fed back and is available as source 15 (Mix output) of the Source Selector.

2.5. Audio Baseband Processing

2.5.1. Automatic Volume Correction (AVC)

Different sound sources (e.g. terrestrial channels, SAT channels, or SCART) fairly often do not have the same volume level. Advertisements during movies usually have a higher volume level than the movie itself. This results in annoying volume changes. The AVC solves this problem by equalizing the volume level.

To prevent clipping, the AVC's gain decreases quickly in dynamic boost conditions. To suppress oscillation effects, the gain increases rather slowly for low level inputs. The decay time is programmable by means of the AVC register (see page 29).

For input signals ranging from –24 dBr to 0 dBr, the AVC maintains a fixed output level of –18 dBr. Fig. 2–4 shows the AVC output level versus its input level. For prescale and volume registers set to 0 dB, a level of 0 dBr corresponds to full scale input/output. This is

– SCART input/output 0 dBr = 2.0 V_{rms}

– Loudspeaker output 0 dBr = 1.4 V_{rms}

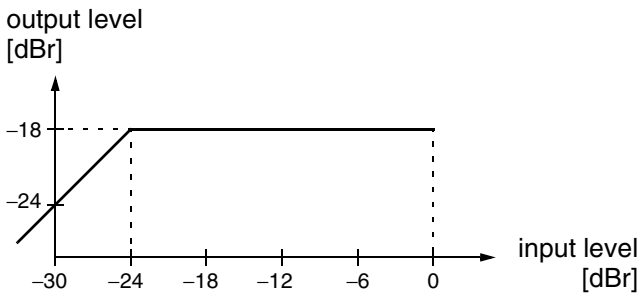


Fig. 2–4: Simplified AVC characteristics

2.5.2. Main and Aux Outputs

The Main and Aux output channels are adjustable in volume. A square wave beeper with adjustable frequency and volume can be added to them.

2.5.3. Quasi-Peak Detector

The Quasi-Peak Readout register can be used to read out the quasi-peak level of any input source. The feature is based on following filter time constants:

– attack time: 1.3 ms

– decay time: 37 ms

2.6. SCART Signal Routing

2.6.1. SCART DSP In and SCART Out Select

The SCART DSP Input Select and SCART Output Select blocks include full matrix switching facilities. To design a TV set with four pairs of SCART-inputs and two pairs of SCART-outputs, no external switching hardware is required. The switches are controlled by the ACB user register (see page 31).

2.6.2. Stand-by Mode

If the MSP 44x8G is switched off by first pulling STANDBYQ low and then (after >1 µs delay) switching off DVSUP and AVSUP, but keeping AHVSUP (**'Stand-by'-mode**), the SCART switches maintain their position and function. This allows the copying from SCART-input to SCART-output in the TV set's stand-by mode.

In case of power on or starting from stand-by (switching on the DVSUP and AVSUP, RESETQ going high 2 ms later), all internal registers except the ACB register (see page 31) are reset to the default configuration (see Table 3–5 on page 18). The reset position of the ACB register becomes active after the first I^2C transmission into the Baseband Processing part. By transmitting the ACB register first, the reset state can be redefined.

2.7. I^2S Bus Interfaces

The MSP 44x8G has two kinds of interfaces: synchronous master/slave input/output interfaces running on 48 kHz and an asynchronous slave interface.

The interfaces accept a variety of formats with different sample width, bit-orientation, and wordstrobe timing. All I^2S options are set by means of the MODUS or I^2S_CONFIG register.

2.7.1. Synchronous I^2S-Interface(s)

The synchronous I^2S bus interface consists of the pins:

– I2S_DA_IN1, I2S_DA_IN2/3 (I2S_DA_IN2 in PQFP80 package):
I^2S serial data input, 16, 18...32 bits per sample.

– I2S_DA_OUT:
I^2S serial data output, 16, 18...32 bits per sample.

– I2S_CL:
I^2S serial clock.

– I2S_WS:
I^2S word strobe signal defines the left and right sample.

If the MSP 44x8G serves as the master on the I^2S interface, the clock and word strobe lines are driven by the MSP. In this mode, only 16, 32 bits per sample can be selected. In slave mode, these lines are input to the MSP 44x8G and the MSP clock is synchronized to 384 times the I2S_WS rate (48 kHz). NICAM operation is not possible in slave mode.

An I^2S timing diagram is shown in Fig. 4–24 on page 62.

2.7.2. Asynchronous I^2S-Interface

The asynchronous I^2S slave interface allows the reception of digital stereo signals with arbitrary sample rates from 5 to 50 kHz. The synchronization is performed by means of an adaptive sample rate converter. No oversampling clock is required.

The following pins are used for the asynchronous I^2S bus interface:

– I2S_WS3 (serves only as input)

– I2S_CL3 (serves only as input)

– I2S_DA_IN2/3 (I2S_DA_IN3 in PQFP80 package).

The interface accepts I^2S-input streams with MSB first and with sample widths of 16,18...32 bits. With left/right alignment and wordstrobe timing polarity, there are additional parameters available for the adaption to a variety of formats in the I^2S-CONFIGURATION register (see page 24).

2.8. ADR Bus Interface

For the ASTRA Digital Radio System (ADR), the MSP 4408G, MSP 4418G, and MSP 4458G performs preprocessing such as carrier selection and filtering. Via the 3-line ADR-bus, the resulting signals are transferred to the DRP 3510A coprocessor, where the source decoding is performed. To be prepared for an upgrade to ADR with an additional DRP board, the following lines of MSP 44x8G should be provided on a feature connector:

– AUD_CL_OUT

– I2S_DA_IN1, 2, or 3

– I2S_DA_OUT, I2S_WS, I2S_CL

– ADR_CL, ADR_WS, ADR_DA

For more details, please refer to the DRP 3510A data sheet.

2.9. Digital Control I/O Pins and Status Change Indication

The static level of the digital input/output pins D_CTR_I/O_0/1 is switchable between HIGH and LOW via the I^2C-bus by means of the ACB register (see page 31). This enables the controlling of external hardware switches or other devices via I^2C-bus.

The digital input/output pins can be set to high impedance by means of the MODUS register (see page 23). In this mode, the pins can be used as input. The current state can be read out of the STATUS register (see page 25).

Optionally, the pin D_CTR_I/O_1 can be used as an interrupt request signal to the controller, indicating any changes in the read register STATUS. This makes polling unnecessary, I^2C bus interactions are reduced to a minimum (see “STATUS Register” on page 25 and “MODUS Register” on page 23).

2.10. Preemphasis

When using the Aux output for feeding an external modulator, a preemphasis can be applied to the right channel.

The signal is scaled down by –3 dB. An overmodulation protection is included in the algorithm which limits the output signal to 0 dBFS. Due to the nature of a preemphasis, its gain at high frequencies exceeds 3 dB. Thus, even with 0 dB input signals and prescaler / volume set to 0 dB, clipping can occur.

There are three modes present: preemphasis off, 50 µs, and 75 µs. (see Table 3–11on 29) for the register settings.

2.11. Clock PLL Oscillator and Crystal Specifications

The MSP 44x8G derives all internal system clocks from the 18.432 MHz oscillator. In NICAM or in I^2S-Slave mode of the synchronous interface, the clock is phase-locked to the corresponding source. Therefore, it is not possible to use NICAM and I^2S-Slave mode of the synchronous interface at the same time.

For proper performance, the MSP clock oscillator requires a 18.432-MHz crystal. Note that for the phase-locked modes (NICAM, I^2S-Slave), crystals with tighter tolerance are required. Please note also, that the asynchronous I^2S3 slave interface uses a different locking mechanism and does not require tighter crystal tolerances.

3. Control Interface

3.1. Device and Subaddresses

The MSP 44x8G is controlled via the I^2C bus slave interface.

The IC is selected by transmitting one of the MSP 44x8G device addresses. In order to allow up to three MSP ICs to be connected to a single bus, an address select pin (ADR_SEL) has been implemented. With ADR_SEL pulled to high, low, or left open, the MSP 44x8G responds to different device addresses. A device address pair is defined as a write address and a read address (see Table 3–1).

Writing is done by sending the write device address, followed by the subaddress byte, two address bytes, and two data bytes.

Reading is done by sending the write device address, followed by the subaddress byte and two address bytes. Without sending a stop condition, reading of the addressed data is completed by sending the device read address and reading two bytes of data.

Refer to Section 3.1.3. for the I^2C bus protocol and to Section 3.4. “Programming Tips” on page 34 for proposals of MSP 44x8G I^2C telegrams. See Table 3–2 for a list of available subaddresses.

Besides the possibility of hardware reset, the MSP can also be reset by means of the RESET bit in the CONTROL register by the controller via I^2C bus.

Due to the architecture of the MSP 44x8G, the IC cannot react immediately to an I^2C request. The typical response time is about 0.3 ms. If the MSP cannot accept another byte of data (e.g. while servicing an internal interrupt), it holds the clock line I2C_CL low to force the transmitter into a wait state. The I^2C Bus Master must read back the clock line to detect when the MSP is ready to receive the next I^2C transmission. The positions within a transmission where this may happen are indicated by ’Wait’ in section Section 3.1.3. The maximum wait period of the MSP during normal operation mode is less than 1 ms.

3.1.1. Internal Hardware Error Handling

In case of any hardware problems (e.g. interruption of the power supply of the MSP), the MSP’s wait period is extended to 1.8 ms. After this time period elapses, the MSP releases data and clock lines.

Indication and solving the error status:

To indicate the error status, the remaining acknowledge bits of the actual I^2C-protocol will be left high. Additionally, bit[14] of CONTROL is set to one. The MSP can then be reset via the I^2C bus by transmitting the RESET condition to CONTROL.

Indication of reset:

Any reset, even caused by an unstable reset line etc., is indicated in bit[15] of CONTROL.

A general timing diagram of the I^2C bus is shown in Fig. 4–23 on page 60.

Table 3–1: I^2C Bus Device Addresses

ADR_SEL	Low (connected to DVSS)		High (connected to DVSUP)		Left Open	
Mode	**Write**	**Read**	**Write**	**Read**	**Write**	**Read**
MSP device address	80_{hex}	81_{hex}	84_{hex}	85_{hex}	88_{hex}	89_{hex}

Table 3–2: I^2C Bus Subaddresses

Name	Binary Value	Hex Value	Mode	Function
CONTROL	0000 0000	00	Read/Write	Write: Software reset of MSP (see Table 3–3) Read: Hardware error status of MSP
WR_DEM	0001 0000	10	Write	write address demodulator
RD_DEM	0001 0001	11	Write	read address demodulator
WR_DSP	0001 0010	12	Write	write address DSP
RD_DSP	0001 0011	13	Write	read address DSP

3.1.2. Description of CONTROL Register

Table 3–3: CONTROL as a Write Register

Name	Subaddress	Bit[15] (MSB)	Bits[14:0]
CONTROL	00_{hex}	1 : RESET 0 : normal	0

Table 3–4: CONTROL as a Read Register

Name	Subaddress	Bit[15] (MSB)	Bit[14]	Bits[13:0]
CONTROL	00_{hex}	RESET status after last reading of CONTROL: 0 : no reset occured 1 : reset occured	Internal hardware status: 0 : no error occured 1 : internal error occured	not of interest
Reading of CONTROL will reset the bits[15,14] of CONTROL. After Power-on, bit[15] of CONTROL will be set; it must be read once to be reset.				

3.1.3. Protocol Description

Write to DSP or Demodulator

S	write device address	Wait	ACK	sub-addr	ACK	addr-byte high	ACK	addr-byte low	ACK	data-byte high	ACK	data-byte low	ACK	P

Read from DSP or Demodulator

S	write device address	Wait	ACK	sub-addr	ACK	addr-byte high	ACK	addr-byte low	ACK	S	read device address	Wait	ACK	data-byte-high	ACK	data-byte low	NAK	P

Write to Control Registers

S	write device address	Wait	ACK	sub-addr	ACK	data-byte high	ACK	data-byte low	ACK	P

Read from Control Register

S	write device address	Wait	ACK	00hex	ACK	S	read device address	Wait	ACK	data-byte-high	ACK	data-byte low	NAK	P

Note: S = I^2C-Bus Start Condition from master
P = I^2C-Bus Stop Condition from master
ACK = Acknowledge-Bit: LOW on I2C_DA from slave (= MSP, light gray) or master (= controller, dark gray)
NAK = Not Acknowledge-Bit: HIGH on I2C_DA from master (dark gray) to indicate 'End of Read' or from MSP indicating internal error state
Wait = I^2C-Clock line is held low, while the MSP is processing the I^2C command. This waiting time is max. 1 ms

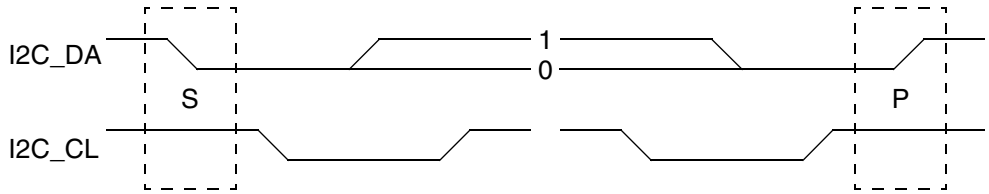


Fig. 3–1: I²C bus protocol (MSB first; data must be stable while clock is high)

3.1.4. Proposals for General MSP 44x8G I²C Telegrams

3.1.4.1. Symbols

daw	write device address (80_{hex}, 84_{hex} or 88_{hex})
dar	read device address (81_{hex}, 85_{hex} or 89_{hex})
<	Start Condition
>	Stop Condition
aa	Address Byte
dd	Data Byte

3.1.4.2. Write Telegrams

<daw 00 d0 00>	write to CONTROL register
<daw 10 aa aa dd dd>	write data into demodulator
<daw 12 aa aa dd dd>	write data into DSP

3.1.4.3. Read Telegrams

<daw 00 <dar dd dd>	read data from CONTROL register
<daw 11 aa aa <dar dd dd>	read data from demodulator
<daw 13 aa aa <dar dd dd>	read data from DSP

3.1.4.4. Examples

<80 00 80 00>	RESET MSP statically
<80 00 00 00>	Clear RESET
<80 10 00 30 00 01>	Automatic Sound Select = ON
<80 10 00 20 00 03>	Set demodulator to stand. 03_{hex}
<80 11 02 00 <81 dd dd>	Read STATUS
<80 12 00 08 01 20>	Set MAIN channel source to Stereo A/B and Matrix to Stereo (transparent mode)

More examples of typical application protocols are listed in Section 3.4. “Programming Tips” on page 34.

3.2. Start-Up Sequence: Power-Up and I²C-Controlling

After POWER-ON or RESET (see Fig. 4–22), the IC is in an inactive state. All registers are in the Reset position (see Table 3–5 and Table 3–6), the analog outputs are muted. The controller has to initialize all registers for which a non-default setting is necessary.

3.3. MSP 44x8G Programming Interface

3.3.1. User Registers Overview

The MSP 44x8G is controlled by means of user registers. The complete list of all user registers are given in Table 3–5 and Table 3–6. The registers are partitioned into the Demodulator section (Subaddress 10_{hex} for writing, 11_{hex} for reading) and the Baseband Processing sections (Subaddress 12_{hex} for writing, 13_{hex} for reading).

Write and read registers are 16 bit wide, whereby the MSB is denoted bit[15]. Transmissions via I²C bus have to take place in 16-bit words (two byte transfers, with the most significant byte transferred first). All write registers, except the demodulator write registers are readable.

Unused parts of the 16-bit write registers must be zero. **Addresses not given in this table must not be accessed.**

Table 3–5: List of MSP 44x8G Write Registers

Write Register	Address (hex)	Bits	Description and Adjustable Range	Reset	See Page
I^2C Subaddress = 10_{hex} ; Registers are *not* readable					
STANDARD SELECT	00 20	[15:0]	Initial Programming of complete Demodulator	00 00	21
MODUS	00 30	[15:0]	Demodulator, Automatic and I^2S options	00 00	22
I^2S CONFIGURATION	00 40	[15:0]	Configuration of I^2S options	00 00	24
I^2C Subaddress = 12_{hex} ; Registers are *all* readable by using I^2C Subaddress = 13_{hex}					
Volume main channel	00 00	[15:8]	[+12 dB ... –114 dB, MUTE]	MUTE	29
		[7:5] [4:0]	1/8 dB Steps must be set to 0	000_{bin} 00000_{bin}	
Volume Aux channel	00 06	[15:8]	[+12 dB ... –114 dB, MUTE]	MUTE	29
		[7:5] [4:0]	1/8 dB Steps must be set to 0	000_{bin} 00000_{bin}	
Volume SCART1 output channel	00 07	[15:8]	[+12 dB ... –114 dB, MUTE]	MUTE	30
Main source select	00 08	[15:8]	[FM/AM, NICAM, SCART, $I^2S1..3$, Mix output]	FM/AM	28
Main channel matrix		[7:0]	[SOUNDA, SOUNDB, STEREO, MONO]	SOUNDA	28
Aux source select	00 09	[15:8]	[FM/AM, NICAM, SCART, $I^2S1..3$, Mix output]	FM/AM	28
Aux channel matrix		[7:0]	[SOUNDA, SOUNDB, STEREO, MONO]	SOUNDA	28
SCART1 source select	00 0A	[15:8]	[FM/AM, NICAM, SCART, $I^2S1..3$, Mix output]	FM/AM	28
SCART1 channel matrix		[7:0]	[SOUNDA, SOUNDB, STEREO, MONO]	SOUNDA	28
I^2S source select	00 0B	[15:8]	[FM/AM, NICAM, SCART, $I^2S1..3$, Mix output]	FM/AM	28
I^2S channel matrix		[7:0]	[SOUNDA, SOUNDB, STEREO, MONO]	SOUNDA	28
Quasi-peak detector source select	00 0C	[15:8]	[FM/AM, NICAM, SCART, $I^2S1..3$, Mix output]	FM/AM	28
Quasi-peak detector matrix		[7:0]	[SOUNDA, SOUNDB, STEREO, MONO]	SOUNDA	28
Prescale SCART input	00 0D	[15:8]	[00_{hex} ... $7F_{hex}$]	00_{hex}	27
Prescale FM/AM	00 0E	[15:8]	[00_{hex} ... $7F_{hex}$]	00_{hex}	26
FM matrix		[7:0]	[NO_MAT, GSTEREO, KSTEREO]	NO_MAT	27
Prescale NICAM	00 10	[15:8]	[00_{hex} ... $7F_{hex}$]	00_{hex}	27
Prescale I^2S3	00 11	[15:8]	[00_{hex} ... $7F_{hex}$]	10_{hex}	27
Prescale I^2S2	00 12	[15:8]	[00_{hex} ... $7F_{hex}$]	10_{hex}	27
SCART switches and D_CTR_I/O	00 13	[15:0]	Bits [15:0]	00_{hex}	31
Beeper	00 14	[15:0]	[00_{hex} ... $7F_{hex}$]/[00_{hex} ... $7F_{hex}$]	$00/00_{hex}$	32
Prescale I^2S1	00 16	[15:8]	[00_{hex} ... $7F_{hex}$]	10_{hex}	27
AVC: Automatic Volume Correction	00 29	[15:8]	[off, on, decay time]	off	29
Aux Preemphasis on right channel	00 34	[15:8]	[OFF, 50 µs, 75 µs]	OFF	29
Mix1 source select	00 38	[15:8]	[FM/AM, NICAM, SCART, $I^2S1..3$, Mix output]	FM/AM	28
Mix1 channel matrix		[7:0]	[SOUNDA, SOUNDB, STEREO, MONO]	SOUNDA	28
Mix2 source select	00 39	[15:8]	[FM/AM, NICAM, SCART, $I^2S1..3$, Mix output]	FM/AM	28
Mix2 channel matrix		[7:0]	[SOUNDA, SOUNDB, STEREO, MONO]	SOUNDA	28
Scale Mix1	00 3A	[15:8]	[00_{hex} ... $7F_{hex}$]	00_{hex}	32

Table 3–5: List of MSP 44x8G Write Registers, continued

Write Register	Address (hex)	Bits	Description and Adjustable Range	Reset	See Page
Scale Mix2	00 3B	[15:8]	[00_{hex} ... $7F_{hex}$]	00_{hex}	32
Volume SCART2 output channel	00 40	[15:8]	[+12 dB ... –114 dB, MUTE]	00_{hex}	30
SCART2 source select	00 41	[15:8]	[FM/AM, NICAM, SCART, I^2S1..3, Mix output]	FM	28
SCART2 channel matrix		[7:0]	[SOUNDA, SOUNDB, STEREO, MONO]	SOUNDA	28

Table 3–6: List of MSP 44x8G Read Registers

Read Register	Address (hex)	Bits	Description and Adjustable Range	See Page
I^2C Subaddress = 11_{hex} ; Registers are *not* writable				
STANDARD RESULT	00 7E	[15:0]	Result of Automatic Standard Detection (see Table 3–8)	25
STATUS	02 00	[15:0]	Monitoring of settings e.g. Stereo, Mono, Mute, D_CTR_I/O etc. .	25
I^2C Subaddress = 13_{hex} ; Registers are *not* writable				
Quasi peak readout left	00 19	[15:0]	[00_{hex} ... $7FFF_{hex}$]16 bit two's complement	33
Quasi peak readout right	00 1A	[15:0]	[00_{hex} ... $7FFF_{hex}$]16 bit two's complement	33
MSP hardware version code	00 1E	[15:8]	[00_{hex} ... FF_{hex}]	33
MSP major revision code		[7:0]	[00_{hex} ... FF_{hex}]	33
MSP product code	00 1F	[15:8]	[00_{hex} ... FF_{hex}]	33
MSP ROM version code		[7:0]	[00_{hex} ... FF_{hex}]	33

3.3.2. Description of User Registers

Table 3–7: Standard Codes for STANDARD SELECT register

MSP Standard Code (Data in hex)	TV Sound Standard	Sound Carrier Frequencies in MHz	MSP 44x8G Version
Automatic Standard Detection			
00 01	Starts Automatic Standard Detection and sets to detected standard		all
Standard Selection			
00 02	M-Dual FM-Stereo	4.5/4.724212	4408, -18, -48, -58
00 03	B/G-Dual FM-Stereo[1)]	5.5/5.7421875	4408, -18, -58
00 04	D/K1-Dual FM-Stereo[2)]	6.5/6.2578125	
00 05	D/K2-Dual FM-Stereo[2)]	6.5/6.7421875	
00 06	D/K-FM-Mono with HDEV3[3)], not detectable by Automatic Standard Detection, HDEV3[3)] SAT-Mono (i.e. Eutelsat, see Table 6–12)	6.5	
00 07	D/K3-Dual FM-Stereo	6.5/5.7421875	4408, -18, -58
00 08	B/G-NICAM-FM[1)]	5.5/5.85	4418, -58
00 09	L-NICAM-AM	6.5/5.85	
00 0A	I-NICAM-FM	6.0/6.552	
00 0B	D/K-NICAM-FM[2)]	6.5/5.85	
00 0C	D/K-NICAM-FM with HDEV2[4)], not detectable by Automatic Standard Detection, for China	6.5/5.85	
00 0D	D/K-NICAM-FM with HDEV3[3)], not detectable by Automatic Standard Detection, for China	6.5/5.85	4418, -58
00 20	BTSC-Stereo	4.5	4428, -48, -58
00 21	BTSC-Mono + SAP		
00 30	EIA-J Japan Stereo	4.5	4428, -48, -58
00 40	FM-Stereo Radio with 75 µs Deemphasis	10.7	4428, -48, -58
00 50	SAT-Mono (see Table 6–12)	6.5	4408, -18, -58
00 51	SAT-Stereo (see Table 6–12)	7.02/7.20	4408, -18, -58
00 60	SAT ADR (Astra Digital Radio)	6.12	4408, -18, -58

[1)] In case of Automatic Sound Select, the B/G-codes 3_{hex} and 8_{hex} are equivalent.
[2)] In case of Automatic Sound Select, the D/K-codes 4_{hex}, 5_{hex}, 7_{hex} and B_{hex} are equivalent.
[3)] HDEV3: Max. FM deviation must not exceed 540 kHz
[4)] HDEV2: Max. FM deviation must not exceed 360 kHz

3.3.2.1. STANDARD SELECT Register

The TV sound standard of the MSP 44x8G demodulator is determined by the STANDARD SELECT register. There are two ways to use the STANDARD SELECT register:

– Setting up the demodulator for a TV sound standard by sending the corresponding standard code with a single I^2C bus transmission.

– Starting the Automatic Standard Detection for terrestrial TV standards. This is the most comfortable way to set up the demodulator. Within 0.5 s, the detection and setup of the actual TV sound standard is performed. The detected standard can be read out of the STANDARD RESULT register by the control processor. This feature is recommended for the primary setup of a TV set. Outputs should be muted during Automatic Standard Detection.

The Standard Codes are listed in Table 3–7.

Selecting a TV sound standard via the STANDARD SELECT register initializes the demodulator. This includes: AGC-settings and carrier mute, tuning frequencies, FIR-filter settings, demodulation mode (FM, AM, NICAM), deemphasis and identification mode.

TV stereo sound standards that are unavailable for a specific MSP version are processed in analog mono sound of the standard. In that case, stereo or bilingual processing will not be possible.

For a complete setup of the TV sound processing from analog IF input to the source selection, the transmissions as shown in Section 3.5.on page 34 are necessary.

There is a manual mode.

3.3.2.2. Refresh of STANDARD SELECT Register

A general refresh of the STANDARD SELECT register is not allowed. However, the following method enables watching the MSP 44x8G “alive” status and detection of accidental resets (only versions B6 and later):

– After Power-on, bit[15] of CONTROL will be set; it must be read once to enable the reset-detection feature.

– Reading of the CONTROL register and checking the reset indicator bit[15] .

– If bit[15] is “0”, any refresh of the STANDARD SELECT register **is not allowed.**

– If bit[15] is “1”, indicating a reset, a refresh of the STANDARD SELECT register and all other MSPG registers is required.

3.3.2.3. STANDARD RESULT Register

If Automatic Standard Detection is selected in the STANDARD SELECT register, status and result of the Automatic Standard Detection process can be read out of the STANDARD RESULT register. The possible results are based on the mentioned Standard Code and are listed in Table 3–8.

In cases where no sound standard has been detected (no standard present, too much noise, strong interferers, etc.) the STANDARD RESULT register contains 00 00_{hex}. In that case, the controller has to start further actions (for example set the standard according to a preference list or by manual input).

As long as the STANDARD RESULT register contains a value greater than 07 FF_{hex}, the Automatic Standard Detection is still active. During this period, the MODUS and STANDARD SELECT register must not be written. The STATUS register will be updated when the Automatic Standard Detection has finished.

If a present sound standard is unavailable for a specific MSP-version, it detects and switches to the analog mono sound of this standard.

Example:
The MSP 4448G will detect a B/G-NICAM signal as standard 3 and will switch to the analog FM-Mono sound.

Table 3–8: Results of the Automatic Standard Detection

Broadcasted Sound Standard	**STANDARD RESULT Register** Read $007E_{hex}$
Automatic Standard Detection could not find a sound standard	0000_{hex}
B/G-FM	0003_{hex}
B/G-NICAM	0008_{hex}
I	$000A_{hex}$
FM-Radio	0040_{hex}
M-Korea M-Japan M-BTSC	0002_{hex} (if MODUS[14,13]=00)
	0020_{hex} (if MODUS[14,13]=01)
	0030_{hex} (if MODUS[14,13]=10)
L-AM D/K1 D/K2 D/K3	0009_{hex} (if MODUS[12]=0)
	0004_{hex} (if MODUS[12]=1)
L-NICAM D/K-NICAM	0009_{hex} (if MODUS[12]=0)
	$000B_{hex}$ (if MODUS[12]=1)
Automatic Standard Detection still active	$>07FF_{hex}$

3.3.2.4. Write Registers on I^2C Subaddress 10_{hex}

Table 3–9: Write Registers on I^2C Subaddress 10_{hex}

Register Address	**Function**	**Name**
STANDARD SELECTION		
$00\ 20_{hex}$	**STANDARD SELECTION Register** Defines TV Sound or FM-Radio Standard bit[15:0] $00\ 01_{hex}$ start Automatic Standard Detection $00\ 02_{hex}$ Standard Codes (see Table 3–7) ... $00\ 60_{hex}$	STANDARD_SEL

Table 3–9: Write Registers on I^2C Subaddress 10_{hex}, continued

Register Address	Function			Name
MODUS				
00 30_{hex}	**MODUS Register**			MODUS
	Preference in Automatic Standard Detection:			
	bit[15]	0	undefined, must be 0	
	bit[14:13]		detected 4.5 MHz carrier is interpreted as:[1)]	
		0	standard M (Korea)	
		1	standard M (BTSC)	
		2	standard M (Japan)	
		3	chroma carrier (M/N standards are ignored)	
	bit[12]		detected 6.5 MHz carrier is interpreted as:[1)]	
		0	standard L (SECAM)	
		1	standard D/K1, D/K2, D/K3, or D/K NICAM	
	General MSP 44x8G Options			
	bit[11:9]	0	undefined, must be 0	
	bit[8]	0/1	ANA_IN1+/ANA_IN2+; select analog sound IF input pin	
	bit[7]	0/1	active/tristate state of audio clock output pin AUD_CL_OUT	
	bit[6]		word strobe alignment (synchronous I^2S)	
		0	WS changes at data word boundary	
		1	WS changes one clock cycle in advance	
	bit[5]	0/1	master/slave mode of I^2S interface (must be set to 0 (= Master) in case of NICAM mode)	
	bit[4]	0/1	active/tristate state of I^2S output pins	
	bit[3]		state of digital output pins D_CTR_I/O_0 and _1	
		0	active: D_CTR_I/O_0 and _1 are output pins (can be set by means of the ACB register. see also: MODUS[1])	
		1	tristate: D_CTR_I/O_0 and _1 are input pins (level can be read out of STATUS[4,3])	
	bit[2]	0	undefined, must be 0	
	bit[1]	0/1	disable/enable STATUS change indication by means of the digital I/O pin D_CTR_I/O_1 Necessary condition: MODUS[3] = 0 (active)	
	bit[0]	0/1	off/on: Automatic Sound Select	

[1)] Valid at the next start of Automatic Standard Detection.

Table 3–9: Write Registers on I^2C Subaddress 10_{hex}, continued

Register Address	Function			Name
0040_{hex}	**I^2S CONFIGURATION Register** (not mentioned bit combinations must not be used)			I2S_CONFIG
	bit[15:12]	0	undefined, must be set to 0	
	bit[11]		I^2S Data alignment (I^2S_3)	
		0	left aligned	
		1	right aligned	
	bit[10]		word strobe polarity (I^2S_3)	
		1	0 = right, 1 = left	
		0	1 = right, 0 = left	
	bit[9]		word strobe alignment (asynchronous I^2S_3)	
		0	WS changes at data word boundary	
		1	WS changes one clock cycle in advance	
	bit[8:2]	0	undefined, must be set to 0	
	bit[1:0]		I2S_CL frequency and I^2S_DA_OUT sample length	
		00	2 * 16 Bit (1.536 MHz Clk)	
		01	2 * 32 Bit (3.072 MHz Clk)	
		1x	undefined, must not be used	

3.3.2.5. Read Registers on I²C Subaddress 11_{hex}

Table 3–10: Read Registers on I²C Subaddress 11_{hex}

Register Address	Function	Name
00 $7E_{hex}$	**STANDARD RESULT Register** Readback of the detected TV Sound or FM-Radio Standard bit[15:0] 00 00_{hex} Automatic Standard Detection could not find a sound standard 00 02_{hex} MSP Standard Codes (see Table on page 24) ... 00 40_{hex} >07 FF_{hex} Automatic Standard Detection still active	STANDARD_RES
02 00_{hex}	**STATUS Register** Contains all user relevant internal information about the status of the MSP bit[15:10] undefined bit[8] 0/1 “1” indicates bilingual sound mode or SAP present (internally evaluated from received analog or digital identification signals) bit[7] 0/1 “1” indicates independent mono sound (only for NICAM) bit[6] 0/1 mono/stereo indication bit[5,9] 00 analog sound standard (FM or AM) active 01 this pattern will not occur 10 digital sound (NICAM) available 11 bad reception condition of digital sound (NICAM) due to: a. high error rate b. unimplemented sound code c. data transmission only bit[4] 0/1 low/high level of digital I/O pin D_CTR_I/O_1 bit[3] 0/1 low/high level of digital I/O pin D_CTR_I/O_0 bit[2] 0 detected secondary carrier (2nd A2 or SAP carrier) 1 no secondary carrier detected bit[1] 0 detected primary carrier (Mono or MPX carrier) 1 no primary carrier detected bit[0] undefined If STATUS change indication is activated by means of MODUS[1]: Each change in the STATUS register sets the digital I/O pin D_CTR_I/O_1 to high level. Reading the STATUS register resets D_CTR_I/O_1.	STATUS

3.3.2.6. Write Registers on I^2C Subaddress 12_{hex}

Table 3–11: Write Registers on I^2C Subaddress 12_{hex}

Register Address	Function	Name
PREPROCESSING		
00 $0E_{hex}$	**FM/AM Prescale** bit[15:8] 00_{hex} ... $7F_{hex}$ Defines the input prescale gain for the demodulated FM or AM signal 00_{hex} off (RESET condition) For all FM modes except satellite FM and AM-mode, the combinations of prescale value and FM deviation listed below lead to internal full scale with 1 kHz test signal and 50 µs emphasis. FM mode bit[15:8] $7F_{hex}$ 28 kHz FM deviation 48_{hex} 50 kHz FM deviation 30_{hex} 75 kHz FM deviation 24_{hex} 100 kHz FM deviation 18_{hex} 150 kHz FM deviation 13_{hex} 180 kHz FM deviation (limit) FM high deviation mode (HDEV2, MSP Standard Code = C_{hex}) bit[15:8] 30_{hex} 150 kHz FM deviation 14_{hex} 360 kHz FM deviation (limit) FM very high deviation mode (HDEV3, MSP Standard Code = 6) bit[15:8] 20_{hex} 450 kHz FM deviation $1A_{hex}$ 540 kHz FM deviation (limit) Satellite FM with adaptive deemphasis bit[15:8] 10_{hex} recommendation AM mode (MSP Standard Code = 9) bit[15:8] $7C_{hex}$ recommendation for SIF input levels from 0.1 V_{pp} to 0.8 V_{pp} (Due to the AGC switched on, the AM-output level remains stable and independent of the actual SIF-level in the mentioned input range)	PRE_FM

Table 3–11: Write Registers on I^2C Subaddress 12_{hex}, continued

Register Address	Function	Name
(continued) 00 $0E_{hex}$	**FM Matrix Modes** Defines the dematrix function for the demodulated FM signal bit[7:0] 00_{hex} no matrix (used for bilingual and unmatrixed stereo sound) 01_{hex} German stereo (Standard B/G) 02_{hex} Korean stereo (also used for BTSC, EIA-J, and FM Radio) 03_{hex} sound A mono (left and right channel contain the mono sound of the FM/AM mono carrier) 04_{hex} sound B mono (i.e. SAP) In case of **Automatic Sound Select = on**, the FM Matrix Mode is set automatically. Writing to the FM/AM prescale register (00 $0E_{hex}$ high part) is still allowed. In order not to disturb the automatic process, the low part of any I^2C transmission to this register is ignored. Therefore, any FM-Matrix readback values may differ from data written previously. In case of **Automatic Sound Select = off**, the FM Matrix Mode must be set as shown in Table 6–11 of Appendix B. To enable a **Forced Mono Mode** set A2 THRESHOLD as described in Section 6.3.2.on page 80	FM_MATRIX
00 10_{hex}	**NICAM Prescale** Defines the input prescale value for the digital NICAM signal bit[15:8] 00_{hex} ... $7F_{hex}$ prescale gain examples: 00_{hex} off 20_{hex} 0 dB gain $5A_{hex}$ 9 dB gain (recommendation) $7F_{hex}$ +12 dB gain (maximum gain)	PRE_NICAM
00 16_{hex} 00 12_{hex} 00 11_{hex}	**I2S1 Prescale** **I2S2 Prescale** **I2S3 Prescale** Defines the input prescale value for digital I^2S input signals bit[15:8] 00_{hex} ... $7F_{hex}$ prescale gain examples: 00_{hex} off 10_{hex} 0 dB gain (recommendation) $7F_{hex}$ +18 dB gain (maximum gain)	PRE_I2S1 PRE_I2S2 PRE_I2S3
00 $0D_{hex}$	**SCART Input Prescale** Defines the input prescale value for the analog SCART input signal bit[15:8] 00_{hex} ... $7F_{hex}$ prescale gain examples: 00_{hex} off 19_{hex} 0 dB gain (2 V_{RMS} input leads to digital full scale) $7F_{hex}$ +14 dB gain (400 mV_{RMS} input leads to digital full scale)	PRE_SCART

Table 3–11: Write Registers on I^2C Subaddress 12_{hex}, continued

Register Address	Function	Name
SOURCE SELECT AND OUTPUT CHANNEL MATRIX		
00 08_{hex} 00 09_{hex} 00 $0A_{hex}$ 00 41_{hex} 00 $0B_{hex}$ 00 $0C_{hex}$ 00 38_{hex} 00 39_{hex}	**Source for:** **Main Output** **Aux Output** **SCART1 DA Output** **SCART2 DA Output** **I^2S Output** **Quasi-Peak Detector** **Mix1 Input** **Mix2 Input** bit[15:8] 00_{hex} “FM/AM”: demodulated FM or AM mono signal 01_{hex} “Stereo or A/B”: demodulator Stereo or A/B signal 03_{hex} “Stereo or A”: demodulator Stereo Sound or Language A (only defined for Automatic Sound Select) 04_{hex} “Stereo or B”: demodulator Stereo Sound or Language B (only defined for Automatic Sound Select) 02_{hex} SCART input 05_{hex} I^2S1 input 06_{hex} I^2S2 input 07_{hex} I^2S3 input $0F_{hex}$ Mix output For demodulator sources, see Table 2–2.	SRC_MAIN SRC_AUX SRC_SCART1 SRC_SCART2 SRC_I2S SRC_QPEAK SRC_MIX1 SRC_MIX2
00 08_{hex} 00 09_{hex} 00 $0A_{hex}$ 00 41_{hex} 00 $0B_{hex}$ 00 $0C_{hex}$ 00 38_{hex} 00 39_{hex}	**Matrix Mode for:** **Main Output** **Aux Output** **SCART1 DA Output** **SCART2 DA Output** **I^2S Output** **Quasi-Peak Detector** **Mix1 Input** **Mix2 Input** bit[7:0] 00_{hex} Sound A Mono (or Left Mono) 10_{hex} Sound B Mono (or Right Mono) 20_{hex} Stereo (transparent mode) 30_{hex} Mono (sum of left and right inputs divided by 2) More modes are listed in Section 6.5.1. In Automatic Sound Select mode, the demodulator source channels are set according to Table 2–2. Therefore, the matrix modes of the corresponding output channels should be set to “Stereo” (transparent).	MAT_MAIN MAT_AUX MAT_SCART1 MAT_SCART2 MAT_I2S MAT_QPEAK MAT_MIX1 MAT_MIX2

Table 3–11: Write Registers on I^2C Subaddress 12_{hex}, continued

Register Address	Function	Name
MAIN AND AUX PROCESSING		
00 00_{hex} 00 06_{hex}	**Volume Main** **Volume Aux** bit[15:8] volume table with 1 dB step size $7F_{hex}$ +12 dB (maximum volume) $7E_{hex}$ +11 dB ... 74_{hex} +1 dB 73_{hex} 0 dB 72_{hex} −1 dB ... 02_{hex} −113 dB 01_{hex} −114 dB 00_{hex} Mute (reset condition) FF_{hex} Fast Mute (needs about 75 ms until the signal is completely ramped down) bit[7:5] higher resolution volume table 0 +0 dB 1 +0.125 dB increase in addition to the volume table ... 7 +0.875 dB increase in addition to the volume table bit[4:0] not used must be set to 0 With large scale input signals, positive volume settings may lead to signal clipping. The MSP 44x8G Main and Aux volume function is divided into a digital and an analog section. With Fast Mute, volume is reduced to mute position by digital volume only. Analog volume is not changed. This reduces any audible DC plops. To turn volume on again, the volume step that has been used before Fast Mute was activated must be transmitted.	VOL_MAIN VOL_AUX
00 29_{hex}	**Automatic Volume Correction (AVC) Loudspeaker Channel** bit[15:12] 00_{hex} AVC off (and reset internal variables) 08_{hex} AVC on bit[11:8] 08_{hex} 8 sec decay time 04_{hex} 4 sec decay time 02_{hex} 2 sec decay time 01_{hex} 20 ms decay time (should be used for approx. 100 ms after channel change)	AVC
00 34_{hex}	**Preemphasis Aux Channel** bit[15:8] 00_{hex} Preemphasis OFF $7F_{hex}$ Preemphasis 50 µs (−3 dB scaling) FF_{hex} Preemphasis 75 µs (−3 dB scaling)	PREEMP_AUX

Table 3–11: Write Registers on I^2C Subaddress 12_{hex}, continued

Register Address	Function	Name
SCART OUTPUT CHANNEL		
00 07_{hex} 00 40_{hex}	**Volume SCART1 Output Channel** **Volume SCART2 Output Channel** bit[15:8] volume table with 1 dB step size $7F_{hex}$ +12 dB (maximum volume) $7E_{hex}$ +11 dB ... 74_{hex} +1 dB 73_{hex} 0 dB 72_{hex} −1 dB ... 02_{hex} −113 dB 01_{hex} −114 dB 00_{hex} Mute (reset condition) bit[7:5] higher resolution volume table 0 +0 dB 1 +0.125 dB increase in addition to the volume table ... 7 +0.875 dB increase in addition to the volume table bit[4:0] 01_{hex} this must be 01_{hex}	VOL_SCART1 VOL_SCART2

Table 3–11: Write Registers on I^2C Subaddress 12_{hex}, continued

Register Address	Function	Name
SCART SWITCHES AND DIGITAL I/O PINS		
00 13_{hex}	**ACB Register** Defines the level of the digital output pins and the position of the SCART switches bit[15] 0/1 low/high of digital output pin D_CTR_I/O_1 (MODUS[3]=0) bit[14] 0/1 low/high of digital output pin D_CTR_I/O_0 (MODUS[3]=0) bit[13:5] SCART DSP Input Select xxxx00 xx0 SCART1 to DSP input (RESET position) xxxx01 xx0 MONO to DSP input (Set Sound A Mono in the channel matrix mode for the corresponding output channels) xxxx10 xx0 SCART2 to DSP input xxxx11 xx0 SCART3 to DSP input xxxx00 xx1 SCART4 to DSP input xxxx11 xx1 mute DSP input bit[13:5] SCART1 Output Select xx00xx x0x SCART3 input to SCART1 output (RESET position) xx01xx x0x SCART2 input to SCART1 output xx10xx x0x MONO input to SCART1 output xx11xx x0x SCART1 DA to SCART1 output xx00xx x1x SCART2 DA to SCART1 output xx01xx x1x SCART1 input to SCART1 output xx10xx x1x SCART4 input to SCART1 output xx11xx x1x mute SCART1 output bit[13:5] SCART2 Output Select 00xxxx 0xx SCART1 DA to SCART2 output (RESET position) 01xxxx 0xx SCART1 input to SCART2 output 10xxxx 0xx MONO input to SCART2 output 00xxxx 1xx SCART2 DA to SCART2 output 01xxxx 1xx SCART2 input to SCART2 output 10xxxx 1xx SCART3 input to SCART2 output 11xxxx 1xx SCART4 input to SCART2 output 11xxxx 0xx mute SCART2 output bit[4:0] must be zero The RESET position becomes active at the time of the first write transmission on the control bus to the audio processing part. By writing to the ACB register first, the RESET state can be redefined.	ACB_REG

Table 3–11: Write Registers on I^2C Subaddress 12_{hex}, continued

Register Address	Function	Name
MIXING UNIT		
00 $3A_{hex}$ 00 $3B_{hex}$	**MIX1 Scale** **MIX2 Scale** Defines the input scale value for the digital mixing unit bit[15:8] 00_{hex} off 20_{hex} 50% (–6 dB gain) 40_{hex} 100% (0 dB gain) $7F_{hex}$ 200% (+6 dB gain = maximum gain) **Note:** If the sum of both mixing inputs exceeds 100%, clipping may occur in the successive processing.	VOL_MIX1 VOL_MIX2
BEEPER		
00 14_{hex}	**Beeper Volume and Frequency** bit[15:8] Beeper Volume 00_{hex} off $7F_{hex}$ maximum volume bit[7:0] Beeper Frequency 01_{hex} 16 Hz (lowest) 40_{hex} 1 kHz FF_{hex} 4 kHz	BEEPER

3.3.2.7. Read Registers on I²C Subaddress 13_{hex}

Table 3–12: Read Registers on I²C Subaddress 13_{hex}

Register Address	Function	Name
QUASI-PEAK DETECTOR READOUT		
00 19_{hex} 00 $1A_{hex}$	**Quasi-Peak Detector Readout Left** **Quasi-Peak Detector Readout Right** bit[15:0] 0_{hex}... $7FFF_{hex}$ Values are 16 bit two's complement (only positive). A value of 4000_{hex} corresponds to internal full scale.	QPEAK_L QPEAK_R
MSP 44x8G VERSION READOUT Registers		
$001E_{hex}$	**MSP Hardware Version Code** bit[15:8] 02_{hex} MSP 44x8G-**B**3 A change in the hardware version code defines hardware optimizations that may have influence on the chip's behavior. The readout of this register is identical to the hardware version code in the chip's imprint. **MSP Family Code** bit[7:4] 1_{hex} **MSP 44**x8G-B3 **MSP Major Revision Code** bit[3:0] 7_{hex} MSP 44x8**G**-B3	MSP_HARD MSP_FAMILY MSP_REVISION
$001F_{hex}$	**MSP Product Code** bit[15:8] 08_{hex} MSP 44**08**G-B3 12_{hex} MSP 44**18**G-B3 $1C_{hex}$ MSP 44**28**G-B3 30_{hex} MSP 44**48**G-B3 $3A_{hex}$ MSP 44**58**G-B3 By means of the MSP-Product Code, the control processor is able to decide which TV sound standards have to be considered. **MSP ROM Version Code** bit[7:0] 43_{hex} MSP 44x8G-B**3** A change in the ROM version code defines internal software optimizations, that may have influence on the chip's behavior, e.g. new features may have been included. While a software change is intended to create no compatibility problems, customers that want to use the new functions can identify new MSP 44x8G versions according to this number.	MSP_PRODUCT MSP_ROM

3.4. Programming Tips

This section describes the preferred method for initializing the MSP 44x8G. The initialization is grouped into four sections:

– SCART Signal Path (analog signal path)

– Demodulator

– SCART and I²S Inputs

– Output Channels

See Fig. 2–1 on page 8 for a complete signal flow.

SCART Signal Path

1. Select analog input for the SCART baseband processing (SCART DSP Input Select) by means of the ACB register.
2. Select the source for each analog SCART output (SCART Output Select) by means of the ACB register.

Demodulator

For a complete setup of the sound processing from analog IF input to the source selection, the following steps must be performed:

1. Set MODUS register to the preferred mode and Sound IF input.
2. Write STANDARD SELECT register.
3. Choose preferred prescale (FM and NICAM) values.
4. If Automatic Sound Select is not active:
   Choose FM matrix repeatedly according to the sound mode indicated in the STATUS register.

SCART and I²S Inputs

1. Select preferred prescale for SCART.
2. Select preferred prescale for I²S inputs (set to 0 dB after RESET).

Output Channels

1. Select the source channel and matrix for each output channel.
2. Set audio baseband features (i.e. AVC, 75 µs preemphasis)
3. Select volume for each output channel.

3.5. Examples of Minimum Initialization Codes

Initialization of the MSP 44x8G according to these listings reproduces sound of the selected standard on the main output. All numbers are hexadecimal. The examples have the following structure:

1. Perform an I²C controlled reset of the IC.
2. Write MODUS register
   (with Automatic Sound Select).
3. Set Source Selection for main channel
   (with matrix set to STEREO).
4. Set Prescale
   (FM and/or NICAM and dummy FM matrix).
5. Write STANDARD SELECT register.
6. Set Volume main channel to 0 dB.

3.5.1. B/G-FM (A2 or NICAM)

```
<80 00 80 00>          // Softreset
<80 00 00 00>
<80 10 00 30 20 03>    // MODUS-Register: Automatic = on
<80 12 00 08 03 20>    // Source Sel. = (St or A) & Ch. Matr. = St
<80 12 00 0E 24 03>    // FM/AM-Prescale = 24hex,
                          FM-Matrix = MONO/SOUNDA
<80 12 00 10 5A 00>    // NICAM-Prescale = 5Ahex
<80 10 00 20 00 03>    // Standard Select: A2 B/G or NICAM B/G
          or
<80 10 00 20 00 08>
<80 12 00 00 73 00>    // Main Volume 0 dB
```

3.5.2. BTSC-Stereo

```
<80 00 80 00>          // Softreset
<80 00 00 00>
<80 10 00 30 20 03>    // MODUS-Register: Automatic = on
<80 12 00 08 03 20>    // Source Sel. = (St or A) & Ch. Matr. = St
<80 12 00 0E 24 03>    // FM/AM-Prescale = 24hex,
                          FM-Matrix = Sound A Mono
<80 10 00 20 00 20>    // Standard Select: BTSC-STEREO
<80 12 00 00 73 00>    // Main Volume 0 dB
```

3.5.3. BTSC-SAP with SAP at Main Channel

```
<80 00 80 00>          // Softreset
<80 00 00 00>
<80 10 00 30 20 03>    // MODUS-Register: Automatic = on
<80 12 00 08 04 20>    // Source Sel. = (St or B) & Ch. Matr. = St
<80 12 00 0E 24 03>    // FM/AM-Prescale = 24hex,
                          FM-Matrix = Sound A Mono
<80 10 00 20 00 21>    // Standard Select: BTSC-SAP
<80 12 00 00 73 00>    // Main Volume 0 dB
```

3.5.4. FM-Stereo Radio

<80 00 80 00> // Softreset

<80 00 00 00>

<80 10 00 30 20 03> // MODUS-Register: Automatic = on

<80 12 00 08 03 20> // Source Sel. = (St or A) & Ch. Matr. = St

<80 12 00 0E 24 03> // FM/AM-Prescale = 24_{hex},
FM-Matrix = Sound A Mono

<80 10 00 20 00 40> // Standard Select: FM-STEREO-RADIO

<80 12 00 00 73 00> // Main Volume 0 dB

3.5.5. Automatic Standard Detection

A detailed software flow diagram is shown in Fig. 3–2 on page 36.

<80 00 80 00> // Softreset

<80 00 00 00>

<80 10 00 30 20 03> // MODUS-Register: Automatic = on

<80 12 00 08 03 20> // Source Sel. = (St or A) & Ch. Matr. = St

<80 12 00 0E 24 03> // FM/AM-Prescale = 24_{hex},
FM-Matrix = Sound A Mono

<80 12 00 10 5A 00> // NICAM-Prescale = $5A_{hex}$

<80 10 00 20 00 01> // Standard Select:
Automatic Standard Detection

// Wait till STANDARD RESULT contains a value ≤ 07FF

// IF STANDARD RESULT contains 0000

// do some error handling

// ELSE

<80 12 00 00 73 00> // Main Volume 0 dB

3.5.6. Software Flow for Interrupt driven STATUS Check

A detailed software flow diagram is shown in Fig. 3–2 on page 36.

If the D_CTR_I/O_1 pin of the MSP 44x8G is connected to an interrupt input pin of the controller, the following interrupt handler can be applied to be automatically called with each status change of the MSP 44x8G. The interrupt handler may adjust the display according to the new status information.

Interrupt Handler:

<80 11 02 00 <81 dd dd> // Read STATUS

// adjust display with given status information

// Return from Interrupt

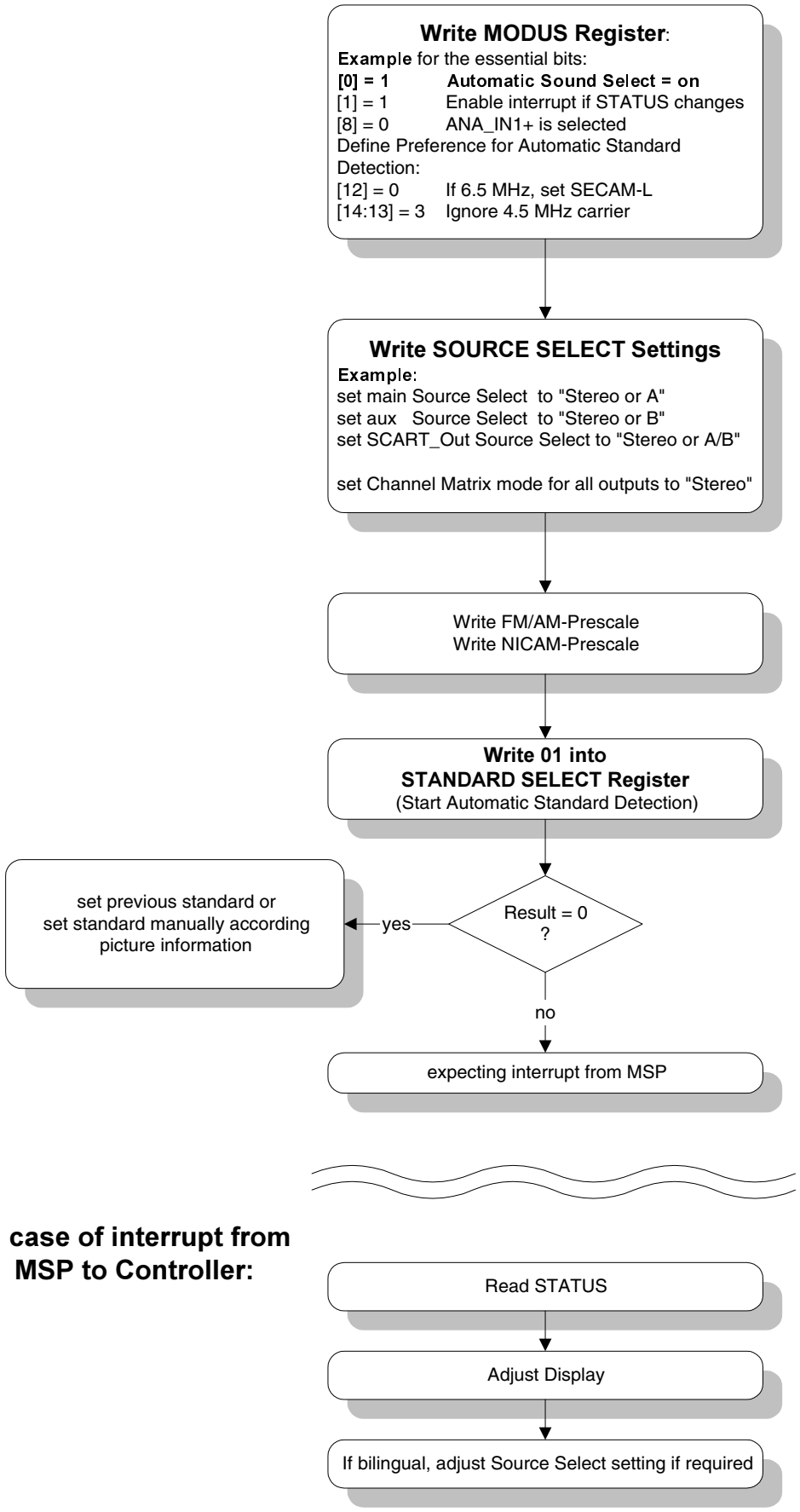
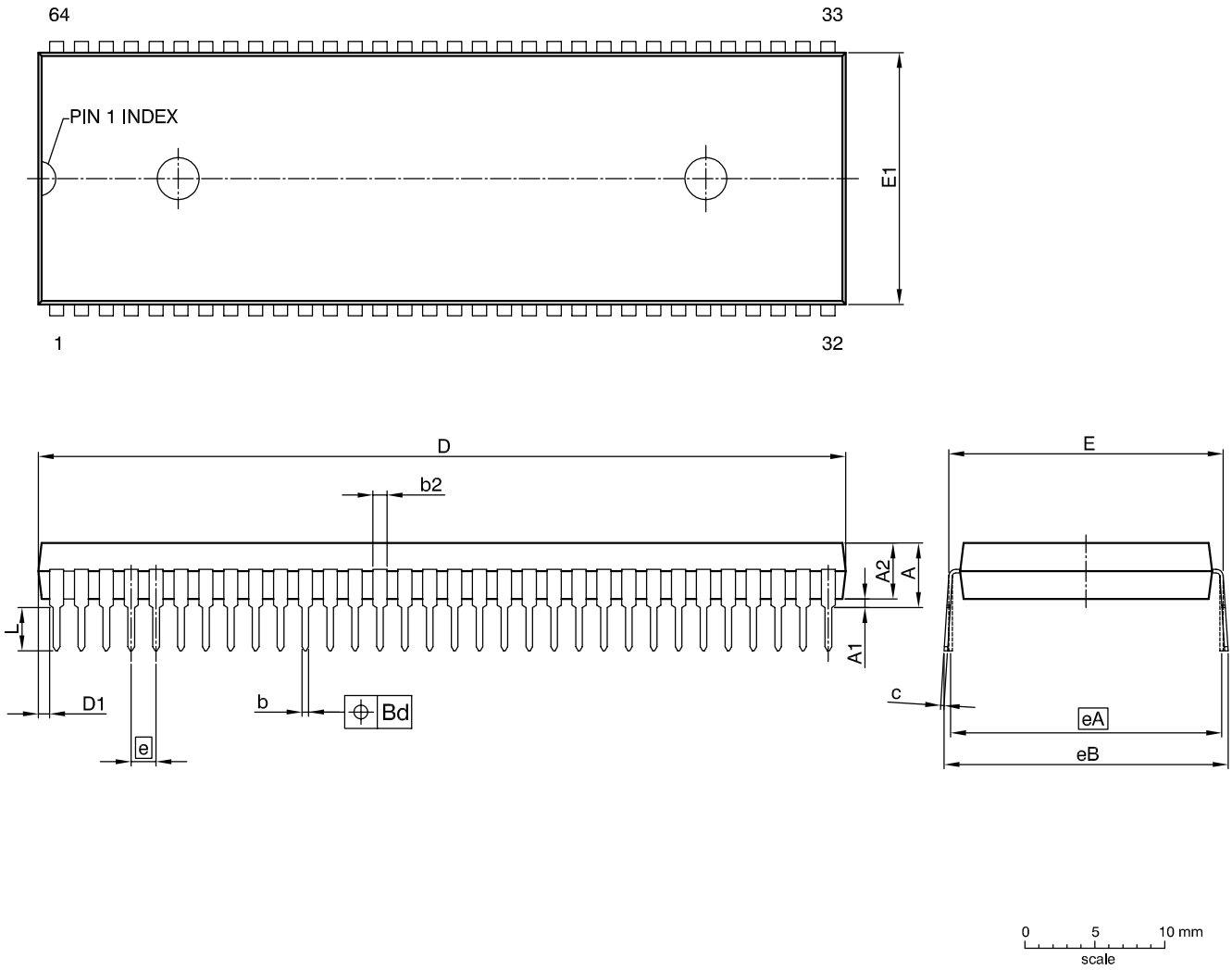


Fig. 3–2: Software flow diagram for a minimum demodulator setup for a European multistandard set applying the Automatic Sound Select feature

4. Specifications

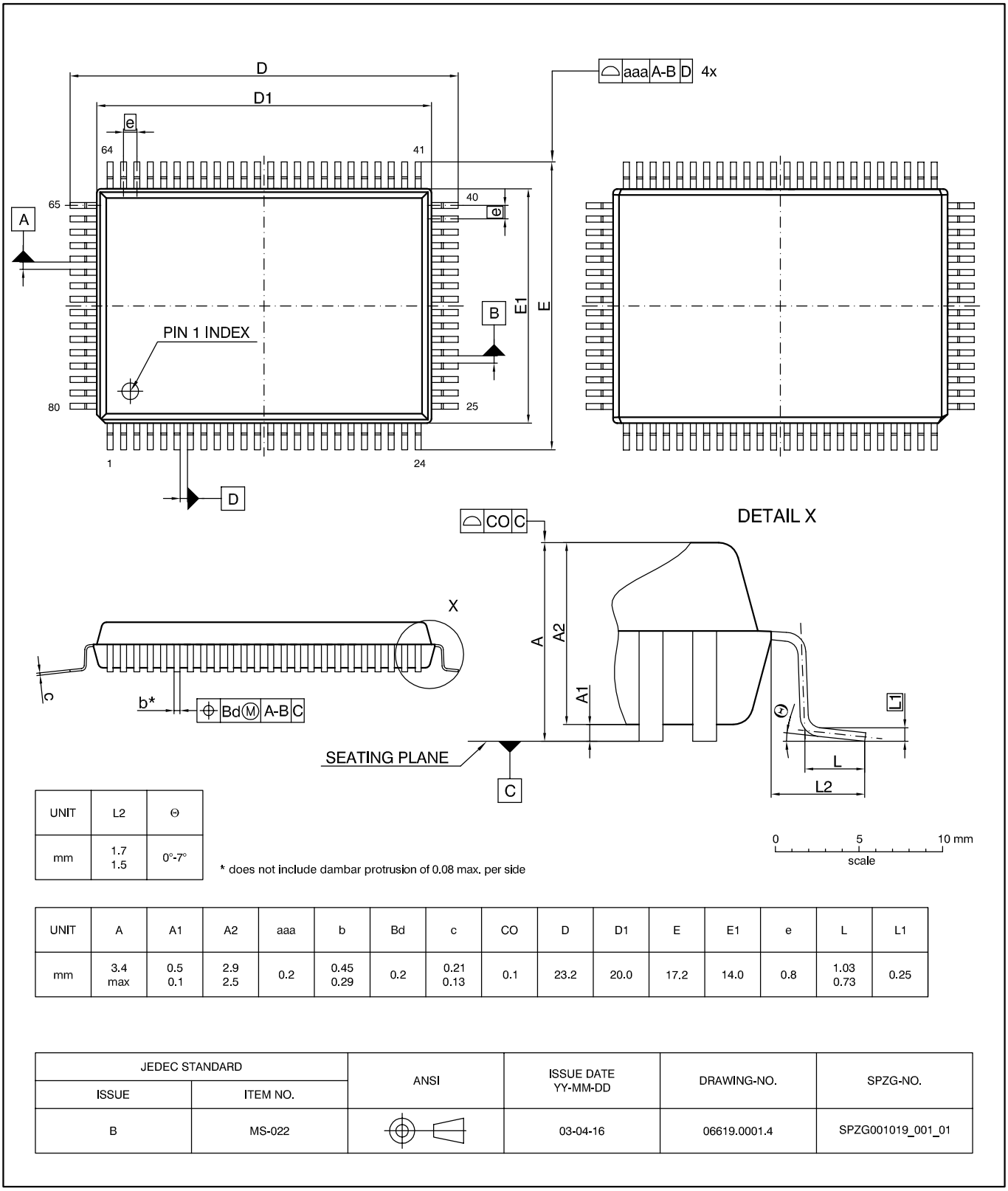
4.1. Outline Dimensions



UNIT	A max.	A1 min.	A2 max.	b	b2	Bd	c	D	D1	E	E1	e	eA	eB	L
mm	4.9	0.6	3.9	0.54 0.42	1.05 0.95	0.125	0.34 0.22	57.8 57.6	0.9 0.7	19.3	18.1 17.9	1.778	19.05	20.8 19.8	3.4 3.0

JEDEC STANDARD		ANSI	ISSUE DATE YY-MM-DD	DRAWING-NO.	SPZG-NO.
ISSUE	ITEM NO.				
A	MS-021		03-05-05	06625.0001.4	SPZG001025_001_01

Fig. 4–1:
PSDIP64-1: Plastic **S**hrink **D**ual **I**n-line **P**ackage, **64** leads, 750 mil
Ordering code: PP
Weight approximately 8.77 g



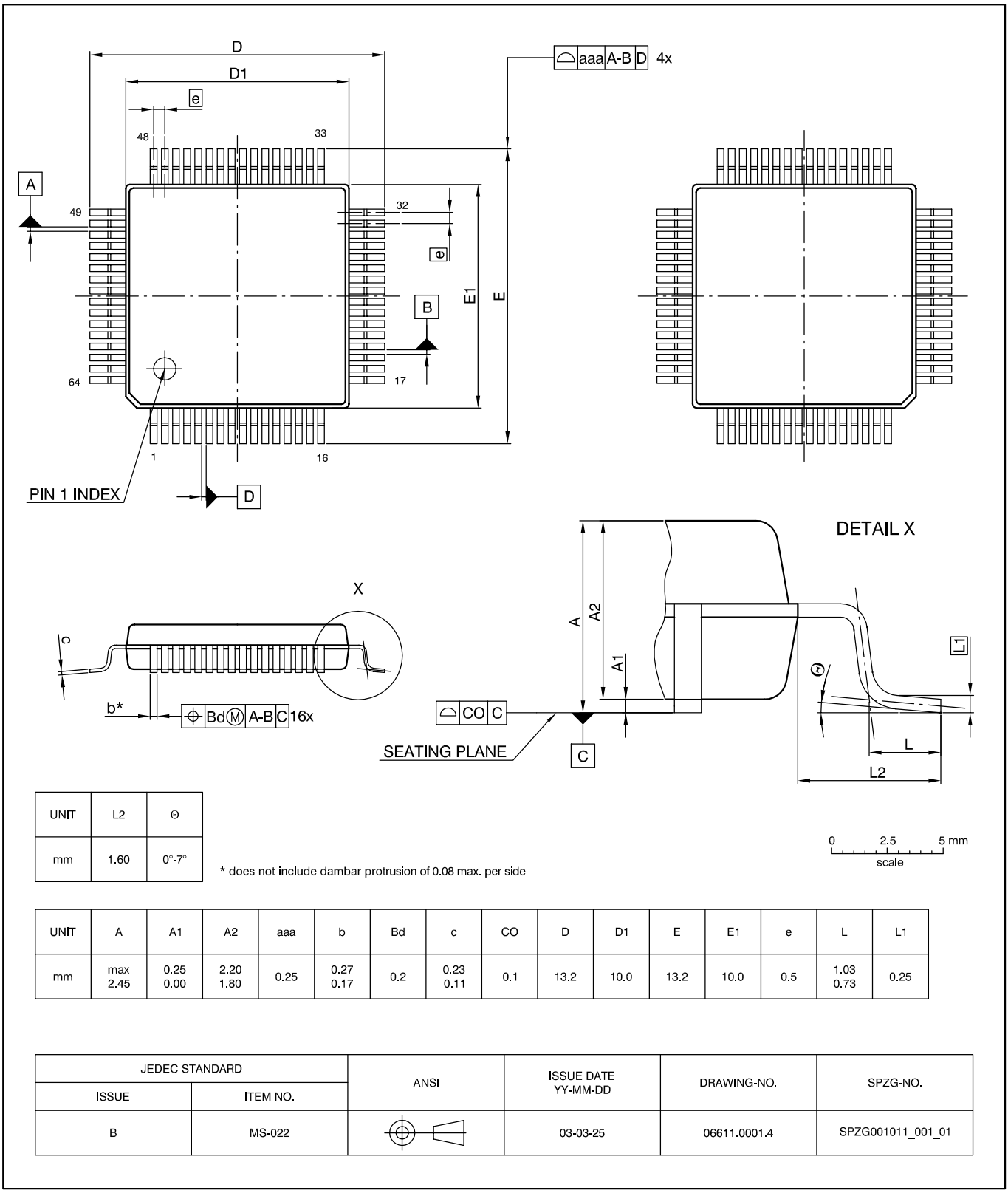
UNIT	L2	Θ
mm	1.7 1.5	0°-7°

* does not include dambar protrusion of 0.08 max. per side

UNIT	A	A1	A2	aaa	b	Bd	c	CO	D	D1	E	E1	e	L	L1
mm	3.4 max	0.5 0.1	2.9 2.5	0.2	0.45 0.29	0.2	0.21 0.13	0.1	23.2	20.0	17.2	14.0	0.8	1.03 0.73	0.25

JEDEC STANDARD		ANSI	ISSUE DATE YY-MM-DD	DRAWING-NO.	SPZG-NO.
ISSUE	ITEM NO.				
B	MS-022		03-04-16	06619.0001.4	SPZG001019_001_01

Fig. 4–2:
PMQFP80-11: Plastic **M**etric **Q**uad **F**lat **P**ackage, **80** leads, $14 \times 20 \times 2.7$ mm^3, high standoff
Ordering code: QA
Weight approximately 1.68 g



UNIT	L2	Θ
mm	1.60	0°-7°

* does not include dambar protrusion of 0.08 max. per side

UNIT	A	A1	A2	aaa	b	Bd	c	CO	D	D1	E	E1	e	L	L1
mm	max 2.45	0.25 0.00	2.20 1.80	0.25	0.27 0.17	0.2	0.23 0.11	0.1	13.2	10.0	13.2	10.0	0.5	1.03 0.73	0.25

JEDEC STANDARD		ANSI	ISSUE DATE YY-MM-DD	DRAWING-NO.	SPZG-NO.
ISSUE	ITEM NO.				
B	MS-022		03-03-25	06611.0001.4	SPZG001011_001_01

Fig. 4–3:
PMQFP64-2: Plastic **M**etric **Q**uad **F**lat **P**ackage, **64** leads, $10 \times 10 \times 2$ mm^3
Ordering code: QI
Weight approximately 0.5 g

4.2. Pin Connections and Short Descriptions

NC = not connected; leave vacant
LV = if not used, leave vacant
OBL = obligatory; connect as described in circuit diagram
DVSS: if not used, connect to DVSS
AHVSS: connect to AHVSS

Pin No.			Pin Name	Type	Connection (if not used)	Short Description
PMQFP 80-11	PMQFP 64-2	PSDIP 64-1				
1	64	8	NC		LV	Not connected
2	1	9	I2C_CL	IN/OUT	OBL	I^2C clock
3	2	10	I2C_DA	IN/OUT	OBL	I^2C data
4	3	11	I2S_CL	IN/OUT	LV	I^2S clock
5	4	12	I2S_WS	IN/OUT	LV	I^2S word strobe
6	5	13	I2S_DA_OUT	OUT	LV	I^2S data output
7	6	14	I2S_DA_IN1	IN	LV	I^2S1 data input
8	7	15	ADR_DA	OUT	LV	ADR data output
9	8	16	ADR_WS	OUT	LV	ADR word strobe
10	9	17	ADR_CL	OUT	LV	ADR clock
11	–	–	DVSUP		OBL	Digital power supply +5 V
12	–	–	DVSUP		OBL	Digital power supply +5 V
13	10	18	DVSUP		OBL	Digital power supply +5 V
14	–	–	DVSS		OBL	Digital ground
15	–	–	DVSS		OBL	Digital ground
16	11	19	DVSS		OBL	Digital ground
–	12	20	I2S_DA_IN2/3	IN	LV	$I^2S2/3$-data input
17	–	–	I2S_DA_IN2	IN	LV	PMQFP80-11: pin 22 separate I2S_DA_IN3
18	13	21	NC		LV	Not connected
19	14	22	I2S_CL3	IN	LV	I^2S3 clock
20	15	23	I2S_WS3	IN	LV	I^2S3 word strobe
21	16	24	RESETQ	IN	OBL	Power-on-reset
22	–	–	I2S_DA_IN3	IN	LV	I^2S3-data input
23	–	–	NC		LV	Not connected
24	17	25	DACA_R	OUT	LV	Aux out, right
25	18	26	DACA_L	OUT	LV	Aux out, left

Pin No.			Pin Name	Type	Connection (if not used)	Short Description
PMQFP 80-11	PMQFP 64-2	PSDIP 64-1				
26	19	27	VREF2		OBL	Reference ground 2
27	20	28	DACM_R	OUT	LV	Main out, right
28	21	29	DACM_L	OUT	LV	Main out, left
29	22	30	NC		LV	Not connected
30	23	31	NC		LV	Not connected
31	24	32	NC		LV	Not connected
32	–	–	NC		LV	Not connected
33	25	33	SC2_OUT_R	OUT	LV	SCART output 2, right
34	26	34	SC2_OUT_L	OUT	LV	SCART output 2, left
35	27	35	VREF1		OBL	Reference ground 1
36	28	36	SC1_OUT_R	OUT	LV	SCART output 1, right
37	29	37	SC1_OUT_L	OUT	LV	SCART output 1, left
38	30	38	CAPL_A		OBL	Volume capacitor Aux
39	31	39	AHVSUP		OBL	Analog power supply 8.0 V
40	32	40	CAPL_M		OBL	Volume capacitor Main
41	–	–	NC		LV	Not connected
42	–	–	NC		LV	Not connected
43	–	–	AHVSS		OBL	Analog ground
44	33	41	AHVSS		OBL	Analog ground
45	34	42	AGNDC		OBL	Analog reference voltage
46	–	–	NC		LV	Not connected
47	35	43	SC4_IN_L	IN	LV	SCART 4 input, left
48	36	44	SC4_IN_R	IN	LV	SCART 4 input, right
49	37	45	ASG		AHVSS	Analog Shield Ground
50	38	46	SC3_IN_L	IN	LV	SCART 3 input, left
51	39	47	SC3_IN_R	IN	LV	SCART 3 input, right
52	40	48	ASG		AHVSS	Analog Shield Ground
53	41	49	SC2_IN_L	IN	LV	SCART 2 input, left
54	42	50	SC2_IN_R	IN	LV	SCART 2 input, right
55	43	51	ASG		AHVSS	Analog Shield Ground
56	44	52	SC1_IN_L	IN	LV	SCART 1 input, left

Pin No.			Pin Name	Type	Connection (if not used)	Short Description
PMQFP 80-11	PMQFP 64-2	PSDIP 64-1				
57	45	53	SC1_IN_R	IN	LV	SCART 1 input, right
58	46	54	VREFTOP		OBL	Reference voltage IF A/D converter
59	–	–	NC		LV	Not connected
60	47	55	MONO_IN	IN	LV	Mono input
61	–	–	AVSS		OBL	Analog ground
62	48	56	AVSS		OBL	Analog ground
63	–	–	NC		LV	Not connected
64	–	–	NC		LV	Not connected
65	–	–	AVSUP		OBL	Analog power supply +5 V
66	49	57	AVSUP		OBL	Analog power supply +5 V
67	50	58	ANA_IN1+	IN	LV	IF input 1
68	51	59	ANA_IN–	IN	AVSS via 56 pF / LV	IF common (Can be left vacant, only if IF input 1 is also not in use)
69	52	60	ANA_IN2+	IN	AVSS via 56 pF / LV	IF input 2 (Can be left vacant, only if IF input 1 is also not in use)
70	53	61	TESTEN	IN	AVSS	Test pin
71	54	62	XTAL_IN	IN	OBL	Crystal oscillator
72	55	63	XTAL_OUT	OUT	OBL / LV	Crystal oscillator (See also Section 4.3. “Pin Descriptions” on page 43)
73	56	64	TP		LV	Test pin
74	57	1	AUD_CL_OUT	OUT	LV	Audio clock output (18.432 MHz)
75	58	2	NC		LV	Not connected
76	59	3	NC		LV	Not connected
77	60	4	D_CTR_I/O_1	IN/OUT	LV	D_CTR_I/O_1
78	61	5	D_CTR_I/O_0	IN/OUT	LV	D_CTR_I/O_0
79	62	6	ADR_SEL	IN	OBL	I^2C Bus address select
80	63	7	STANDBYQ	IN	OBL	Stand-by (low-active)

4.3. Pin Descriptions

Pin numbers refer to the PMQFP80-11 package.

Pin 1, **NC** – Pin not connected.

Pin 2, **I2C_CL** – I^2C Clock Input/Output (Fig. 4–14)
Via this pin, the I^2C-bus clock signal has to be supplied. The signal can be pulled down by the MSP in case of wait conditions.

Pin 3, **I2C_DA** – I^2C Data Input/Output (Fig. 4–14)
Via this pin, the I^2C-bus data is written to or read from the MSP.

Pin 4, **I2S_CL** – I^2S Clock Input/Output (Fig. 4–15)
Clock line for the synchronous I^2S bus. In master mode, this line is driven by the MSP; in slave mode, an external I^2S clock has to be supplied.

Pin 5, **I2S_WS** – I^2S Word Strobe Input/Output (Fig. 4–15)
Word strobe line for the synchronous I^2S bus. In master mode, this line is driven by the MSP; in slave mode, an external I^2S word strobe has to be supplied.

Pin 6, **I2S_DA_OUT1** – I^2S Data Output (Fig. 4–19)
Output of digital serial sound data of the MSP on the synchronous I^2S bus.

Pin 7, **I2S_DA_IN1** – I^2S Data Input 1 (Fig. 4–11)
First input of digital serial sound data to the MSP via the synchronous I^2S bus.

Pin 8, **ADR_DA** – ADR Bus Data Output (Fig. 4–19)
Output of digital serial data to the DRP 3510A via the ADR bus.

Pin 9, **ADR_WS** – ADR Bus Word Strobe Output (Fig. 4–19)
Word strobe output for the ADR bus.

Pin 10, **ADR_CL** – ADR Bus Clock Output (Fig. 4–19)
Clock line for the ADR bus.

Pins 11, 12, 13, **DVSUP*** – Digital Supply Voltage
Power supply for the digital circuitry of the MSP. Must be connected to a +5 V or +3.3 V power supply.

Pins 14, 15, 16, **DVSS*** – Digital Ground
Ground connection for the digital circuitry of the MSP.

Pin 17, **I2S_DA_IN2** – I^2S Data Input 2 (Fig. 4–11)
Second input of digital serial sound data to the MSP via the synchronous I^2S bus. In all packages except PQFP80, this pin is also connected to the asynchronous I^2S interface 3.

Pins 18, **NC** – Pin not connected.

Pins 19, **I2S_CL3** – I^2S Clock Input (Fig. 4–11)
Clock line for the asynchronous I^2S bus. Since only a slave mode is available an external I^2S clock has to be supplied.

Pins 20, **I2S_WS3** – I^2S Word Strobe Input (Fig. 4–11)
Word strobe line for the asynchronous I^2S bus. Since only a slave mode is available an external I^2S word strobe has to be supplied.

Pin 21, **RESETQ** – Reset Input (Fig. 4–7)
In the steady state, high level is required. A low level resets the MSP 44x8G.

Pin 22, **I2S_DA_IN3** – I^2S Data Input 3 (Fig. 4–11)
Input of digital serial sound data to the MSP via the asynchronous I^2S bus. In all packages except PQFP80, this pin is also connected to synchronous I^2S interface 2.

Pins 23, **NC** – Pin not connected.

Pins 24, 25, **DACA_R/L** – Aux Outputs (Fig. 4–17)
Output of the Aux signal. A 1 nF capacitor to AHVSS must be connected to these pins. The DC offset on these pins depends on the selected Aux volume.

Pin 26, **VREF2** – Reference Ground 2
Reference analog ground. This pin must be connected separately to the ground (AHVSS). VREF2 serves as a clean ground and should be used as the reference for analog connections to the Main and Aux outputs.

Pins 27, 28, **DACM_R/L** – Main Outputs (Fig. 4–17)
Output of the Main signal. A 1 nF capacitor to AHVSS must be connected to these pins. The DC offset on these pins depends on the selected Main volume.

Pin 29, 30, 31, 32 **NC** – Pin not connected.

Pins 33, 34, **SC2_OUT_R/L** – SCART2 Outputs (Fig. 4–18)
Output of the SCART2 signal. Connections to these pins must use a 100-Ω series resistor and are intended to be AC-coupled.

Pin 35, **VREF1** – Reference Ground 1
Reference analog ground. This pin must be connected separately to the ground (AHVSS). VREF1 serves as a clean ground and should be used as the reference for analog connections to the SCART outputs.

Pins 36, 37, **SC1_OUT_R/L** – SCART1 Outputs (Fig. 4–18)
Output of the SCART1 signal. Connections to these pins must use a 100-Ω series resistor and are intended to be AC-coupled.

Pin 38, **CAPLA** – Volume Capacitor Aux (Fig. 4–20)
A 10-µF capacitor to AHVSUP must be connected to this pin. It serves as a smoothing filter for Aux volume changes in order to suppress audible plops. The value of the capacitor can be lowered to 1-µF if faster response is required. The area encircled by the trace lines should be minimized; keep traces as short as possible. This input is sensitive for magnetic induction.

Pin 39, **AHVSUP*** – Analog Power Supply High Voltage
Power is supplied via this pin for the analog circuitry of the MSP (except IF input). This pin must be connected to the +8 V supply. (+5 V-operation is possible with restrictions in performance)

Pin 40, **CAPLM** – Volume Capacitor Main (Fig. 4–20)
A 10-µF capacitor to AHVSUP must be connected to this pin. It serves as a smoothing filter for Main volume changes in order to suppress audible plops. The value of the capacitor can be lowered to 1 µF if faster response is required. The area encircled by the trace lines should be minimized; keep traces as short as possible. This input is sensitive for magnetic induction.

Pins 41, 42, **NC** – Pins not connected.

Pins 43, 44, **AHVSS*** – Analog Power Supply High Voltage
Ground connection for the analog circuitry of the MSP (except IF input).

Pin 45, **AGNDC** – Internal Analog Reference Voltage
This pin serves as the internal ground connection for the analog circuitry (except IF input). It must be connected to the VREF pins with a 3.3-µF and a 100-nF capacitor in parallel. This pins shows a DC level of typically 3.73 V (with AHVSUP = 8 V).

Pin 46, **NC** – Pin not connected.

Pins 47, 48, **SC4_IN_L/R** – SCART4 Inputs
(Fig. 4–10)
The analog input signal for SCART4 is fed to this pin. Analog input connection must be AC-coupled.

Pins 49, 52, and 55, **ASG*** – Analog Shield Ground
Analog ground (AHVSS) should be connected to this pin to reduce cross-coupling between SCART inputs.

Pins 50, 51, **SC3_IN_L/R** – SCART3 Inputs
(Fig. 4–10)
The analog input signal for SCART3 is fed to this pin. Analog input connection must be AC-coupled.

Pins 53, 54 **SC2_IN_L/R** – SCART2 Inputs (Fig. 4–10)
The analog input signal for SCART2 is fed to this pin. Analog input connection must be AC-coupled.

Pins 56, 57 **SC1_IN_L/R** – SCART1 Inputs (Fig. 4–10)
The analog input signal for SCART1 is fed to this pin. Analog input connection must be AC-coupled.

Pin 58, **VREFTOP** – Reference Voltage IF A/D Converter (Fig. 4–12)
Via this pin, the reference voltage for the IF A/D converter is decoupled. It must be connected to AVSS pins with a 10-µF and a 100-nF capacitor in parallel. Traces must be kept short.

Pin 59, **NC** – Pin not connected.

Pin 60 **MONO_IN** – Mono Input (Fig. 4–10)
The analog mono input signal is fed to this pin. Analog input connection must be AC-coupled.

Pins 61, 62, **AVSS*** – Analog Power Supply Voltage
Ground connection for the analog IF input circuitry of the MSP.

Pins 63, 64, **NC** – Pins not connected.

Pins 65, 66, **AVSUP*** – Analog Power Supply Voltage
Power is supplied via this pin for the analog IF input circuitry of the MSP. This pin must be connected to the +5 V supply.

Pin 67, **ANA_IN1**+ – IF Input 1 (Fig. 4–12)
The analog sound IF signal is supplied to this pin. Inputs must be AC-coupled. This pin is designed as symmetrical input: ANA_IN1+ is internally connected to one input of a symmetrical op amp, ANA_IN- to the other.

Pin 68, **ANA_IN**– – IF Common (Fig. 4–12)
This pins serves as a common reference for ANA_IN1/2+ inputs and must be AC-coupled.

Pin 69, **ANA_IN2**+ – IF Input 2 (Fig. 4–12)
The analog sound if signal is supplied to this pin. Inputs must be AC-coupled. This pin is designed as symmetrical input: ANA_IN2+ is internally connected to one input of a symmetrical op amp, ANA_IN– to the other.

Pin 70, **TESTEN** – Test Enable Pin (Fig. 4–8)
This pin enables factory test modes. For normal operation, it must be connected to ground.

Pins 71, 72 **XTAL_IN, XTAL_OUT** – Crystal Input and Output Pins (Fig. 4–16)
These pins are connected to an 18.432 MHz crystal oscillator which is digitally tuned by integrated capacitances. An external clock can be fed into XTAL_IN (leave XTAL_OUT vacant in this case). The audio clock output signal AUD_CL_OUT is derived from the oscillator. External capacitors at each crystal pin to ground (AVSS) are required. It should be verified by layout, that no supply current for the digital circuitry is flowing through the ground connection point.

Pin 73, **TP** – This pin enables factory test modes. For normal operation, it must be left vacant.

Pin 74, **AUD_CL_OUT** – Audio Clock Output
(Fig. 4–16)
This is the 18.432 MHz main clock output.

Pins 75, 76, **NC** – Pins not connected.

Pins 77, 78, **D_CTR_I/O_1/0** – Digital Control Input/ Output Pins (Fig. 4–15)
These pins serve as general purpose input/output pins. Pin D_CTR_I/O_1 can be used as an interrupt request pin to the controller.

Pin 79, **ADR_SEL** – I^2C Bus Address Select
(Fig. 4–13)
By means of this pin, one of three device addresses for the MSP can be selected. The pin can be connected to ground (I^2C device addresses $80/81_{hex}$), to +5 V supply ($84/85_{hex}$), or left open ($88/89_{hex}$).

Pin 80, **STANDBYQ** – Stand-by
In normal operation, this pin must be High. If the MSP is switched off by first pulling STANDBYQ low and then (after >1 µs delay) switching off the 5 V, but keeping the 8-V power supply (‘**Stand-by’-mode**), the SCART switches maintain their position and function.

Pin -, **I2S_DA_IN2/3** –I^2S data input (see Fig. 4–11).
This pin is connected to I2S_DA_IN2 and I2S_DA_IN3. Not available for PQFP80-pin package.

*** Application Note:**
All ground pins should be connected to one low-resistive ground plane.

All supply pins should be connected separately with short and low-resistive lines to the power supply.

Decoupling capacitors from DVSUP to DVSS, AVSUP to AVSS, and AHVSUP to AHVSS are recommended as closely as possible to these pins. Decoupling of DVSUP and DVSS is most important. We recommend using more than one capacitor. By choosing different values, the frequency range of active decoupling can be extended. In our application boards we use: 220 pF, 470 pF, 1.5 nF, and 10 µF. The capacitor with the lowest value should be placed nearest to the pins.

The ASG pins should be connected as closely as possible to the MSP ground. They are intended for leading with the SCART signals as shield lines and should not be connected to ground at the SCART-connector.

4.4. Pin Configurations

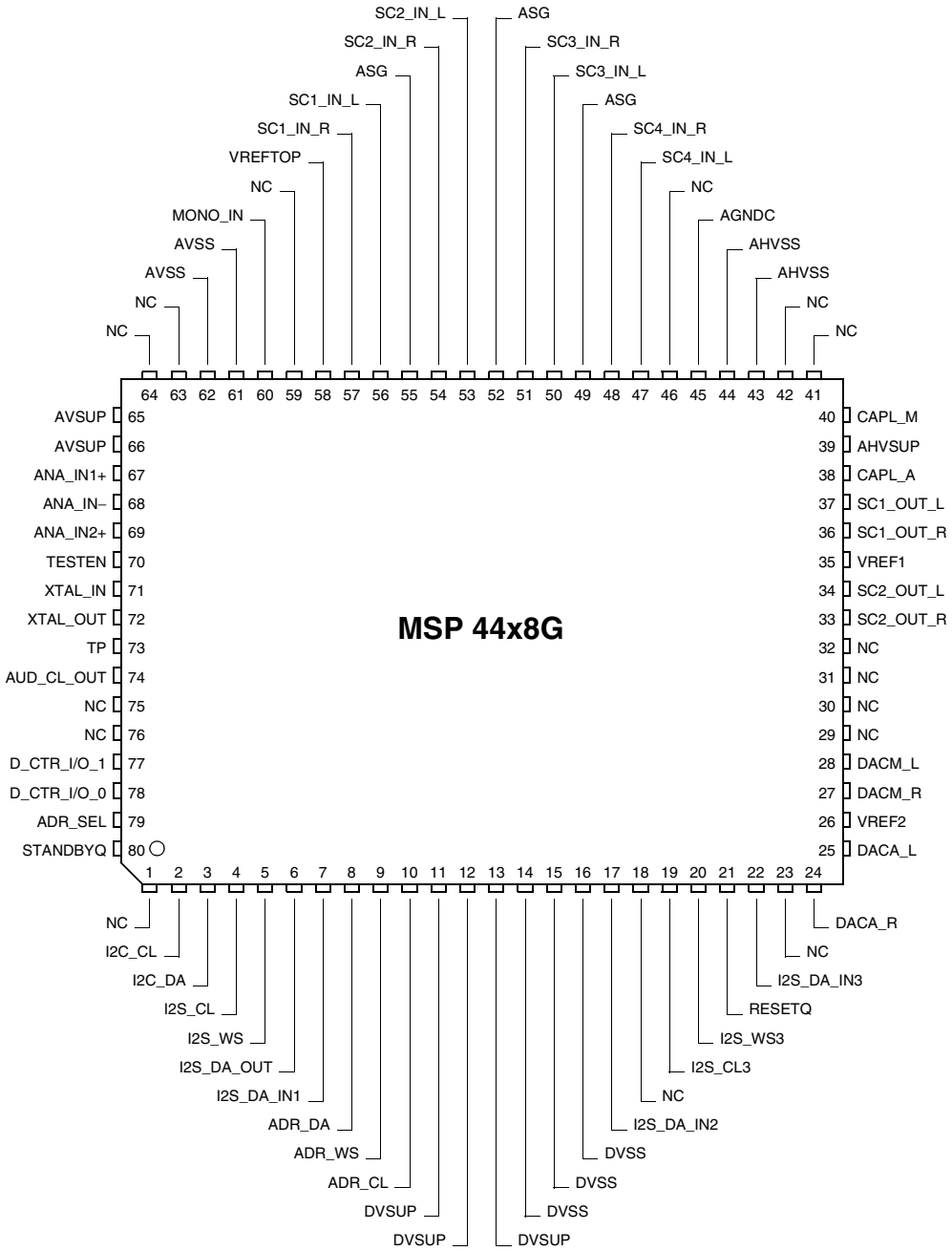


Fig. 4–4: PMQFP80-11 package

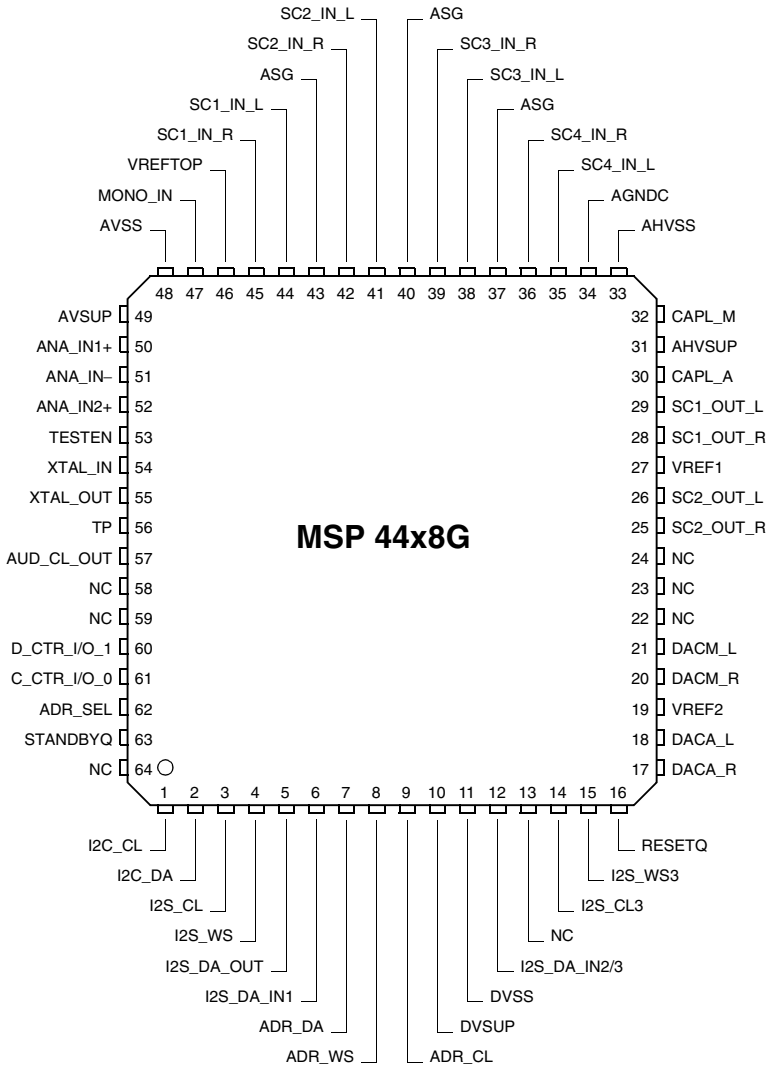


Fig. 4–5: PMQFP64-2 package

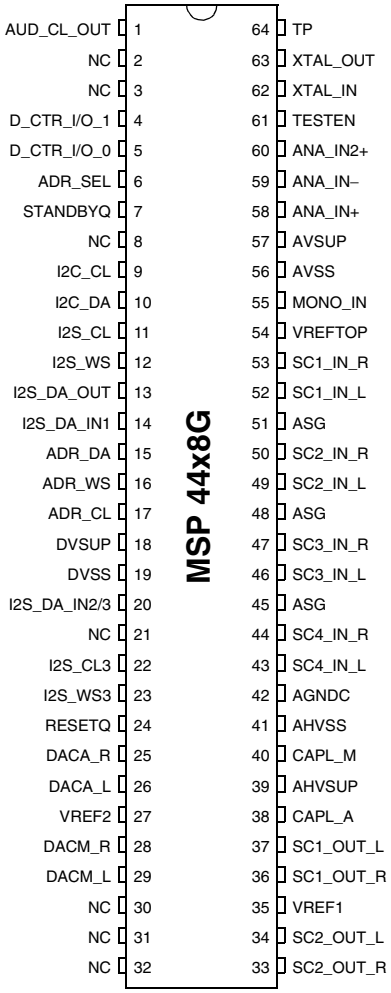


Fig. 4–6: PSDIP64-1 package

4.5. Pin Circuits

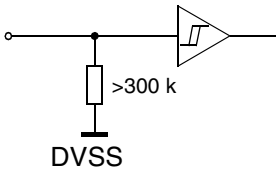


Fig. 4–7: Input Pin: **RESETQ**

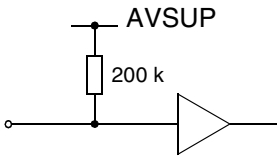


Fig. 4–8: Input Pin: **TESTEN**

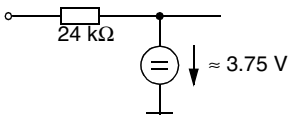


Fig. 4–9: Input Pin: **MONO_IN**

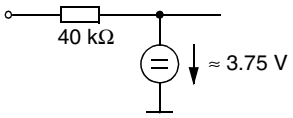


Fig. 4–10: Input Pins: **SC4-1_IN_L/R**

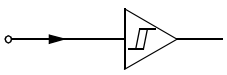


Fig. 4–11: Input Pins:
I2S_DA_IN1..3, I2S_CL3, I2S_WS3, STANDBYQ

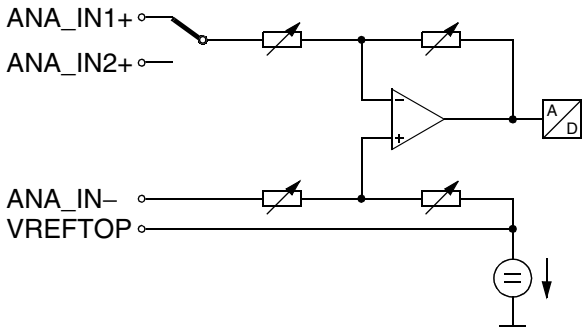


Fig. 4–12: Input Pins:
VREFTOP, ANA_IN1+, ANA_IN-, ANA_IN2+

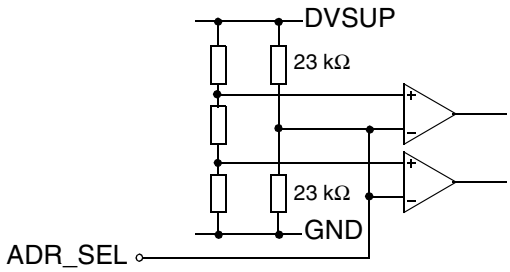


Fig. 4–13: Input Pin: **ADR_SEL**

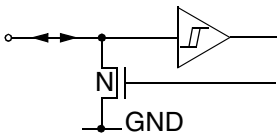


Fig. 4–14: Input/Output Pins: **I2C_CL, I2C_DA**

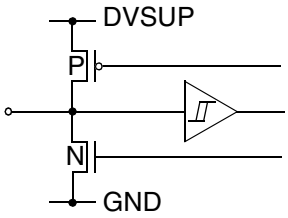


Fig. 4–15: Input/Output Pins:
I2S_CL, I2S_WS, D_CTR_I/O_1, D_CTR_I/O_0

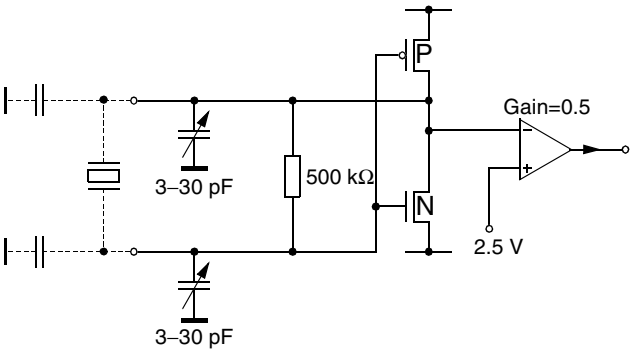


Fig. 4–16: Input/Output Pins:
XTAL_IN, XTAL_OUT, AUD_CL_OUT

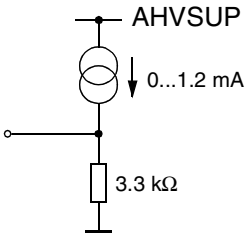


Fig. 4–17: Output Pins: **DACA_R/L, DACM_R/L**

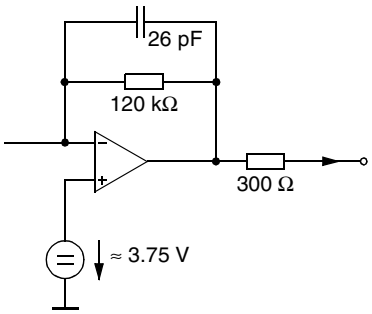


Fig. 4–18: Output Pins:
SC_2_OUT_R/L, SC_1_OUT_R/L

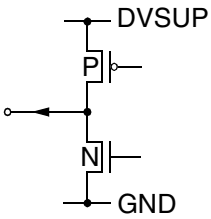


Fig. 4–19: Output Pins:
I2S_DA_OUT, ADR_DA, ADR_WS, ADR_CL

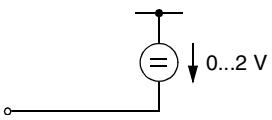


Fig. 4–20: Capacitor Pins: **CAPL_A, CAPL_M**

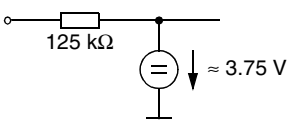


Fig. 4–21: Pin: **AGNDC**

4.6. Electrical Characteristics

Abbreviations:

tbd = to be defined
vacant = not applicable
positive current values mean current flowing into the chip

4.6.1. Absolute Maximum Ratings

Stresses beyond those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these conditions is not implied. Exposure to absolut maximum rating conditions for extended periods will affect device reliability.

All voltages listed are referenced to ground (0 V, V_{SS}), except where noted.

All grounds must be externally connected low ohmic.

This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than absolut maximum-rated voltages to this high-impedance circuit.

Table 4–1: Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Limit Values		Unit
			Min.	Max.	
T_A [1)]	Ambient Operating Temperature PSDIP64-1 PMQFP80-11 PMQFP64-2	–	0	 70 70 65	°C
T_C	Case Operating Temperature PSDIP64-1 PMQFP80-11 PMQFP64-2	–	0	 85 95 100	°C
T_S	Storage Temperature	–	–40	125	°C
P_{MAX}	Maximum Power Dissipation PSDIP64-1 PMQFP80-11 PMQFP64-2			 1540 980 1000	 mW mW mW
V_{SUP1}	Supply Voltage 1	AHVSUP	–0.3	9.0	V
V_{SUP2}	Supply Voltage 2	DVSUP	–0.3	6.0	V
V_{SUP3}	Supply Voltage 3	AVSUP	–0.3	6.0	V
V_{Idig}	Input Voltage, all Digital Inputs		–0.3	V_{SUP2}+0.3	V
I_{Idig}	Input Current, all Digital Pins	–	–20	+20	mA

[1)] Measured on standard board according to JESD 51 Standard with maximum power consumption allowed for this package.

Table 4–1: Absolute Maximum Ratings, continued

Symbol	Parameter	Pin Name	Limit Values		Unit
			Min.	Max.	
V_{Iana}	Input Voltage, all Analog Inputs	SCn_IN_s,[1] MONO_IN	–0.3	V_{SUP1}+0.3	V
I_{Iana}	Input Current, all Analog Inputs	SCn_IN_s,[1] MONO_IN	–5	+5	mA
I_{Oana}	Output Current, all SCART Outputs	SCn_OUT_s[1]	[2]	[2]	
I_{Oana}	Output Current, all Analog Outputs except SCART Outputs	DACp_s[1]	[2]	[2]	
I_{Cana}	Output Current, other pins connected to capacitors	CAPL_p,[1] AGNDC	[2]	[2]	

[1] “n” means “1”, “2”, “3”, or “4”, “s” means “L” or “R”, “p” means “M” or “A”

[2] The analog outputs are short-circuit proof with respect to Supply Voltage 1 and ground.

4.6.2. Recommended Operating Conditions

Functional operation of the device beyond those indicated in the "Recommended Operating Conditions/Characteristics" is not implied and will result in unpredictable behavior of the device and may result in device destruction.

All voltages listed are referenced to ground (V_{SS} = 0 V) except where noted.

All grounds must be externally connected low ohmic.

Do not insert the device into a live socket. Instead, apply power by switching on the external power supply. For power-up/-down sequences, see the instructions in Section 4.6.3.3. of this document.

4.6.2.1. General Recommended Operating Conditions

Symbol	Parameter	Pin Name	Limit Values			Unit
			Min.	Typ.	Max.	
T_A	Ambient Operating Temperature PSDIP64-1 PMQFP80-11 PMQFP64-2	–			[1] 70 70 65	°C
T_C	Case Operating Temperature PSDIP64-1 PMQFP80-11 PMQFP64-2	–			 85 95 100	°C
V_{SUP1}	Supply Voltage 1 (AHVSUP = 8 V)	AHVSUP	7.6	8.0	8.7	V
	Supply Voltage 1 (AHVSUP = 5 V)		4.75	5.0	5.25	V
V_{SUP2}	Supply Voltage 2 (DVSUP = 5 V)	DVSUP	4.75	5.0	5.25	V
	Supply Voltage 2 (DVSUP = 3.3 V)		3.15	3.3	3.45	V
V_{SUP3}	Supply Voltage 3	AVSUP	4.75	5.0	5.25	V
t_{STBYQ1}	STANDBYQ Setup Time before Turn-off of Second Supply Voltage	STANDBYQ, DVSUP	1			µs

[1] A power-optimized board layout is recommended. The Case Operating Temperatures mentioned in the Recommended Operating Conditions must not be exceeded at worst case conditions of the application.

4.6.2.2. Analog Input and Output Recommendations

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
C_{AGNDC}	AGNDC-Filter-Capacitor	AGNDC	–20%	3.3		µF
	Ceramic Capacitor in Parallel		–20%	100		nF
C_{inSC}	DC-Decoupling Capacitor in front of SCART Inputs	SCn_IN_s[1)]	–20%	330		nF
V_{inSC}	SCART Input Level				2.0	V_{RMS}
V_{inMONO}	Input Level, Mono Input	MONO_IN			2.0	V_{RMS}
R_{LSC}	SCART Load Resistance	SCn_OUT_s[1)]	10			kΩ
C_{LSC}	SCART Load Capacitance				6.0	nF
C_{VMA}	Main/Aux Volume Capacitor	CAPL_p		10		µF
C_{FMA}	Main/Aux Filter Capacitor	DACp_s[1)]	–10%	1	+10%	nF

[1)] “n” means “1”, “2”, “3”, or “4”, “s” means “L” or “R”, “p” means “M” or “A”

4.6.2.3. Recommendations for Analog Sound IF Input Signal

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
$C_{VREFTOP}$	VREFTOP-Filter-Capacitor	VREFTOP	–20%	10		µF
	Ceramic Capacitor in Parallel		–20%	100		nF
F_{IF_FMTV}	Analog Input Frequency Range for TV Applications	ANA_IN1+, ANA_IN2+, ANA_IN–	0		9	MHz
$F_{IF\_FMRADIO}$	Analog Input Frequency for FM-Radio Applications			10.7		MHz
V_{IF_FM}	Analog Input Range FM/NICAM		0.1	0.8	3	V_{pp}
V_{IF_AM}	Analog Input Range AM/NICAM		0.1	0.45	0.8	V_{pp}
R_{FMNI}	Ratio: NICAM Carrier/FM Carrier (unmodulated carriers) BG: I:		 –20 –23	 –7 –10	 0 0	 dB dB
R_{AMNI}	Ratio: NICAM Carrier/AM Carrier (unmodulated carriers)		–25	–11	0	dB
R_{FM}	Ratio: FM-Main/FM-Sub Satellite			7		dB
$R_{FM1/FM2}$	Ratio: FM1/FM2 German FM-System			7		dB
R_{FC}	Ratio: Main FM Carrier/ Color Carrier		15	–	–	dB
R_{FV}	Ratio: Main FM Carrier/ Luma Components		15	–	–	dB
PR_{IF}	Passband Ripple		–	–	±2	dB
SUP_{HF}	Suppression of Spectrum above 9.0 MHz (not for FM Radio)		15			dB
FM_{MAX}	Maximum FM-Deviation (approx.) normal mode HDEV2: high deviation mode HDEV3: very high deviation mode				 ±180 ±360 ±540	 kHz kHz kHz

4.6.2.4. Crystal Recommendations

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
General Crystal Recommendations						
f_P	Crystal Parallel Resonance Frequency at 12 pF Load Capacitance			18.432		MHz
R_R	Crystal Series Resistance			8	25	Ω
C_0	Crystal Shunt (Parallel) Capacitance			6.2	7.0	pF
C_L	External Load Capacitance[1)]	XTAL_IN, XTAL_OUT	PSDIP PMQFP	approx. 1.5 approx. 3.3		pF pF
Crystal Recommendations for Master-Slave Applications (MSP-clock must perform synchronization to I^2S clock)						
f_{TOL}	Accuracy of Adjustment		–20		+20	ppm
D_{TEM}	Frequency Variation versus Temperature		–20		+20	ppm
C_1	Motional (Dynamic) Capacitance		19	24		fF
f_{CL}	Required Open Loop Clock Frequency (T_{amb} = 25 °C)	AUD_CL_OUT	18.431		18.433	MHz
Crystal Recommendations for FM / NICAM Applications (No MSP-clock synchronization to I^2S clock possible)						
f_{TOL}	Accuracy of Adjustment		–30		+30	ppm
D_{TEM}	Frequency Variation versus Temperature		–30		+30	ppm
C_1	Motional (Dynamic) Capacitance		15			fF
f_{CL}	Required Open Loop Clock Frequency (T_{amb} = 25 °C)	AUD_CL_OUT	18.4305		18.4335	MHz
Crystal Recommendations for all analog FM/AM Applications (No MSP-clock synchronization to I^2S clock possible)						
f_{TOL}	Accuracy of Adjustment		–100		+100	ppm
D_{TEM}	Frequency Variation versus Temperature		–50		+50	ppm
f_{CL}	Required Open Loop Clock Frequency (T_{amb} = 25 °C)	AUD_CL_OUT	18.429		18.435	MHz
Amplitude Recommendation for Operation with External Clock Input (C_{load} after reset typ. 22 pF)						
V_{XCA}	External Clock Amplitude	XTAL_IN	0.7			V_{pp}

[1)] External capacitors at each crystal pin to ground are required. They are necessary to tune the open-loop frequency of the internal PLL and to stabilize the frequency in closed-loop operation. Due to different layouts, the accurate capacitor value should be determined with the customer PCB. The suggested values (1.5...3.3 pF) are figures based on experience and should serve as “start value”.

To adjust the capacitor value, reset the MSP. After the reset, no I^2C telegrams should be transmitted. Measure the frequency at AUD_CL_OUT-pin. Change the capacitor value until the free running frequency matches 18.432 MHz as closely as possible. The higher the capacity, the lower the resulting clock frequency.

Note: To minimize adjustment tolerances for all MSP-generations, it is strongly recommended to use the so-called MSP-XTAL-REF ICs (available in all packages) for the capacitor adjustment.

4.6.3. Characteristics

For Min./Max. values: at T_A = 0 to 70 °C, f_{CLOCK} = 18.432 MHz
V_{SUP1} = 7.6 to 8.7 V (4.75 to 5.25 V if V_{SUP1} = 5 V)
V_{SUP2} = 4.75 to 5.25 V (3.15 to 3.45 V if V_{SUP2} = 3.3 V)
V_{SUP3} = 4.75 to 5.2 V

For typical values: at T_A = 60 °C, f_{CLOCK} = 18.432 MHz
V_{SUP1} = 8 V (5 V if noted)
V_{SUP2} = 5 V (3.3 V if noted)
V_{SUP3} = 5 V

T_J = Junction Temperature

MAIN (M) = Main Channel, AUX (A) = Aux Channel

4.6.3.1. General Characteristics

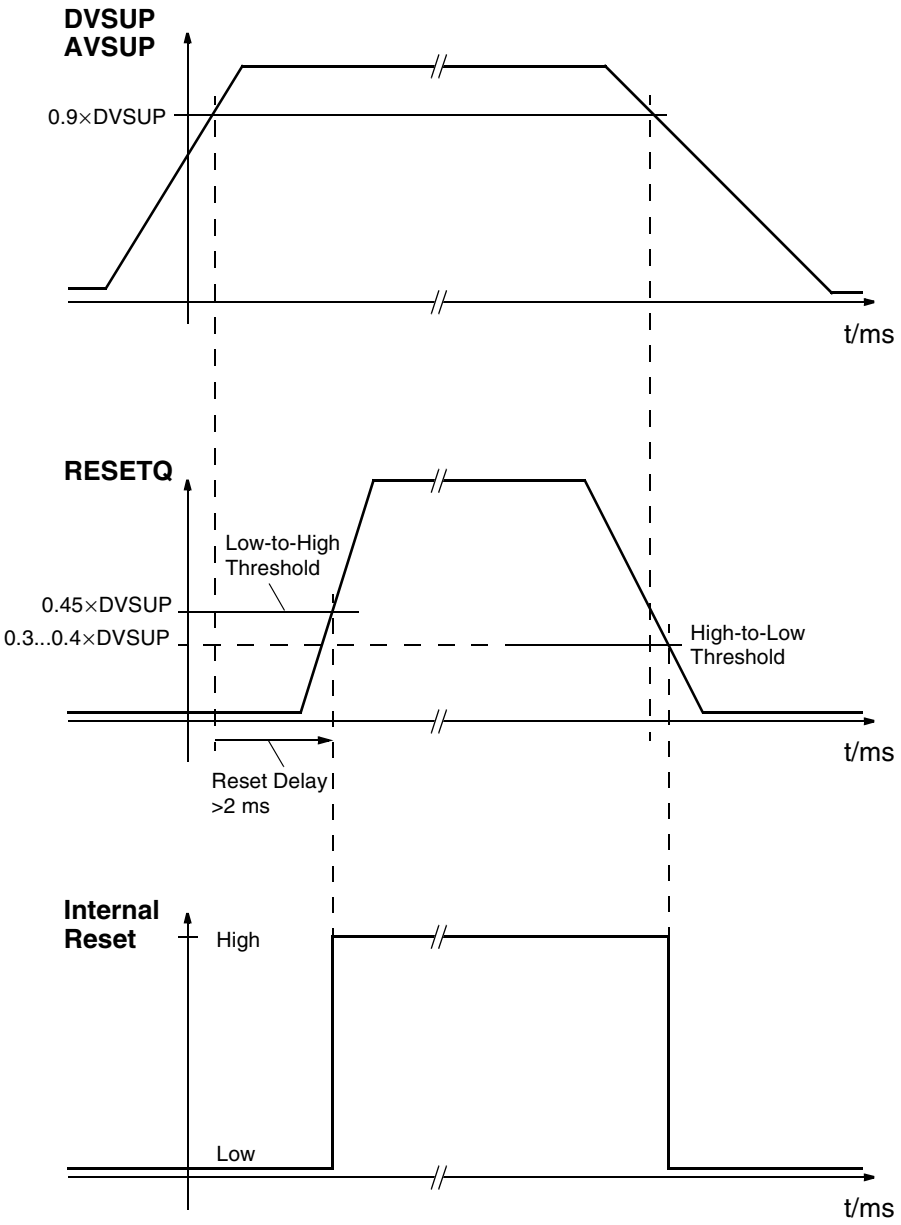
Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Supply							
I_{SUP1A}	First Supply Current (active) (AHVSUP = 8 V)	AHVSUP		17 11	25 16	mA mA	Vol. Main and Aux = 0 dB Vol. Main and Aux = -30dB
	First Supply Current (active) (AHVSUP = 5 V)			11 8	17 11	mA mA	Vol. Main and Aux = 0 dB Vol. Main and Aux = -30 dB
I_{SUP2A}	Second Supply Current (active) (DVSUP = 5 V)	DVSUP		55	70	mA	
	Second Supply Current (active) (DVSUP = 3.3 V)			55	70	mA	
I_{SUP3A}	Third Supply Current (active)	AVSUP		35	45	mA	
I_{SUP1S}	First Supply Current (AHVSUP = 8 V)	AHVSUP		5.6	7.7	mA	STANDBYQ = low
	First Supply Current (AHVSUP = 5 V)			3.7	5.1	mA	
Clock							
f_{CLOCK}	Clock Input Frequency	XTAL_IN		18.432		MHz	
D_{CLOCK}	Clock High to Low Ratio		45		55	%	
t_{JITTER}	Clock Jitter (Verification not provided in Production Test)				50	ps	
V_{xtalDC}	DC-Voltage Oscillator			2.5		V	
$t_{Startup}$	Oscillator Startup Time at VDD Slew-rate of 1 V/µs	XTAL_IN, XTAL_OUT		0.4	2	ms	
V_{ACLKAC}	Audio Clock Output AC Voltage	AUD_CL_OUT	1.2	1.8		V_{pp}	load = 40 pF
V_{ACLKDC}	Audio Clock Output DC Voltage		0.4		0.6	V_{SUP3}	I_{max} = 0.2 mA
r_{outHF_ACL}	HF Output Resistance			140		Ω	

4.6.3.2. Digital Inputs, Digital Outputs

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Digital Inputs Levels							
V_{DIGIL}	Digital Input Low Voltage	STANDBYQ D_CTR_I/O_0/1			0.2	V_{SUP2}	
V_{DIGIH}	Digital Input High Voltage		0.5			V_{SUP2}	
Z_{DIGI}	Input Impedance				5	pF	
I_{DLEAK}	Digital Input Leakage Current		−1		1	µA	0 V < U_{INPUT}< DVSUP D_CTR_I/O_0/1: tri-state
V_{DIGIL}	ADR_SEL Input Low Voltage	ADR_SEL			0.2	V_{SUP2}	
V_{DIGIH}	ADR_SEL Input High Voltage		0.8			V_{SUP2}	
I_{ADRSEL}	Input Current		−500	−220		µA	U_{ADR_SEL}= DVSS
				220	500	µA	U_{ADR_SEL}= DVSUP
Digital Output Levels							
V_{DCTROL}	Digital Output Low Voltage	D_CTR_I/O_0 D_CTR_I/O_1			0.4	V	IDDCTR = 1 mA
V_{DCTROH}	Digital Output High Voltage		V_{SUP2} − 0.3			V	IDDCTR = −1 mA

4.6.3.3. Reset Input and Power-Up

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
RESETQ Input Levels							
V_{RHL}	Reset High-Low Transition Voltage	RESETQ	0.3		0.4	V_{SUP2}	
V_{RLH}	Reset Low-High Transition Voltage			0.45		V_{SUP2}	
Z_{RES}	Input Capacitance				5	pF	
I_{RES}	Input High Current				20	µA	U_{RESETQ} = DVSUP



Note: The reset should not reach high level before the oscillator has started. This requires a reset delay of >2 ms

0.45 x DVSUP means 2.25 Volt with DVSUP = 5.0 V

Fig. 4–22: Power-up sequence

4.6.3.4. I²C-Bus Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{I2CIL}	I²C-BUS Input Low Voltage	I2C_CL, I2C_DA			0.3	V_{SUP2}	
V_{I2CIH}	I²C-BUS Input High Voltage		0.6			V_{SUP2}	
t_{I2C1}	I²C START Condition Setup Time		120			ns	
t_{I2C2}	I²C STOP Condition Setup Time		120			ns	
t_{I2C5}	I²C-Data Setup Time before Rising Edge of Clock		55			ns	
t_{I2C6}	I²C-Data Hold Time after Falling Edge of Clock		55			ns	
t_{I2C3}	I²C-Clock Low Pulse Time	I2C_CL	500			ns	
t_{I2C4}	I²C-Clock High Pulse Time		500			ns	
f_{I2C}	I²C-BUS Frequency				1.0	MHz	
V_{I2COL}	I²C-Data Output Low Voltage	I2C_CL, I2C_DA			0.4	V	I_{I2COL} = 3 mA
I_{I2COH}	I²C-Data Output High Leakage Current				1.0	µA	V_{I2COH} = 5 V
t_{I2COL1}	I²C-Data Output Hold Time after Falling Edge of Clock		15			ns	
t_{I2COL2}	I²C-Data Output Setup Time before Rising Edge of Clock		100			ns	f_{I2C} = 1 MHz

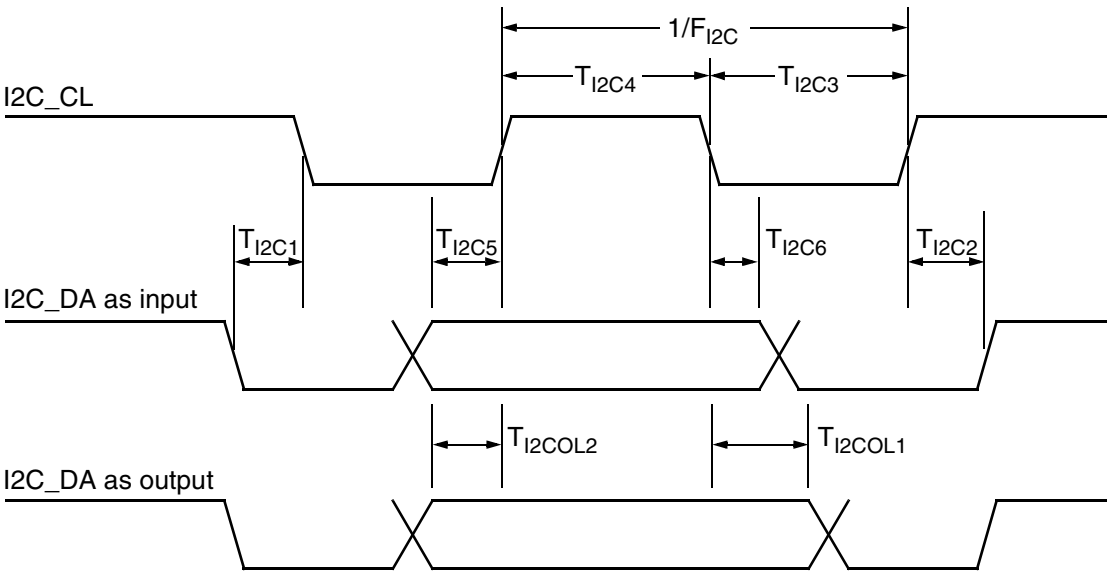
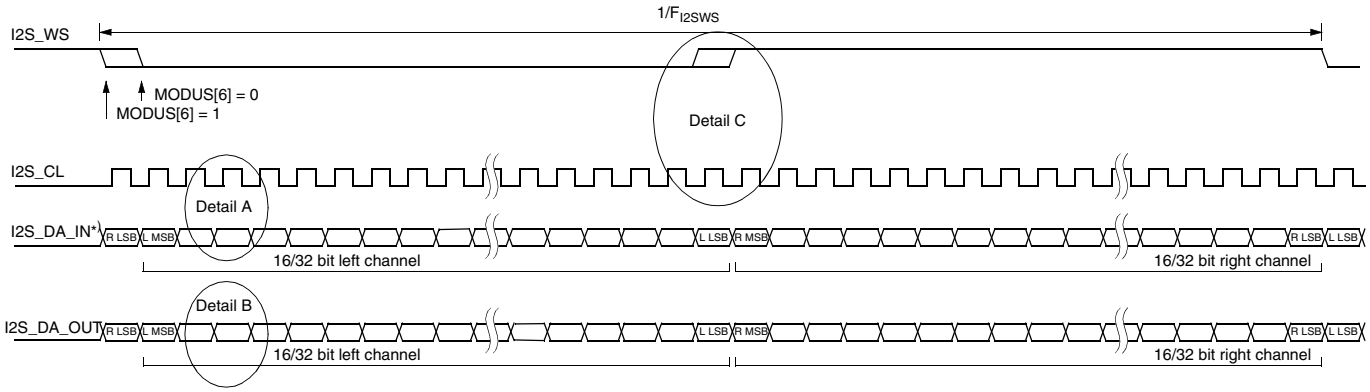


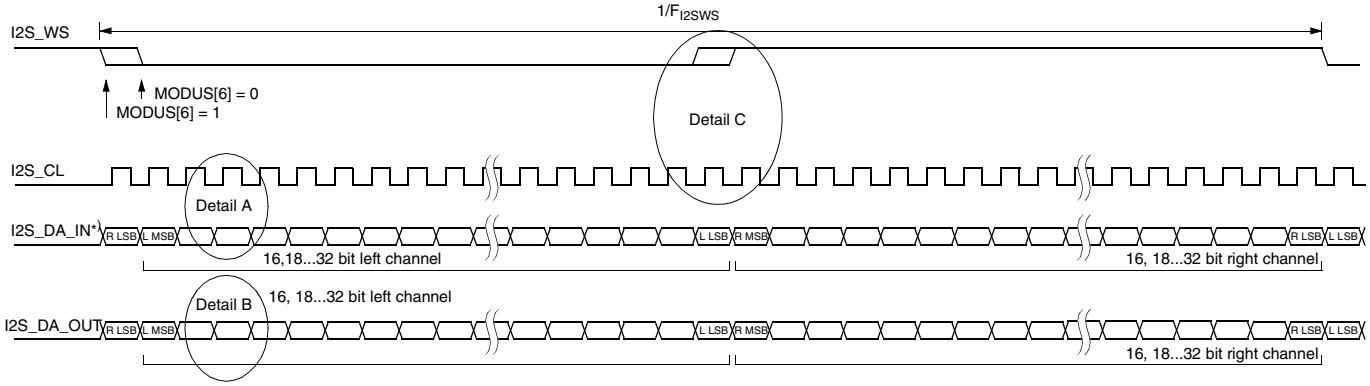
Fig. 4–23: I²C bus timing diagram

4.6.3.5. I²S-Bus Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{I2SIL}	Input Low Voltage	I2S_CL I2S_WS I2S_CL3 I2S_WS3 I2S_DA_IN1..3			0.2	V_{SUP2}	
V_{I2SIH}	Input High Voltage		0.5			V_{SUP2}	
Z_{I2SI}	Input Impedance				5	pF	
$I_{LEAKI2S}$	Input Leakage Current		–1		1	µA	0 V < U_{INPUT}< DVSUP
V_{I2SOL}	I²S Output Low Voltage	I2S_CL I2S_WS I2S_DA_OUT			0.4	V	I_{I2SOL} = 1 mA
V_{I2SOH}	I²S Output High Voltage		V_{SUP2} – 0.3			V	I_{I2SOH} = –1 mA
f_{I2SOWS}	I²S-Word Strobe Output Frequency	I2S_WS		48.0		kHz	
f_{I2SOCL}	I²S-Clock Output Frequency	I2S_CL		1.536	3.072	MHz	
$R_{I2S10/I2S20}$	I²S-Clock Output High/Low-Ratio		0.9	1.0	1.1		
Synchronous I²S Interface							
t_{s_I2S}	I²S Input Setup Time before Rising Edge of Clock	I2S_DA_IN1/2 I2S_CL	12			ns	for details see Fig. 4–24 “I²S timing diagram (synchronous interface)”
t_{h_I2S}	I²S Input Hold Time after Rising Edge of Clock		40			ns	
t_{d_I2S}	I²S Output Delay Time after Falling Edge of Clock	I2S_CL I2S_WS I2S_DA_OUT			28	ns	C_L=30 pF
f_{I2SWS}	I²S-Word Strobe Input Frequency	I2S_WS		48.0		kHz	
f_{I2SCL}	I²S-Clock Input Frequency	I2S_CL		1.536	3.072	MHz	
R_{I2SCL}	I²S-Clock Input Ratio		0.9		1.1		
Asynchronous I²S Interface							
t_{s_I2S3}	I²S3 Input Setup Time before Rising Edge of Clock	I2S_CL3 I2S_WS3 I2S_DA_IN3	4			ns	for details see Fig. 4–25 “I²S timing diagram (asynchronous interface)”
t_{h_I2S3}	I²S3 Input Hold Time after Rising Edge of Clock		40			ns	
f_{I2S3WS}	I²S3-Word Strobe Input Frequency	I2S_WS3	5		50	kHz	
f_{I2S3CL}	I²S3-Clock Input Frequency	I2S_CL3			3.2	MHz	
R_{I2S3CL}	I²S3-Clock Input Ratio		0.9		1.1		



Data: MSB first, I²S synchronous master



Data: MSB first, I²S synchronous slave

Note:

1) I2S_DA_IN can be
– I2S_DA_IN1,
– I2S_DA_IN2, or
– I2S_DA_IN2/3

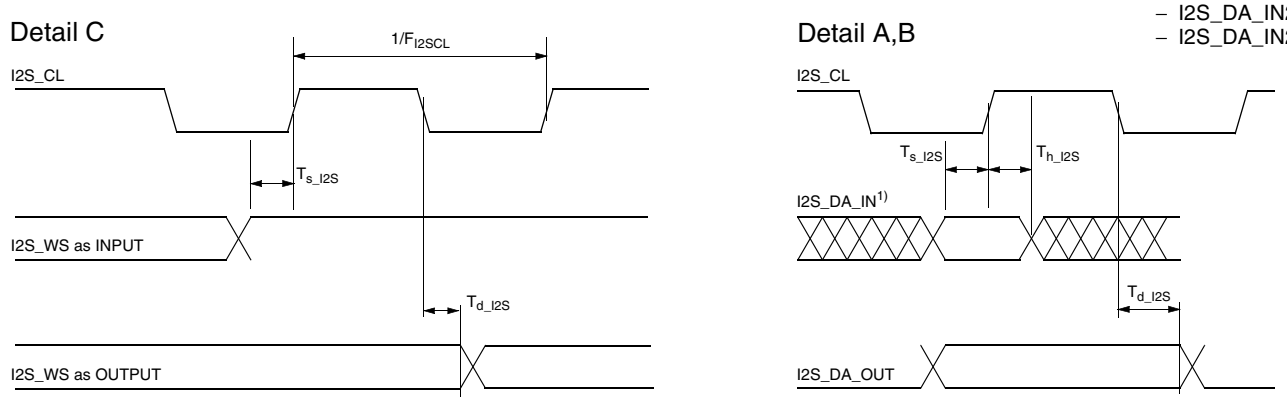


Fig. 4–24: I²S timing diagram (synchronous interface)

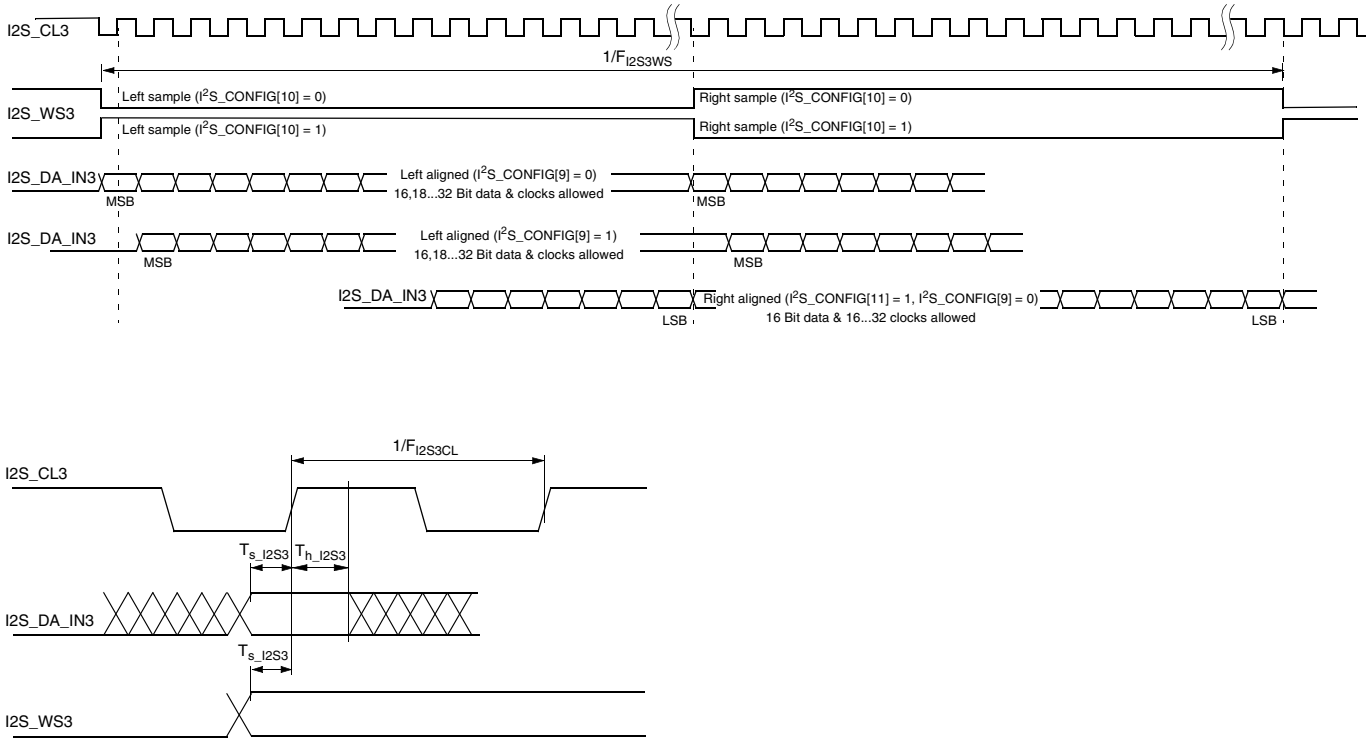


Fig. 4–25: I^2S timing diagram (asynchronous interface)

4.6.3.6. Analog Baseband Inputs and Outputs, AGNDC

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Analog Ground							
V_{AGNDC0}	AGNDC Open Circuit Voltage (AHVSUP =8 V)	AGNDC		3.77		V	$R_{load} \geq 10$ MΩ
	AGNDC Open Circuit Voltage (AHVSUP = 5 V)			2.51		V	
R_{outAGN}	AGNDC Output Resistance (AHVSUP = 8 V)		70	125	180	kΩ	3 V ≤ V_{AGNDC} ≤ 4 V
	AGNDC Output Resistance (AHVSUP = 5 V)		47	83	120	kΩ	
Analog Input Resistance							
R_{inSC}	SCART Input Resistance from T_A = 0 to 70 °C	SCn_IN_s[1)]	25	40	58	kΩ	f_{signal} = 1 kHz, I = 0.05 mA
R_{inMONO}	MONO Input Resistance from T_A = 0 to 70 °C	MONO_IN	15	24	35	kΩ	f_{signal} = 1 kHz, I = 0.1 mA

1) "n" means "1", "2", "3", or "4"; "s" means "L" or "R"

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Audio Analog-to-Digital-Converter							
V_{AICL}	Analog Input Clipping Level for Analog-to-Digital-Conversion (AHVSUP = 8 V)	SCn_IN_s,[1] MONO_IN	2.00		2.25	V_{RMS}	f_{signal} = 1 kHz
	Analog Input Clipping Level for Analog-to-Digital-Conversion (AHVSUP = 5 V)		1.13		1.51	V_{RMS}	
SCART Outputs							
R_{outSC}	SCART Output Resistance	SCn_OUT_s[1]	200 200	330	460 500	Ω Ω	f_{signal} = 1 kHz, I = 0.1 mA T_j = 27 °C T_A = 0 to 70 °C
dV_{OUTSC}	Deviation of DC-Level at SCART Output from AGNDC Voltage		−70		+70	mV	
A_{SCtoSC}	Gain from Analog Input to SCART Output	SCn_IN_s,[1] MONO_IN → SCn_OUT_s[1]	−1.0		+0.5	dB	f_{signal} = 1 kHz
$f_{rSCtoSC}$	Frequency Response from Analog Input to SCART Output		−0.5		+0.5	dB	with resp. to 1 kHz Bandwidth: 0 to 20000 Hz
V_{outSC}	Signal Level at SCART Output (AHVSUP = 8 V)	SCn_OUT_s[1]	1.8	1.9	2.0	V_{RMS}	f_{signal} = 1 kHz Volume 0 dB Full Scale input from I^2S
	Signal Level at SCART Output (AHVSUP = 5V)		1.17	1.27	1.37	V_{RMS}	
Main and Aux Outputs							
R_{outMA}	Main/AUX Output Resistance	DACp_s[1]	2.1 2.1	3.3	4.6 5.0	kΩ kΩ	f_{signal} = 1 kHz, I = 0.1 mA T_j = 27 °C T_A = 0 to 70 °C
$V_{outDCMA}$	DC-Level at Main/AUX-Output (AHVSUP = 8 V)		1.80	2.04 61	2.28	V mV	Volume 0 dB Volume −30 dB
	DC-Level at Main/AUX-Output (AHVSUP = 5 V)		1.12	1.36 40	1.60	V mV	Volume 0 dB Volume −30 dB
V_{outMA}	Signal Level at Main/AUX-Output (AHVSUP = 8 V)		1.23	1.37	1.51	V_{RMS}	f_{signal} = 1 kHz Volume 0 dB Full scale input from I^2S
	Signal Level at Main/AUX-Output (AHVSUP = 5 V)		0.76	0.90	1.04	V_{RMS}	

[1] "n" means "1", "2", "3", or "4"; "s" means "L" or "R"; "p" means "M" or "A"

4.6.3.7. Sound IF Inputs

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
R_{IFIN}	Input Impedance	ANA_IN1+, ANA_IN2+, ANA_IN–	1.5 6.8	2 9.1	2.5 11.4	kΩ kΩ	Gain AGC = 20 dB Gain AGC = 3 dB
$DC_{VREFTOP}$	DC Voltage at VREFTOP	VREFTOP	2.45	2.65	2.75	V	
DC_{ANA_IN}	DC Voltage on IF Inputs	ANA_IN1+, ANA_IN2+, ANA_IN–	1.3	1.5	1.7	V	
$XTALK_{IF}$	Crosstalk Attenuation	ANA_IN1+, ANA_IN2+, ANA_IN–	40			dB	f_{signal} = 1 MHz Input Level = –2 dBr
BW_{IF}	3 dB Bandwidth		10			MHz	
AGC	AGC Step Width			0.85		dB	

4.6.3.8. Power Supply Rejection

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
PSRR: Rejection of Noise on AHVSUP at 1 kHz							
PSRR	AGNDC	AGNDC		80		dB	
	From Analog Input to I^2S Output	MONO_IN, SCn_IN_s[1)]		70		dB	
	From Analog Input to SCART Output	MONO_IN, SCn_IN_s[1)] SCn_OUT_s[1)]		70		dB	
	From I^2S Input to SCART Output	SCn_OUT_s[1)]		60		dB	
	From I^2S Input to Main/Aux Output	DACp_s[1)]		80		dB	

1) “n” means “1”, “2”, “3”, or “4”; “s” means “L” or “R”; “p” means “M” or “A”

4.6.3.9. Analog Performance

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Specifications for AHVSUP = 8 V							
SNR	Dynamic Range and Signal-to-Noise Ratio						
	from Analog Input to I^2S Output	MONO_IN, SCn_IN_s[1)]	90	95		dB	Input Level = –20 dB with resp. to V_{AICL}, f_{sig} = 1 kHz, A-weighted 20 Hz...20 kHz
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s[1)] → SCn_OUT_s[1)]	93	96		dB	Input Level = –20 dB, f_{sig} = 1 kHz, A-weighted 20 Hz...20 kHz Volume = 0 dB
	from I^2S Input to SCART Output	SCn_OUT_s[1)]	90	95		dB	
	from I^2S Input to Main/Aux-Output for Analog Volume at 0 dB for Analog Volume at –30 dB	DACp_s[1)]	90 83	95 88		dB dB	
THD	Total Harmonic Distortion						
	from Analog Input to I^2S Output	MONO_IN, SCn_IN_s[1)]		0.008	0.03	%	Input Level = –3 dBr with resp. to V_{AICL}, f_{sig} = 1 kHz, unweighted 20 Hz...20 kHz
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s → SCn_OUT_s[1)]		0.008	0.03	%	Input Level = –3 dBr, f_{sig} = 1 kHz, unweighted 20 Hz...20 kHz
	from I^2S Input to SCART Output	SCn_OUT_s[1)]		0.008	0.03	%	
	from I^2S Input to Main or Aux Output	DACp_s[1)]		0.008	0.03	%	

1) "n" means "1", "2", "3", or "4"; "s" means "L" or "R"; "p" means "M" or "A"

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Specifications for AHVSUP = 5 V							
SNR	Dynamic Range and Signal-to-Noise Ratio						
	from Analog Input to I^2S Output	MONO_IN, SCn_IN_s[1)]	87	92		dB	Input Level = –20 dB with resp. to V_{AICL}, f_{sig} = 1 kHz, A-weighted 20 Hz...20 kHz
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s[1)] → SCn_OUT_s[1)]	90	93		dB	Input Level = –20 dB, f_{sig} = 1 kHz, A-weighted 20 Hz...20 kHz Volume = 0 dB
	from I^2S Input to SCART Output	SCn_OUT_s[1)]	87	92		dB	
	from I^2S Input to Main/Aux-Output for Analog Volume at 0 dB for Analog Volume at –30 dB	DACp_s[1)]	87 75	92 80		dB dB	
THD	Total Harmonic Distortion						
	from Analog Input to I^2S Output	MONO_IN, SCn_IN_s[1)]		0.03	0.1	%	Input Level = –3 dBr with resp. to V_{AICL}, f_{sig} = 1 kHz, unweighted 20 Hz...20 kHz
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s → SCn_OUT_s[1)]			0.1	%	Input Level = –3 dBr, f_{sig} = 1 kHz, unweighted 20 Hz...20 kHz
	from I^2S Input to SCART Output	SCn_OUT_s[1)]			0.1	%	
	from I^2S Input to Main or Aux Output	DACp_s[1)]			0.1	%	

[1)] “n” means “1”, “2”, “3”, or “4”; “s” means “L” or “R”; “p” means “M” or “A”

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
CROSSTALK Specifications							
XTALK	Crosstalk Attenuation						Input Level = –3 dB, f_{sig} = 1 kHz, unused analog inputs connected to ground by Z < 1 kΩ
	between left and right channel within SCART Input/Output pair (L→R, R→L)						unweighted 20 Hz...20 kHz
	SCn_IN → SCn_OUT[1)]		80			dB	
	SC1_IN or SC2_IN → I²S Output		80			dB	
	SC3_IN → I²S Output		80			dB	
	I²S Input → SCn_OUT[1)]		80			dB	
	between left and right channel within Main or Aux Output pair						unweighted 20 Hz...20 kHz
	I²S Input → DACp[1)]		75			dB	
	between SCART Input/Output pairs[1)]						(unweighted 20 Hz...20 kHz) same signal source on left and right disturbing channel, effect on each observed output channel
	D = disturbing program O = observed program						
	D: MONO/SCn_IN → SCn_OUT O: MONO/SCn_IN → SCn_OUT[1)]		100			dB	
	D: MONO/SCn_IN → SCn_OUT or unsel. O: MONO/SCn_IN → I²S Output		95			dB	
	D: MONO/SCn_IN → SCn_OUT O: I²S Input → SCn_OUT[1)]		100			dB	
	D: MONO/SCn_IN → unselected O: I²S Input → SC1_OUT[1)]		100			dB	
	Crosstalk between Main and Aux Output pairs						(unweighted 20 Hz...20 kHz) same signal source on left and right disturbing channel, effect on each observed output channel
	I²S Input DSP → DACp[1)]		90			dB	
XTALK	Crosstalk from Main or Aux Output to SCART Output and vice versa						(unweighted 20 Hz...20 kHz) same signal source on left and right disturbing channel, effect on each observed output channel
	D = disturbing program O = observed program						
	D: MONO/SCn_IN/DSP → SCn_OUT O: I²S Input → DACp[1)]		80			dB	SCART output load resistance 10 kΩ
	D: MONO/SCn_IN/DSP → SCn_OUT O: I²S Input → DACp[1)]		85			dB	SCART output load resistance 30 kΩ
	D: I²S Input → DACp O: MONO/SCn_IN → SCn_OUT[1)]		95			dB	
	D: I²S Input → DACM O: I²S Input → SCn_OUT[1)]		95			dB	

[1)] "n" means "1", "2", "3", or "4"; "s" means "L" or "R"; "p" means "M" or "A"

4.6.3.10. Sound Standard Dependent Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
NICAM Characteristics (MSP Standard Code = 8)							
$dV_{NICAMOUT}$	Tolerance of Output Voltage of NICAM Baseband Signal	DACp_s SCn_OUT_s[1)]	–1.5		+1.5	dB	2.12 kHz, Modulator input level = 0 dBref
S/N_{NICAM}	S/N of NICAM Baseband Signal		72			dB	NICAM: –6 dB, 1 kHz, RMS unweighted 0 to 15 kHz, Vol = 9 dB NIC_Presc = 7Fh Output level 1 V_{RMS} at DACp_s
THD_{NICAM}	Total Harmonic Distortion + Noise of NICAM Baseband Signal				0.1	%	2.12 kHz, Modulator input level = 0 dBref
BER_{NICAM}	NICAM: Bit Error Rate				1	10^{-7}	FM+NICAM, norm conditions
fR_{NICAM}	NICAM Frequency Response, 20...15000 Hz		–1.0		+1.0	dB	Modulator input level = –12 dB dBref; RMS
$XTALK_{NICAM}$	NICAM Crosstalk Attenuation (Dual)		80			dB	
SEP_{NICAM}	NICAM Channel Separation (Stereo)		80			dB	
FM Characteristics (MSP Standard Code = 3)							
dV_{FMOUT}	Tolerance of Output Voltage of FM Demodulated Signal	DACp_s, SCn_OUT_s[1)]	–1.5		+1.5	dB	1 FM-carrier, 50 µs, 1 kHz, 40 kHz deviation; RMS
S/N_{FM}	S/N of FM Demodulated Signal		73			dB	1 FM-carrier 5.5 MHz, 50 µs, 1 kHz, 40 kHz deviation; RMS, unweighted 0 to 15 kHz (for S/N); full input range, FM-Prescale = 46 h, Vol = 0 dB → Output Level 1 V_{RMS} at DACp_s
THD_{FM}	Total Harmonic Distortion + Noise of FM Demodulated Signal				0.1	%	
fR_{FM}	FM Frequency Responses, 20...15000 Hz		–1.0		+1.0	dB	1 FM-carrier 5.5 MHz, 50 µs, Modulator input level = –14.6 dBref; RMS
$XTALK_{FM}$	FM Crosstalk Attenuation (Dual)		80			dB	2 FM-carriers 5.5/5.74 MHz, 50 µs, 1 kHz, 40 kHz deviation; Bandpass 1 kHz
SEP_{FM}	FM Channel Separation (Stereo)		50			dB	2 FM-carriers 5.5/5.74 MHz, 50 µs, 1 kHz, 40 kHz deviation; RMS

1) "n" means "1", "2", "3", or "4"; "s" means "L" or "R"; "p" means "M" or "A"

2) EIM refers to 75-µs Equivalent Input Modulation. It is defined as the audio-signal level which results in a stated percentage modulation, when the DBX encoding process is replaced by a 75-µs preemphasis network.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
AM Characteristics (MSP Standard Code = 9)							
$S/N_{AM(1)}$	S/N of AM Demodulated Signal measurement condition: RMS/Flat	DACp_s, SCn_OUT_s[1)]	55			dB	SIF level: 0.1–0.8 V_{pp} AM-carrier 54% at 6.5 MHz Vol = 0 dB, FM/AM prescaler set for output = 0.5 V_{RMS} at Main out; Standard Code = 09_{hex} no video/chrominance components
$S/N_{AM(2)}$	S/N of AM Demodulated Signal measurement condition: QP/CCIR		45			dB	
THD_{AM}	Total Harmonic Distortion + Noise of AM Demodulated Signal				0.6	%	
fR_{AM}	AM Frequency Response 50 Hz... 12 kHz		–2.5		+1.0	dB	
BTSC Characteristics (MSP Standard Code = 20_{hex}, 21_{hex})							
S/N_{BTSC}	S/N of BTSC Stereo Signal S/N of BTSC-SAP Signal	DACp_s, SCn_OUT_s[1)]	68 57			dB dB	1 kHz L or R or SAP, 100% modulation, 75 µs deemphasis, RMS unweighted 0 to 15 kHz
THD_{BTSC}	THD+N of BTSC Stereo Signal THD+N of BTSC SAP Signal				0.1 0.5	% %	1 kHz L or R or SAP, 100% 75 µs EIM[2)], DBX NR or MNR, RMS unweighted 0 to 15 kHz
fR_{DBX}	Frequency Response of BTSC Stereo, 50 Hz...12 kHz Frequency Response of BTSC-SAP, 50 Hz...9 kHz		–1.0 –1.0		1.0 1.0	dB dB	L or R or SAP, 1%...66% EIM[2)], DBX NR
fR_{MNR}	Frequency Response of BTSC Stereo, 50 Hz...12 kHz		–2.0		2.0	dB	L or R 5%...66% EIM[2)], MNR
	Frequency Response of BTSC-SAP, 50 Hz...9 kHz		–2.0		2.0	dB	SAP, white noise, 10% Modulation, MNR
$XTALK_{BTSC}$	Stereo → SAP SAP → Stereo		76 80			dB dB	1 kHz L or R or SAP, 100% modulation, 75 µs deemphasis, Bandpass 1 kHz
SEP_{DBX}	Stereo Separation DBX NR 50 Hz...10 kHz 50 Hz...12 kHz		 35 30			 dB dB	L or R 1%...66% EIM[2)], DBX NR
SEP_{MNR}	Stereo Separation MNR		30			dB	L = 300 Hz, R = 3.1 kHz 14% Modulation, MNR
FM_{pil}	Pilot deviation threshold Stereo off → on Stereo on → off	ANA_IN1+, ANA_IN2+	 3.2 1.2		 3.5 1.5	 kHz kHz	4.5 MHz carrier modulated with f_h = 15.734 kHz SIF level = 100 mV_{pp} indication: STATUS Bit[6]
f_{Pilot}	Pilot Frequency Range		15.563		15.843	kHz	standard BTSC stereo signal, sound carrier only

1) "n" means "1", "2", "3", or "4"; "s" means "L" or "R"; "p" means "M" or "A"

2) EIM refers to 75-µs Equivalent Input Modulation. It is defined as the audio-signal level which results in a stated percentage modulation, when the DBX encoding process is replaced by a 75-µs preemphasis network.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
BTSC Characteristics (MSP Standard Code = 20_{hex}, 21_{hex}) with a minimum IF input signal level of 70 mVpp (measured without any video/chroma signal components)							
S/N_{BTSC}	S/N of BTSC Stereo Signal S/N of BTSC-SAP Signal	DACp_s, SCn_OUT_s[1)]	64 55			dB dB	1 kHz L or R or SAP, 100% modulation, 75 µs deemphasis, RMS unweighted 0 to 15 kHz
THD_{BTSC}	THD+N of BTSC Stereo Signal THD+N of BTSC SAP Signal				0.15 0.8	% %	1 kHz L or R or SAP, 100% 75 µs EIM[2)], DBX NR or MNR, RMS unweighted 0 to 15 kHz
fR_{DBX}	Frequency Response of BTSC Stereo, 50 Hz...12 kHz Frequency Response of BTSC-SAP, 50 Hz...9 kHz		–1.0 –1.0		1.0 1.0	dB dB	L or R or SAP, 1%...66% EIM[2)], DBX NR
fR_{MNR}	Frequency Response of BTSC Stereo, 50 Hz...12 kHz		–2.0		2.0	dB	L or R 5%...66% EIM[2)], MNR
	Frequency Response of BTSC-SAP, 50 Hz...9 kHz		–2.0		2.0	dB	SAP, white noise, 10% Modulation, MNR
$XTALK_{BTSC}$	Stereo → SAP SAP → Stereo		75 75			dB dB	1 kHz L or R or SAP, 100% modulation, 75 µs deemphasis, Bandpass 1 kHz
SEP_{DBX}	Stereo Separation DBX NR 50 Hz...10 kHz 50 Hz...12 kHz		 35 30			 dB dB	L or R 1%...66% EIM[2)], DBX NR
SEP_{MNR}	Stereo Separation MNR		30			dB	L = 300 Hz, R = 3.1 kHz 14% Modulation, MNR
EIA-J Characteristics (MSP Standard Code = 30_{hex})							
S/N_{EIAJ}	S/N of EIA-J Stereo Signal S/N of EIAJ Sub-Channel	DACp_s, SCn_OUT_s[1)]	60 60			dB dB	1 kHz L or R, 100% modulation, 75 µs deemphasis, RMS unweighted 0 to 15 kHz
THD_{EIAJ}	THD+N of EIA-J Stereo Signal THD+N of EIA-J Sub-Channel				0.2 0.3	% %	
fR_{EIAJ}	Frequency Response of EIA-J Stereo, 50 Hz...12 kHz Frequency Response of EIA-J Sub-Channel, 50 Hz...12 kHz		–1.0 –1.0		1.0 1.0	dB dB	100% modulation, 75 µs deemphasis
$XTALK_{EIAJ}$	Main → SUB Sub → Main		66 80			dB dB	1 kHz L or R, 100% modulation, 75 µs deemphasis, Bandpass 1 kHz
SEP_{EIAJ}	Stereo Separation 50 Hz...5 kHz 50 Hz...10 kHz		 35 28			 dB dB	EIA-J Stereo Signal, L or R 100% modulation

1) "n" means "1", "2", "3", or "4"; "s" means "L" or "R"; "p" means "M" or "A"

2) EIM refers to 75-µs Equivalent Input Modulation. It is defined as the audio-signal level which results in a stated percentage modulation, when the DBX encoding process is replaced by a 75-µs preemphasis network.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
FM-Radio Characteristics (MSP Standard Code = 40_{hex})							
S/N_{UKW}	S/N of FM-Radio Stereo Signal	DACp_s, SCn_OUT_s[1)]	70			dB	1 kHz L or R, 100% modulation, 75 µs deemphasis, RMS unweighted 0 to 15 kHz
THD_{UKW}	THD+N of FM-Radio Stereo Signal				0.1	%	
fR_{UKW}	Frequency Response of FM-Radio Stereo 50 Hz...15 kHz		−1.0		+1.0	dB	L or R, 1%...100% modulation, 75 µs deemphasis
Sep_{UKW}	Stereo Separation 50 Hz...15 kHz		45			dB	
f_{Pilot}	Pilot Frequency Range	ANA_IN1+ ANA_IN2+	18.844		19.125	kHz	standard FM radio stereo signal

1) “n” means “1”, “2”, “3”, or “4”; “s” means “L” or “R”; “p” means “M” or “A”

2) EIM refers to 75-µs Equivalent Input Modulation. It is defined as the audio-signal level which results in a stated percentage modulation, when the DBX encoding process is replaced by a 75-µs preemphasis network.

5. Appendix A: Overview of TV-Sound Standards

5.1. NICAM 728

Table 5–1: Summary of NICAM 728 sound modulation parameters

Specification	I	B/G	L		D/K	
Carrier frequency of digital sound	6.552 MHz	5.85 MHz	5.85 MHz		5.85 MHz	
Transmission rate	728 kbit/s					
Type of modulation	Differentially encoded quadrature phase shift keying (DQPSK)					
Spectrum shaping Roll-off factor	by means of Roll-off filters					
	1.0	0.4	0.4		0.4	
Carrier frequency of analog sound component	6.0 MHz FM mono	5.5 MHz FM mono	6.5 MHz AM mono		6.5 MHz FM mono	
			terrestrial	cable		
Power ratio between vision carrier and analog sound carrier	10 dB	13 dB	10 dB	16 dB	13 dB	
Power ratio between analog and modulated digital sound carrier	10 dB	7 dB	17 dB	11 dB	China/ Hungary	Poland
					12 dB	7 dB

Table 5–2: Summary of NICAM 728 sound coding characteristics

Characteristics	Values
Audio sampling frequency	32 kHz
Number of channels	2
Initial resolution	14 bit/sample
Companding characteristics	near instantaneous, with compression to 10 bits/sample in 32-samples (1 ms) blocks
Coding for compressed samples	2’s complement
Preemphasis	CCITT Recommendation J.17 (6.5 dB attenuation at 800 Hz)
Audio overload level	+12 dBm measured at the unity gain frequency of the preemphasis network (2 kHz)

5.2. A2-Systems

Table 5–3: Key parameters for A2 Systems of Standards B/G, D/K, and M

Characteristics	**Sound Carrier FM1**			**Sound Carrier FM2**		
TV-Sound Standard	**B/G**	**D/K**	**M**	**B/G**	**D/K**	**M**
Carrier frequency in MHz	5.5	6.5	4.5	5.7421875	6.2578125 6.7421875 5.7421875	4.724212
Vision/sound power difference	13 dB			20 dB		
Sound bandwidth	40 Hz to 15 kHz					
Preemphasis	50 µs		75 µs	50 µs		75 µs
Frequency deviation (nom/max)	±27/±50 kHz		±17/±25 kHz	±27/±50 kHz		±15/±25 kHz
Transmission Modes						
Mono transmission	mono			mono		
Stereo transmission	(L+R)/2		(L+R)/2	R		(L–R)/2
Dual sound transmission	language A			language B		
Identification of Transmission Mode						
Pilot carrier frequency				54.6875 kHz		55.0699 kHz
Max. deviation portion				±2.5 kHz		
Type of modulation / modulation depth				AM / 50%		
Modulation frequency				mono: unmodulated stereo: 117.5 Hz dual: 274.1 Hz		 149.9 Hz 276.0 Hz

5.3. BTSC-Sound System

Table 5–4: Key parameters for BTSC-Sound Systems

	Aural Carrier	BTSC-MPX-Components				
		(L+R)	Pilot	(L–R)	SAP	Prof. Ch.
Carrier frequency (f_{hNTSC} = 15.734 kHz) (f_{hPAL} = 15.625 kHz)	4.5 MHz	Baseband	f_h	2 f_h	5 f_h	6.5 f_h
Sound bandwidth in kHz		0.05 - 15		0.05 - 15	0.05 - 10	0.05 - 3.4
Preemphasis		75 µs		DBX	DBX	150 µs
Max. deviation to Aural Carrier	73 kHz (total)	25 kHz[1)]	5 kHz	50 kHz[1)]	15 kHz	3 kHz
Max. Freq. Deviation of Subcarrier Modulation Type				AM	10 kHz FM	3 kHz FM
[1)] Sum does not exceed 50 kHz due to interleaving effects						

5.4. Japanese FM Stereo System (EIA-J)

Table 5–5: Key parameters for Japanese FM-Stereo Sound System EIA-J

	Aural Carrier FM	EIA-J-MPX-Components		
		(L+R)	(L–R)	Identification
Carrier frequency (f_h = 15.734 kHz)	4.5 MHz	Baseband	2 f_h	3.5 f_h
Sound bandwidth		0.05 - 15 kHz	0.05 - 15 kHz	–
Preemphasis		75 µs	75 µs	none
Max. deviation portion to Aural Carrier	47 kHz	25 kHz	20 kHz	2 kHz
Max. Freq. Deviation of Subcarrier Modulation Type			10 kHz FM	60% AM
Transmitter-sided delay		20 µs	0 µs	0 µs
Mono transmission		L+R	–	unmodulated
Stereo transmission		L+R	L–R	982.5 Hz
Bilingual transmission		Language A	Language B	922.5 Hz

5.5. FM Satellite Sound

Table 5–6: Key parameters for FM Satellite Sound

Carrier Frequency	Maximum FM Deviation	Sound Mode	Bandwidth	Deemphasis
6.5 MHz	85 kHz	Mono	15 kHz	50 µs
7.02/7.20 MHz	50 kHz	Mono/Stereo/Bilingual	15 kHz	adaptive
7.38/7.56 MHz	50 kHz	Mono/Stereo/Bilingual	15 kHz	adaptive
7.74/7.92 MHz	50 kHz	Mono/Stereo/Bilingual	15 kHz	adaptive

5.6. FM-Stereo Radio

Table 5–7: Key parameters for FM-Stereo Radio Systems

	Aural Carrier	FM-Radio-MPX-Components			
		(L+R)	Pilot	(L–R)	RDS/ARI
Carrier frequency (f_p = 19 kHz)	10.7 MHz	Baseband	f_p	2 f_p	3 f_p
Sound bandwidth in kHz		0.05 - 15		0.05 - 15	
Preemphasis: – USA – Europe		 75 µs 50 µs		 75 µs 50 µs	
Max. deviation to Aural Carrier	75 kHz (100%)	90%[1)]	10%	90%[1)]	5%

[1)] Sum does not exceed 90% due to interleaving effects

6. Appendix B: Manual Mode

To adapt the modes of the STANDARD SELECT register to individual requirements, the MSP 44x8G offers a Manual Mode, which provides sophisticated programming of the MSP 44x8G.

The Manual Mode can be used only in those cases, where user specific requirements concerning detection, identification, or carrier positioning have to be met.

After the setting of the STANDARD SELECT register, the MSP 44x8G is set up for optimal behavior. **Therefore, it is not recommended to use the Manual mode.**

6.1. Demodulator Write and Read Registers for Manual Mode

In case of Automatic Sound Select (MODUS[0]=1), any modifications of all DCO registers listed in Table 6–1 are ignored.

Table 6–1: Demodulator Write Registers; Subaddress: 10_{hex}; these registers are not readable!

Demodulator Write Registers	Address (hex)	MSP-Version	Description	Reset Mode	Page
AUTO_FM/AM	00 21	4418, 4458	**1. MODUS[0]=1 (Automatic Sound Select):** Switching Level threshold of Automatic Switching between NICAM and FM/AM in case of bad NICAM reception **2. MODUS[0]=0 (Manual Mode):** Activation and configuration of Automatic Switching between NICAM and FM/AM in case of bad NICAM reception	00 00_{hex}	78
A2_Threshold	00 22		A2 Stereo Identification Threshold	01 90_{hex}	
CM_Threshold	00 24		Carrier-Mute Threshold	00 $2A_{hex}$	
DCO1_LO DCO1_HI DCO2_LO DCO2_HI	00 93 00 9B 00 A3 00 AB		**Note:** Modifications are ignored for Automatic Sound Select = on (MODUS[0]=1) Increment channel 1 Low Part Increment channel 1 High Part Increment channel 2 Low Part Increment channel 2 High Part	00 00_{hex}	81
Note: All registers except AUTO_FM/AM, A2_Threshold, and CM_Threshold are initialized during STANDARD SELECTION and are automatically updated when Automatic Sound Select (MODUS[0]=1) is on.					

Table 6–2: Demodulator Read Registers; Subaddress: 11_{hex}; these registers are not writable!

Demodulator Read Registers	Address (hex)	MSP-Version	Description	Page
C_AD_BITS	00 23	4418, 4458	NICAM-Sync bit, NICAM-C-Bits, and bit[2:0] of additional data bits	82
ADD_BITS	00 38		NICAM: bit[10:3] of additional data bits	82
CIB_BITS	00 3E		NICAM: CIB1 and CIB2 control bits	82
ERROR_RATE	00 57		NICAM error rate, updated with 182 ms	82

6.2. DSP Write and Read Registers for Manual Mode

Table 6–3: DSP-Write Registers; Subaddress: 12_{hex}, all registers are readable as well

Write Register	Address (hex)	Bits	Operational Modes and Adjustable Range	Reset Mode	Page
Additional Channel Matrix Modes	00 08 00 09 00 0A 00 41 00 0B 00 0C	[7:0]	[SUM/DIFF, AB_XCHANGE, PHASE_CHANGE_B, PHASE_CHANGE_A, A_ONLY, B_ONLY]	00_{hex}	83
FM Fixed Deemphasis	00 0F	[15:8]	[50 µs, 75 µs, J17, OFF]	OFF	83
FM Adaptive Deemphasis		[7:0]	[OFF, WP1]	OFF	83
Identification Mode	00 15	[7:0]	[B/G, M]	B/G	83

Table 6–4: DSP Read Registers; Subaddress: 13_{hex}, all registers are not writable

Additional Read Registers	Address (hex)	Bits	Output Range		Page
Stereo detection register for A2 Stereo Systems	00 18	[15:8]	[80_{hex} ... $7F_{hex}$]	8 bit two's complement	84
DC level readout FM1/Ch2-L	00 1B	[15:0]	[8000_{hex} ... $7FFF_{hex}$]	16 bit two's complement	84
DC level readout FM2/Ch1-R	00 1C	[15:0]	[8000_{hex} ... $7FFF_{hex}$]	16 bit two's complement	84

6.3. Manual Mode: Description of Demodulator Write Registers

6.3.1. Automatic Switching between NICAM and Analog Sound

In case of bad NICAM reception or loss of the NICAM-carrier, the MSP 44x8G offers an Automatic Switching (fall back) to the analog sound (FM/AM-mono), without the necessity for the controller of reading and evaluating any parameters. If a proper NICAM signal returns, switching back to this source is performed automatically as well. The feature evaluates the NICAM ERROR_RATE and switches, if necessary, all output channels which are assigned to the NICAM-source, to the analog source, and vice versa.

An appropriate hysteresis algorithm avoids oscillating effects (see Fig. 6–1). STATUS[9] and C_AD_BITS[11] (Addr: 0023 hex) provide information about the actual NICAM-FM/AM-status.

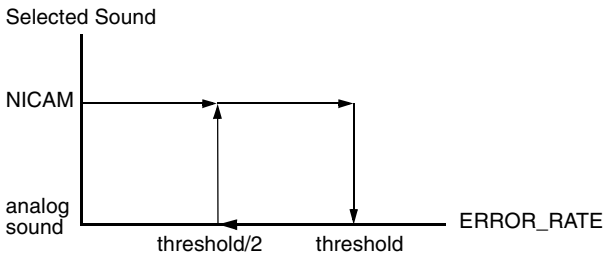


Fig. 6–1: Hysteresis for Automatic Switching

6.3.1.1. Function in Automatic Sound Select Mode

The Automatic Sound Select feature (MODUS[0]=1) includes the procedure mentioned above. By default, the internal ERROR_RATE threshold is set to 700_{dec}. i.e.:

– NICAM → analog Sound if ERROR_RATE > 700

– analog Sound → NICAM if ERROR_RATE < 700/2

The ERROR_RATE value of 700 corresponds to a BER of approximately $5.46*10^{-3}$ /s.

Individual configuration of the threshold can be done using Table 6–5. However, the internal setting used by the standard selection is recommended.

The optimum NICAM sound can be assigned to the MSP output channels by selecting one of the “Stereo or A/B”, “Stereo or A”, or “Stereo or B” source channels

6.3.1.2. Function in Manual Mode

If the manual mode (MODUS[0]=0) is required, the activation and configuration of the Automatic Switching feature has to be done as described in Table 6–6. Note, that the channel matrix of the corresponding output-channels must be set according to the NICAM-mode and need not to be changed in the FM/AM-fallback case.

Example:
Required threshold = 500: bits[10:1] = 00 1111 1010

Table 6–5: Coding of Automatic NICAM/Analog Sound Switching;
Automatic Sound Select is on (MODUS[0] = 1)

Mode	Description	AUTO_FM [11:0] Addr. = 00 21_{hex}	ERROR_RATE-Threshold/dec	Source Select: Input at NICAM Path[1)]
1 Default	Automatic Switching with **internal** threshold	bit[11:0] = 0	700	NICAM or FM/AM, depending on ERROR_RATE
2	Automatic Switching with **external** threshold (Customizing of Automatic Sound Select)	bit[11] = 0 bit[10:1] = 25...1000 = threshold/2 bit[0] = 1	set by customer; recommended range: 50...2000	
3	Forced Analog Mono	bit[11] = 1 bit[10:1] = ignored bit[0] = 1		always FM/AM

1) The NICAM path may be assigned to “Stereo or A/B”, “Stereo or A”, or “Stereo or B” source channels (see Table 2–2 on page 11).

Table 6–6: Coding of Automatic NICAM/Analog Sound Switching;
Automatic Sound Select is off (MODUS[0] = 0)

Mode	Description	AUTO_FM [11:0] Addr. = 00 21_{hex}	ERROR_RATE-Threshold/dec	Source Select: Input at NICAM Path
0 reset status	Forced NICAM (Automatic Switching disabled)	bit[11] = 0 bit[10:1] = 0 bit[0] = 0	none	always NICAM; Mute in case of no NICAM available
1	Automatic Switching with **internal** threshold (Default, if Automatic Sound Select is on)	bit[11] = 0 bit[10:1] = 0 bit[0] = 1	700	NICAM or FM/AM, depending on ERROR_RATE
2	Automatic Switching with **external** threshold (Customizing of Automatic Sound Select)	bit[11] = 0 bit[10:1] = 25...1000 = threshold/2 bit[0] = 1	set by customer; recommended range: 50...2000	
3	Forced Analog Mono (Automatic Switching disabled)	bit[11] = 1 bit[10:1] = 0 bit[0] = 1	none	always FM/AM

6.3.2. A2 Threshold

The threshold between Stereo/Bilingual and Mono Identification for the A2 Standard has been made programmable according to the user's preferences.

An internal hysteresis ensures robustness and stability.

Table 6–7: Write Register on I^2C Subaddress 10_{hex}: A2 Threshold

Register Address	Function	Name
THRESHOLDS		
00 22_{hex} (write)	**A2 THRESHOLD Register** Defines threshold of all A2 and EIA_J standards for Stereo and Bilingual detection bit[15:0] $07F0_{hex}$ force Mono Identification ... 0190_{hex} default setting after reset ... $00A0_{hex}$ minimum Threshold for stable detection recommended range: $00A0_{hex}$...$03C0_{hex}$	A2_THRESH

6.3.3. Carrier-Mute Threshold

The Carrier-Mute threshold has been made programmable according to the users preferences. An internal hysteresis ensures stable behavior.

Table 6–8: Write Register on I^2C Subaddress 10_{hex}: Carrier-Mute Threshold

Register Address	Function	Name
THRESHOLDS		
00 24_{hex} (write)	**Carrier-Mute THRESHOLD Register** Defines threshold for the carrier mute feature bit[15:0] 0000_{hex} Carrier-Mute always ON (both channels muted) ... $002A_{hex}$ default setting after reset ... $07FF_{hex}$ Carrier-Mute always OFF (both channels forced on) recommended range: 0014_{hex}...0050_{hex}	CM_THRESH

6.3.4. DCO-Registers

Note: The use of this register is not recommended. It should be used only in cases where non-standard carrier frequencies have to be processed. Please note, that the usage of user specific demodulation frequencies is not possible in combination with the Automatic Sound Select (MODUS[0]=1).

When selecting a TV-sound standard by means of the STANDARD SELECT register, all frequency tuning is performed automatically.

If manual setting of the tuning frequency is required, a set of 24-bit registers determining the mixing frequencies of the quadrature mixers can be written manually into the MSP. In Table 6–9, examples for DCO register programming are listed. It is necessary to separate these registers into two categories: low part and high part. The formula for the calculation of the INCR values for any chosen IF frequency is as follows:

$INCR_{dec} = int (f / fs \cdot 2^{24})$

with: int = integer function
f = IF frequency in MHz
f_S = sampling frequency (18.432 MHz)

Conversion of INCR into hex-format and separation of the 12-bit low and high parts lead to the required register values (DCO1_HI and _LO for MSP-Ch1, DCO2_HI and _LO for MSP-Ch2).

6.4. Manual Mode: Description of Demodulator Read Registers

Note: Using the STANDARD SELECTION register together with the STATUS register provides a more economic way to program the MSP 44x8G and to retrieve information from the MSP.

All registers except C_AD_BITs are 8 bits wide. They can be read out of the RAM of the MSP 44x8G.

All transmissions take place in 16-bit words. The valid 8-bit data are the 8 LSBs of the received data word.

If the Automatic Sound Select feature is not used, the NICAM or FM-identification parameters must be read and evaluated by the controller in order to enable appropriate switching of the channel select matrix of the baseband processing part. The FM-identification registers are described in Section 6.6.1. To handle the NICAM-sound and to observe the NICAM-quality, at least the registers C_AD_BITS and ERROR_RATE must be read and evaluated by the controller. Additional data bits and CIB bits, if supplied by the NICAM transmitter, can be obtained by reading the registers ADD_BITS and CIB_BITS.

Table 6–9: DCO registers for the MSP 44x8G; reset status: DCO_HI/LO = “00 00”

DCO1_LO 00 93_{hex}, DCO1_HI 00 $9B_{hex}$; DCO2_LO 00 $A3_{hex}$, DCO2_HI 00 AB_{hex}					
IF-Freq. [MHz]	**DCO_HI [hex]**	**DCO_LO [hex]**	**IF-Freq. [MHz]**	**DCO_HI [hex]**	**DCO_LO [hex]**
4.5	03 E8	00 00			
5.04 5.5 5.58 5.7421875	04 60 04 C6 04 D8 04 FC	00 00 03 8E 00 00 00 AA	5.76 5.85 5.94	05 00 05 14 05 28	00 00 00 00 00 00
6.0 6.2 6.5 6.552	05 35 05 61 05 A4 05 B0	05 55 0C 71 07 1C 00 00	6.6 6.65 6.8	05 BA 05 C5 05 E7	0A AA 0C 71 01 C7
7.02	06 18	00 00	7.2	06 40	00 00
7.38	06 68	00 00	7.56	06 90	00 00

6.4.1. NICAM Mode Control/Additional Data Bits Register

NICAM operation mode control bits and A[2:0] of the additional data bits.

Format:

MSB		C_AD_BITS 00 23_{hex}							LSB
11	...	7	6	5	4	3	2	1	0
Auto _FM	...	A[2]	A[1]	A[0]	C4	C3	C2	C1	S

Important: “S” = Bit[0] indicates correct NICAM-synchronization (S = 1). If S = 0, the MSP 4418/4458G has not yet synchronized correctly to frame and sequence, or has lost synchronization. The remaining read registers are therefore not valid. The MSP mutes the NICAM output automatically and tries to synchronize again as long as any NICAM standard is selected by the STANDARD SELECT register.

The operation mode is coded by C4-C1 as shown in Table 6–10.

Table 6–10: NICAM operation modes as defined by the EBU NICAM 728 specification

C4	C3	C2	C1	Operation Mode
0	0	0	0	Stereo sound (NICAMA/B), independent mono sound (FM1)
0	0	0	1	Two independent mono signals (NICAMA, FM1)
0	0	1	0	Three independent mono channels (NICAMA, NICAMB, FM1)
0	0	1	1	Data transmission only; no audio
1	0	0	0	Stereo sound (NICAMA/B), FM1 carries same channel
1	0	0	1	One mono signal (NICAMA). FM1 carries same channel as NICAMA
1	0	1	0	Two independent mono channels (NICAMA, NICAMB). FM1 carries same channel as NICAMA
1	0	1	1	Data transmission only; no audio
x	1	x	x	Unimplemented sound coding option (not yet defined by EBU NICAM 728 specification)
AUTO_FM: monitor bit for the AUTO_FM Status: 0: NICAM source is NICAM 1: NICAM source is FM				

Note: It is not necessary to read out and evaluate the C_AD_BITS. All evaluation is performed in the MSP and indicated in the STATUS register.

6.4.2. Additional Data Bits Register

Contains the remaining 8 of the 11 additional data bits. The additional data bits are not yet defined by the NICAM 728 system.

Format:

MSB		ADD_BITS 00 38_{hex}					LSB
7	6	5	4	3	2	1	0
A[10]	A[9]	A[8]	A[7]	A[6]	A[5]	A[4]	A[3]

6.4.3. CIB Bits Register

CIB bits 1 and 2 (see NICAM 728 specifications).

Format:

MSB		CIB_BITS 00 $3E_{hex}$					LSB
7	6	5	4	3	2	1	0
x	x	x	x	x	x	CIB1	CIB2

6.4.4. NICAM Error Rate Register

ERROR_RATE	00 57_{hex}
Error free	0000_{hex}
maximum error rate	$07FF_{hex}$

Average error rate of the NICAM reception in a time interval of 182 ms, which should be close to 0. The initial and maximum value of ERROR_RATE is 2047. This value is also active if no NICAM-standard is selected. Since the value is achieved by filtering, a certain transition time (approx. 0.5 sec) is unavoidable. Acceptable audio may have error rates up to a value of 700_{dec}. Individual evaluation of this value by the controller and an appropriate threshold may define the fallback mode from NICAM to FM/AM-Mono in case of poor NICAM reception.

The bit error rate per second (BER) can be calculated by means of the following formula:

$BER = ERROR\_RATE * 12.3*10^{-6} /s$

6.5. Manual Mode: Description of DSP Write Registers

6.5.1. Additional Channel Matrix Modes

Main Matrix	00 08_{hex}	L
Aux Matrix	00 09_{hex}	L
SCART1 Matrix	00 $0A_{hex}$	L
SCART2 Matrix	00 41_{hex}	L
I^2S Matrix	00 $0B_{hex}$	L
Quasi-Peak Detector Matrix	00 $0C_{hex}$	L
Mix1	00 38_{hex}	L
Mix2	00 38_{hex}	L
SUM/DIFF	0100 0000	40_{hex}
AB_XCHANGE	0101 0000	50_{hex}
PHASE_CHANGE_B	0110 0000	60_{hex}
PHASE_CHANGE_A	0111 0000	70_{hex}
A_ONLY	1000 0000	80_{hex}
B_ONLY	1001 0000	90_{hex}

This table shows additional modes for the channel matrix registers.

The sum/difference mode can be used together with the quasi-peak detector to determine the sound material mode. If the difference signal on channel B (right) is near to zero, and the sum signal on channel A (left) is high, the incoming audio signal is mono. If there is a significant level on the difference signal, the incoming audio is stereo.

6.5.2. FM Fixed Deemphasis

FM Deemphasis	00 $0F_{hex}$	H
50 µs	0000 0000 RESET	00_{hex}
75 µs	0000 0001	01_{hex}
J17	0000 0100	04_{hex}
OFF	0011 1111	$3F_{hex}$

Note: This register is initialized during STANDARD SELECTION and is automatically updated when Automatic Sound Select (MODUS[0]=1) is on.

6.5.3. FM Adaptive Deemphasis

FM Adaptive Deemphasis WP1	00 $0F_{hex}$	L
OFF	0000 0000 RESET	00_{hex}
WP1	0011 1111	$3F_{hex}$

Note: This register is initialized during STANDARD SELECTION and is automatically updated when Automatic Sound Select (MODUS[0]=1) is on.

6.5.4. NICAM Deemphasis

A J17 Deemphasis is always applied to the NICAM signal. It is not switchable.

6.5.5. Identification Mode for A2 Stereo Systems

Identification Mode	00 15_{hex}	L
Standard B/G (German Stereo)	0000 0000 RESET	00_{hex}
Standard M (Korean Stereo)	0000 0001	01_{hex}
Reset of Ident-Filter	0011 1111	$3F_{hex}$

To shorten the response time of the identification algorithm after a program change between two FM-Stereo capable programs, the reset of the ident-filter can be applied.

Sequence:

1. Program change
2. Reset ident-filter
3. Set identification mode back to standard B/G or M
4. Wait approx. 500 ms
5. Read stereo detection register

Note: This register is initialized during STANDARD SELECTION and is automatically updated when Automatic Sound Select (MODUS[0]=1) is on.

6.6. Manual Mode: Description of DSP Read Registers

All readable registers are 16-bit wide. Transmissions via I^2C bus have to take place in 16-bit words. Some of the defined 16-bit words are divided into low and high byte, thus holding two different control entities.

These registers are not writable.

6.6.1. Stereo Detection Register for A2 Stereo Systems

Stereo Detection Register	**00 18_{hex} H**
Stereo Mode	Reading (two's complement)
MONO	near zero
STEREO	positive value (ideal reception: $7F_{hex}$)
BILINGUAL	negative value (ideal reception: 80_{hex})

Note: It is not necessary to read out and evaluate the A2 identification level. All evaluation is performed in the MSP and indicated in the STATUS register.

6.6.2. DC Level Register

DC Level Readout FM1 (MSP-Ch2)	**00 $1B_{hex}$ H+L**
DC Level Readout FM2 (MSP-Ch1)	**00 $1C_{hex}$ H+L**
DC Level	[8000_{hex} ... $7FFF_{hex}$] values are 16 bit two's complement

The DC level register measures the DC component of the incoming FM signals (FM1 and FM2). This can be used for seek functions in satellite receivers and for IF FM frequencies fine tuning. If the DCO frequency is lower than the actuel carrier frequency, the resulting DC level will be positive, an dvia versa. In the audio signal the DC content is suppressed. The time constant τ, defining the transition time of the DC Level Register, is approximately 28 ms.

6.7. Demodulator Source Channels in Manual Mode

6.7.1. Terrestrial Sound Standards

Table 6–11 shows the source channel assignment of the demodulated signals in case of manual mode for all terrestrial sound standards. See Table 2–2 for the assignment in the Automatic Sound Select mode. In manual mode for terrestrial sound standards, only two demodulator sources are defined.

6.7.2. SAT Sound Standards

Table 6–12 shows the source channel assignment of the demodulated signals for SAT sound standards.

Table 6–11: Manual Sound Select Mode for Terrestrial Sound Standards

				Source Channels of Sound Select Block	
Broadcasted Sound Standard	**Selected MSP Standard Code**	**Broadcasted Sound Mode**	**FM Matrix**	**FM/AM** (use 0 for channel select)	**Stereo or A/B** (use 1 for channel select)
B/G-FM D/K-FM M-Korea M-Japan	03 04, 05 02 30	MONO	Sound A Mono	Mono	Mono
		STEREO	German Stereo Korean Stereo	Stereo	Stereo
		BILINGUAL, Languages A and B	No Matrix	Left = A Right = B	Left = A Right = B
B/G-NICAM L-NICAM I-NICAM D/K-NICAM D/K-NICAM (with high deviation FM)	08 09 0A 0B 0C, 0D	NICAM not available or NICAM error rate too high	Sound A Mono[1)]	analog Mono	no sound with AUTO_FM: analog Mono
		MONO	Sound A Mono[1)]	analog Mono	NICAM Mono
		STEREO	Sound A Mono[1)]	analog Mono	NICAM Stereo
		BILINGUAL, Languages A and B	Sound A Mono[1)]	analog Mono	Left = NICAM A Right = NICAM B
BTSC	20	MONO	Sound A Mono	Mono	Mono
		STEREO	Korean Stereo	Stereo	Stereo
		MONO + SAP	Sound A Mono	Mono	Mono
		STEREO + SAP	Korean Stereo	Stereo	Stereo
	21	MONO	Sound A Mono	Mono	Mono
		STEREO			
		MONO + SAP	No Matrix	Left = Mono Right = SAP	Left = Mono Right = SAP
		STEREO + SAP			
FM-Radio	40	MONO	Sound A Mono	Mono	Mono
		STEREO	Korean Stereo	Stereo	Stereo

[1)] Automatic refresh to Sound A Mono, do not write any other value to the register FM Matrix!

Table 6–12: Manual Sound Select Modes for SAT-reception (FM Matrix is set automatically)

				Source Channels of Sound Select Block for SAT-Modes			
Broadcasted Sound Standard	**Selected MSP Standard Code**	**Broadcasted Sound Mode**	**FM Matrix**	**FM/AM** (source select: 0)	**Stereo or A/B** (source select: 1)	**Stereo or A** (source select: 3)	**Stereo or B** (source select: 4)
FM SAT	$6, 50_{hex}$	MONO	Sound A Mono	Mono	Mono	Mono	Mono
	51_{hex}	STEREO	No Matrix	Stereo	Stereo	Stereo	Stereo
		BILINGUAL	No Matrix	Left = A (FM1) Right = B (FM2)	Left = A (FM1) Right = B (FM2)	A (FM1)	B (FM2)

7. Appendix C: Application Information

7.1. Exclusions of Audio Baseband Features

In general, all functions can be switched independently. Two exceptions exist:

1. NICAM cannot be processed simultaneously with secondary channel (see Fig. 2–3 and Fig. 2–2 on page 10).
2. FM adaptive deemphasis cannot be processed simultaneously with FM-identification.

7.2. Phase Relationship of Analog Outputs

The analog output signals: Main, Aux, and SCART2 all have the same phases. The SCART1 output has opposite phase.

Using the I^2S-outputs for other DSPs or D/A converters, care must be taken to adjust for the correct phase.

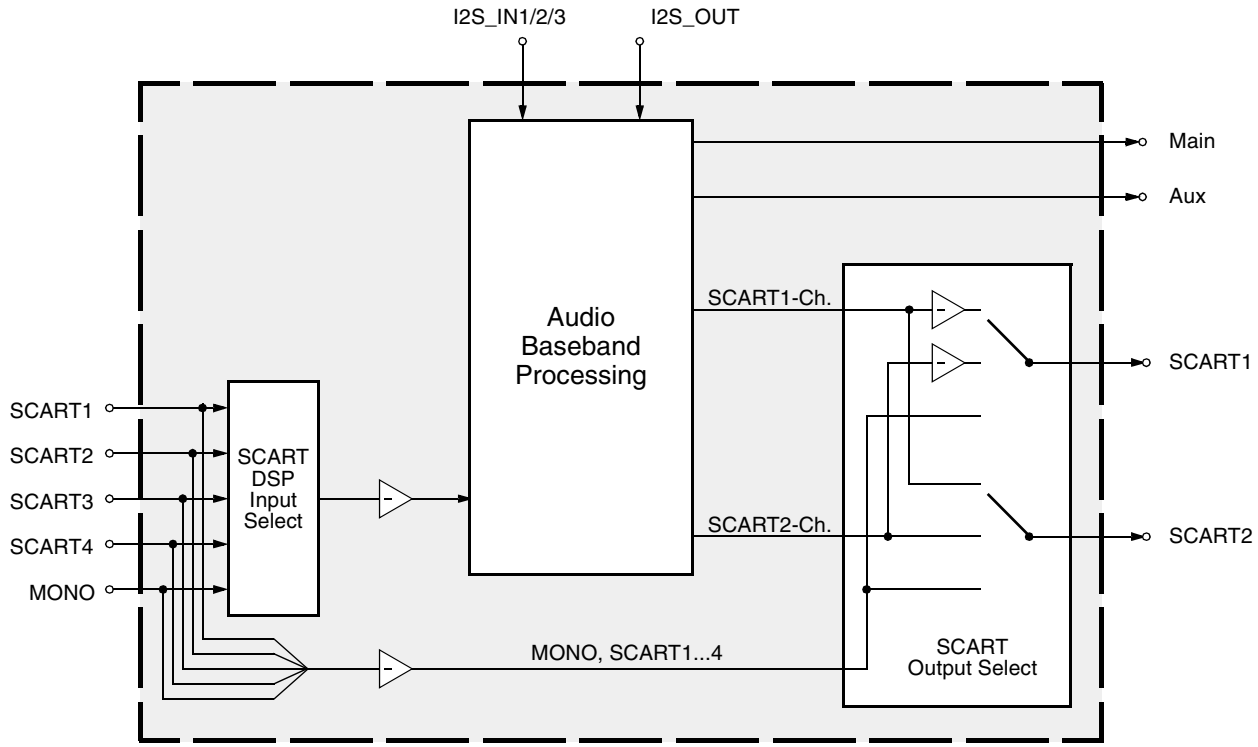
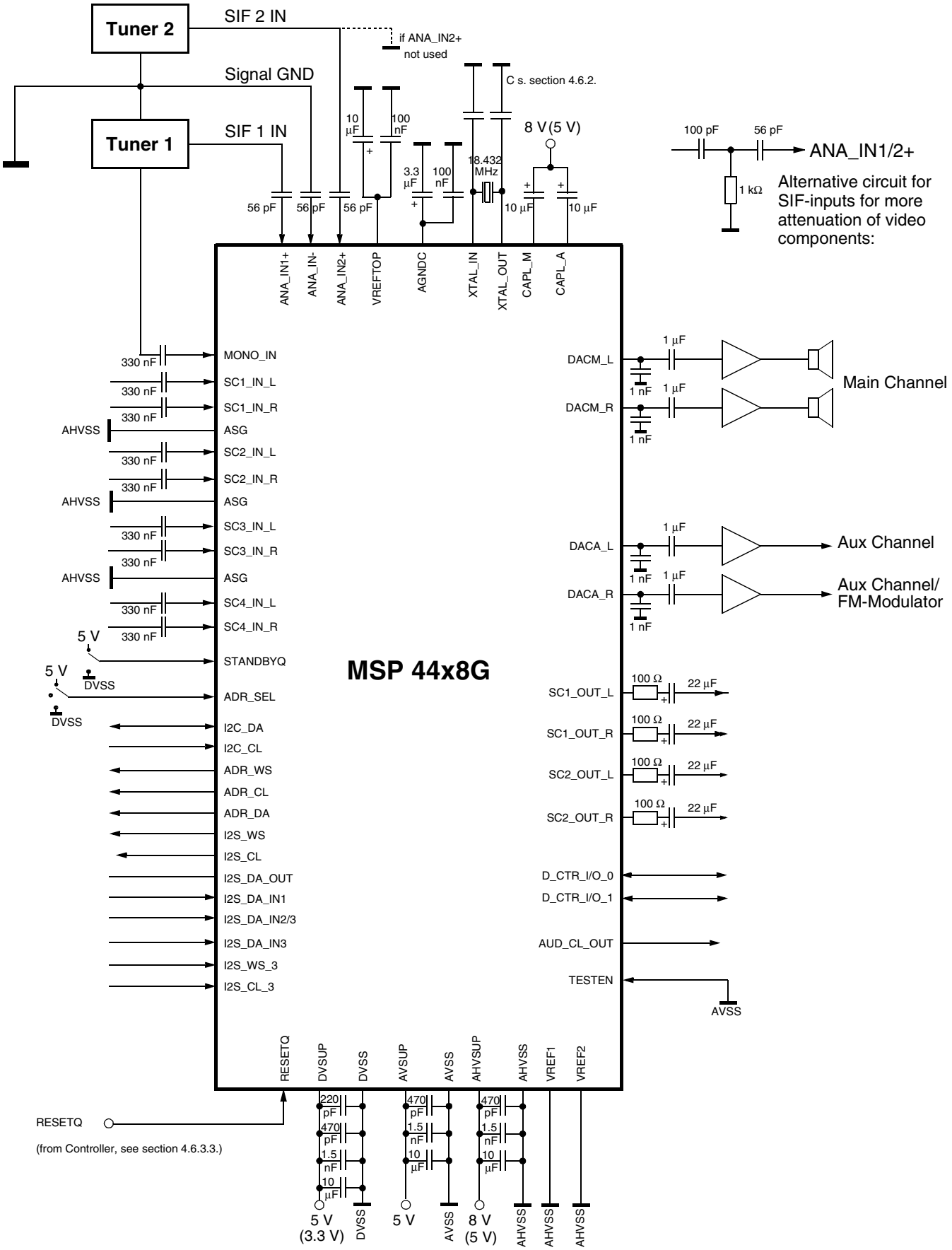


Fig. 7–1: Phase diagram of the MSP 44x8G

7.3. Application Circuit



8. Appendix D: MSP 44x8G Version History

MSP 44x8G-A1

First release

MSP 44x8G-A2

– J17 FM-deemphasis implemented

– input specification for RESETQ and TESTEN changed

MSP 44x8G-B3

– The Automatic Sound Select (ASS) malfunction has been corrected. In the previous version, under certain circumstances and depending on the processor load, e.g.: use of the asynchronous I^2S3 interface, the Automatic Sound Select Feature (ASS) did not work correctly.

– correction of 10 µs delay between Left and Right: In case of any Stereo output from the demodulator (FM/AM, ST or A/B) there was a constant time delay of 10 µs between Left and Right channel in the A1 and A2 versions.

– correction of default Scart-Switch configuration during power-up

– correction of unstable sound mode detection when the MSP reaches a specific higher case temperature

– correction of I2S output interface

9. Data Sheet History

1. : “MSP 44x8G Multistandard Sound Processor Family”, March 15, 2001, 6251-516-2PD. Second release of the . Major changes:

– specification for version A2 added (see Appendix D: Version History)

– I^2C-bus description changed

– ACB register: documentation for bit allocation D_CTR_I/O changed

2. Data Sheet: “MSP 44x8G Multistandard Sound Processor Family”, June 16, 2003, 6251-516-1DS. First release of the data sheet.Major changes:

– specification for version B3 added

– Section 4.1.: diagrams for all packages changed

– PLQFP64 changed to PMQFP64-2

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