Features

- **Initialization of the Program Memory by DMA via the User Extension Interface (8-bit or 16-bit data format possible) or via the Synchronous Serial Input Link 1 (16-bit data format),**
- **SRAM and DRAM support**
- **Write access protection**
- **40-bit User Extension interface**
- **Automatic conversion to and from a 32-bit data User Extension Interface**
- **Powerful 16-bit programmable versatile IO port featuring 2 input/output serial ports, up to 16-bit input/output parallel port, 4 pulse generators, 2 full duplex UART**
- **Four External interrupts**
- **Two 32-bit timers**
- **Watch Dog**
- **Two CRC accelerators (one for the input data stream, one for the output data stream)**
- **JTAG**
- **Maximum Operating frequency: 40MHz for ClkIn**
- **Power Consumption: 350 mA at 40MHz for ClkIn**
- **Latch Up immunity better than 100 MeV**
- **Designed on Atmel M62265E matrix sea of gates, into an MQFPF256**

Introduction

After Atmel successfully released the TSC21020F DSP, a code and pin compatible radiation hard version (including SEU hardening) of the ADI ADSP-21020, ASTRIUM have, under an ESA contract, developed a TSC21020F companion chip called DSP Peripheral Controller (DPC).

This DSP Peripheral Controller is a generic support device suitable for on-board applications using the TSC21020F processor. The device implements those support functions which are required for the integration of the processor with other devices in a board design.

It has been designed on the Atmel MG2RT Sea of Gates series, allowing to have a DPC chip hardened almost at the same level as the TSC21020F is, latch up and total dose wise.

The T7904E is now available from Atmel as a standard ASIC. It is available in a 256-pin MQFPF ceramic package.

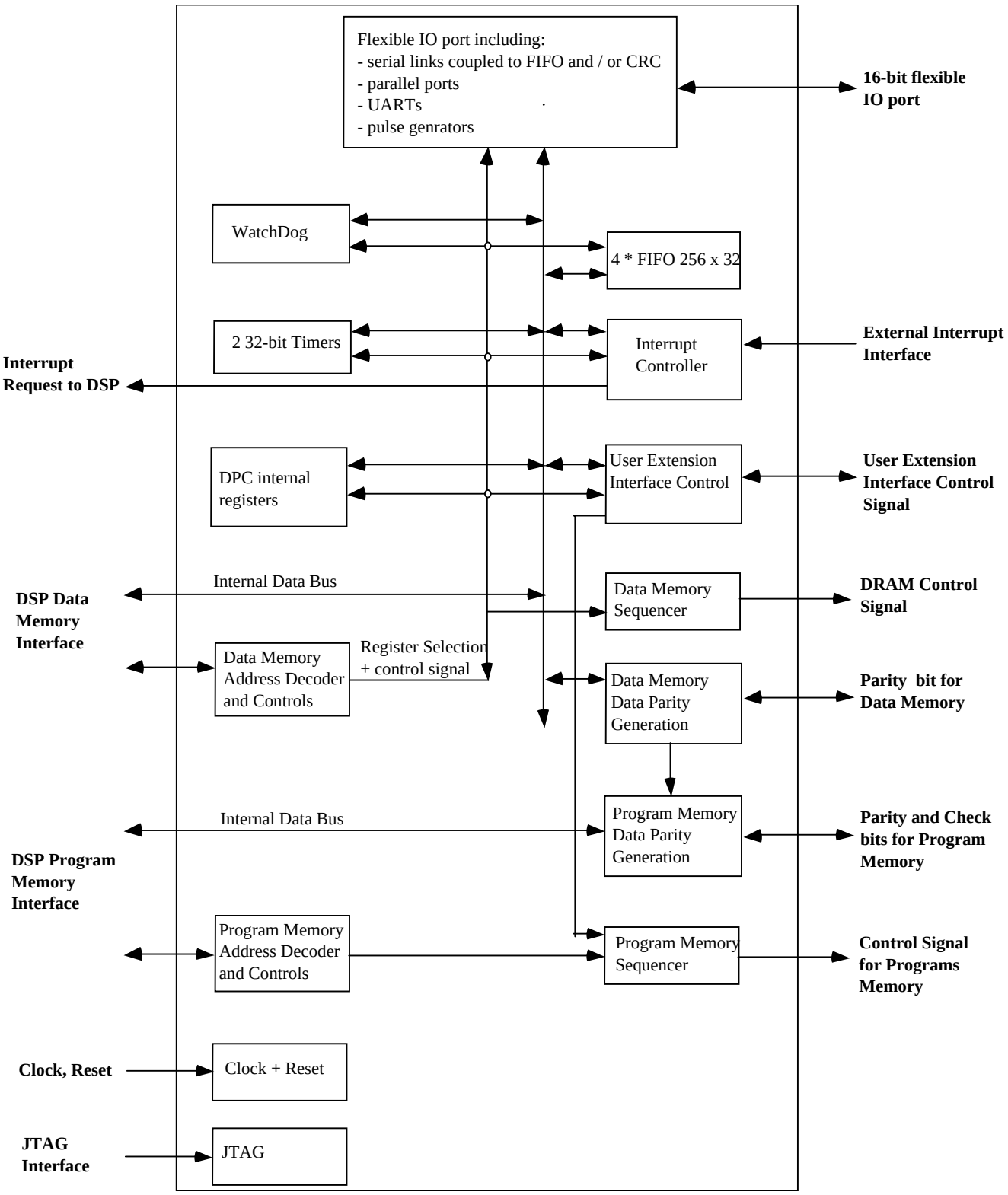
WIRELESS & µC

Radiation Tolerant DSP Peripheral Controller

T7904E

Rev. C–24-Aug-01

Figure 1. Functional block diagram of the T7904E



Typical DSP core architecture based on the T7904E

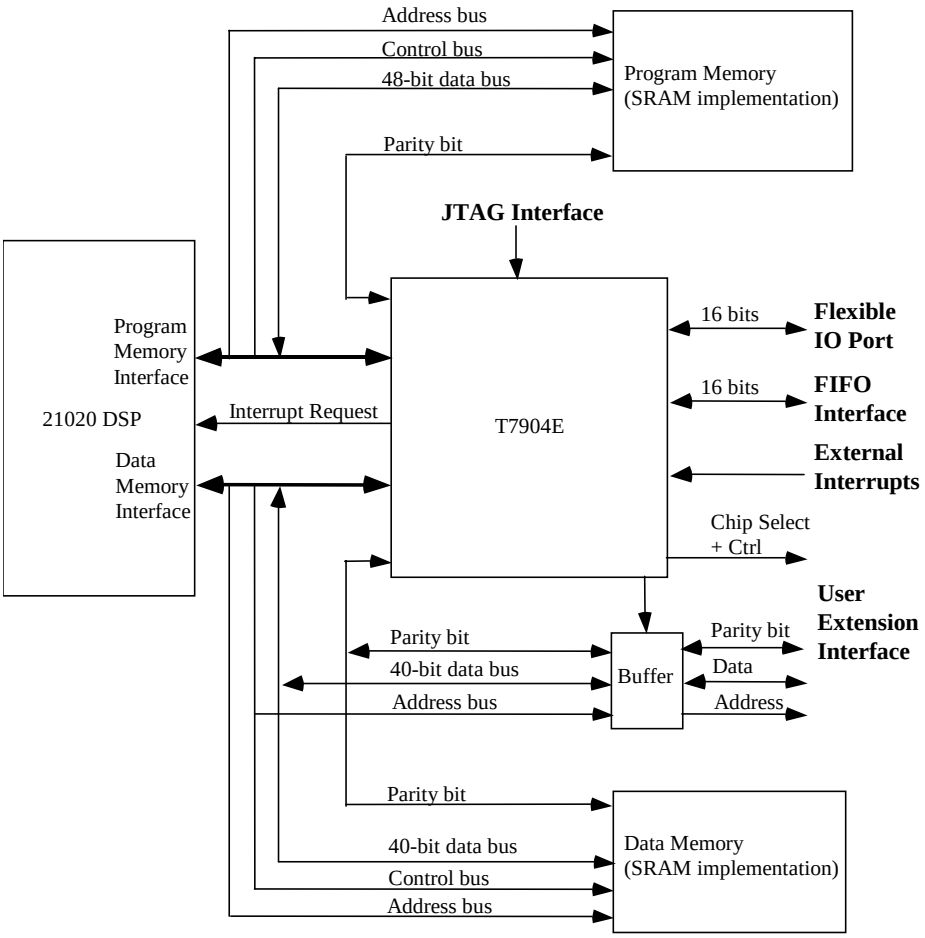
This section presents 2 typical DSP core architectures implementing the T7904E.

DSP Processor Core Architecture: SRAM implementation

This architecture is based on a parallel data bus approach. The DSP Processor core implements the following discrete circuits on a PCB:

- the TSC21020 DSP,
- the T7904E,
- SRAMs for both the Program Memory and the Data Memory (optional parity protection),
- transceivers on the address and data bus of the User Extension Interface (the control signal of this interface are directly generated by the T7904E).

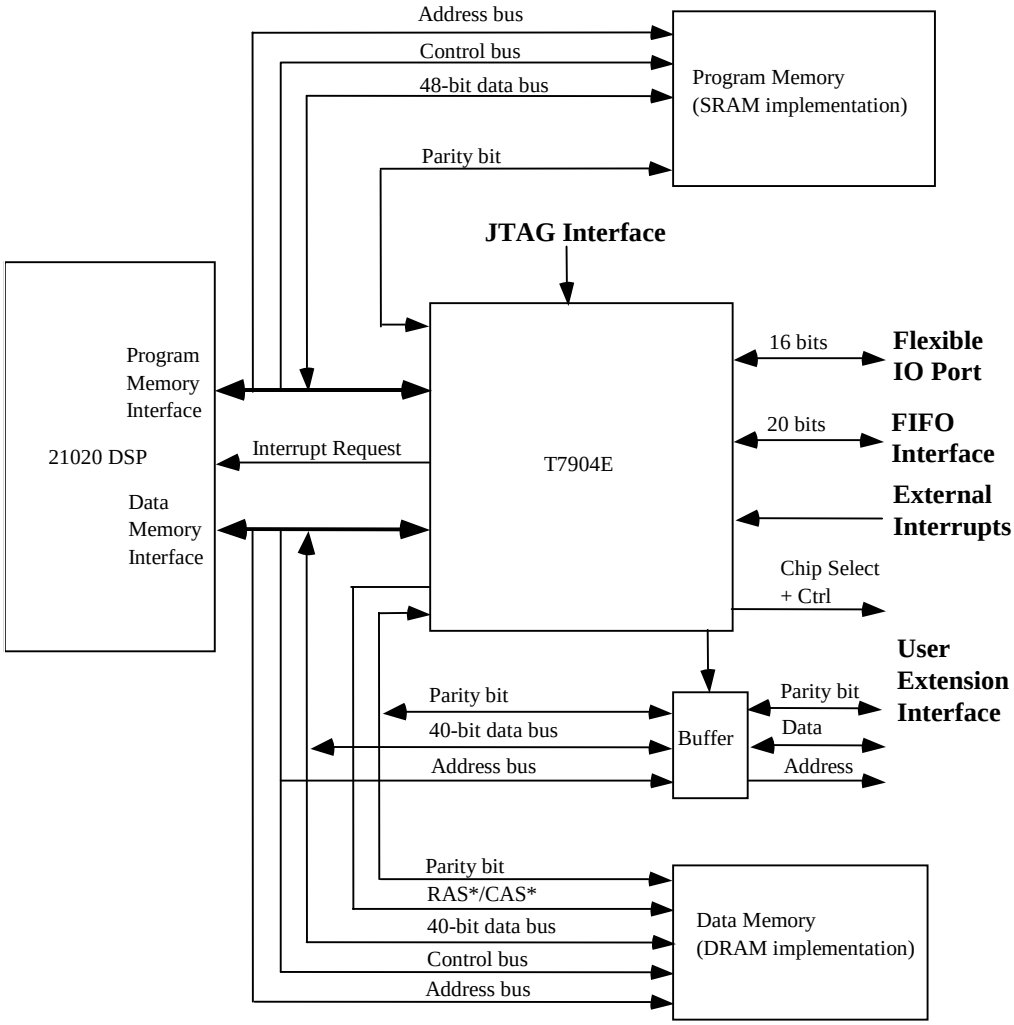
Figure 2. DSP Processor Core Architecture: SRAM implementation



DSP Processor Core Architecture: DRAM implementation

This architecture is quite similar to the previous one, except that the Data Memory (DMBANK0) is made up of DRAMs.

Figure 3. DSP Processor Core Architecture: DRAM implementation



Functional description

Program Memory initialization

- The T7904E can initialize the program memory according to a predefined configuration. The configuration is selected by reading the PMD(1-0) data bus in the last cycle of the reset phase:
  1. PMD(1-0) = 00: No Program Memory Initialization is performed by the T7904E,
  2. PMD(1-0) = 01: The Program Memory Initialization is done via the data bus DMD(15-8) of IO Area 0 for the flat package T7904E: 8-bit width,
  3. PMD(1-0) = 10: The Program Memory Initialization is done via the data bus DMD(23-8) of IO Area 0 for the flat package T7904E: 16-bit width,
  4. PMD(1-0) = 11: The Program Memory Initialization is done via the Synchronous Serial Input Link 1: 16-bit width.
- When the Program Memory Initialization is done via the IO Area 0 or via the Synchronous Serial Input Link 1, the 20 lsb of the first 6 x 8 bytes that are fetched, indicate the number of 48-bit words to be loaded in the Program Memory RAM. The least significant byte of the 48-bit words are fetched first. Each time a new byte is fetched, it is stored in the Program Register named PrgReg(47-0), the first byte in PrgReg(7-0), the second byte in PrgReg(15-8), the third byte in PrgReg(23-16), the fourth byte in PrgReg(31-24), the fifth byte in PrgReg(39-32) and the sixth byte in PrgReg(47-40). When 6 bytes are available in PrgReg, the T7904E performs a DMA access to write the content of PrgReg(47-0) into the Program Memory RAM.
- During the Program Memory initialization, the T7904E generates the parity bit PMPar over PMD(47-0) if required.
- As soon as the Program Memory initialization is completed, the DSP can set the bit SysAv in the General Configuration Register (GConfReg). The value of SysAv in GConfReg is reflected on the output signal SysAv to indicate the system is available.

Memory Organization

- The Data Memory interface is organized into 4 identical banks DMBANK0, DMBANK1, DMBANK2, DMBANK3 corresponding to the Data Memory banks defined in the TSC21020 User's manual:
  1. DMBANK0 is dedicated to the Data Memory RAM. The T7904E supports to implement DRAM devices or SRAM devices in the DMBANK0. DMBANK0 is a 40-bit data bus area,
  2. DMBANK1 provides 4 identical areas which size is 4Mwords for User Extensions. Each area is decoded by a specific selection signal IOSel*(3-0). The T7904E implements its internal registers in DMBANK1. DMBANK1 is a 40-bit data bus area except the T7904E internal register area which is a 32-bit data bus area,
  3. DMBANK2 and DMBANK3 are 40-bit data bus areas.
- The T7904E supports to perform a 32-bit data bus automatic conversion to and from 8-bit/16-bit data bus on the sub-areas IOArea0, IOArea1, IOArea2 and IOArea3 of DMANK1. The automatic conversion is enable by programming the General Configuration Register. The T7904E generates the DMAC(1-0) address bits during the automatic conversion. Only DMAC(1) is relevant in 16-bit mode. The 8-bit data bus device must be connected on DMD(15-8). The 16-bit data bus device must be connected on DMD(23-8).

Table 1. T7904E Program Memory mapping

Bank Designation	Address (hex)	Content	Features
PMBANK0	0 00000 0 FFFFF	Program Memory RAM (PMRAM0)	• 48-bit data bus • SRAM devices supported • Parity protection option • Write access protection if PMRAM1 not used • Failing address support if PMRAM1 not used • Accesses are performed in 1 clock cycle (+ 1 clock cycle for the write access if parity protection enable or write access protection is selected)
	1 00000 7 FFFFF	Program Memory RAM (PMRAM1)	• 48-bit data bus • SRAM devices supported • Parity protection option • Accesses are performed in 1 clock cycle (+ 1 clock cycle for the write access if parity protection)
PMBANK1	8 00000 8 FFFFF	Program Memory RAM	Same as PMRAM0
	9 00000 F FFFFF	Program Memory RAM	Same as PMRAM1

Table 2. T7904E Data Memory mapping

Bank Designation	Address (hex)	Content	Features
DMBANK0	00 000000 0 FFFFFF	Data Memory RAM (DMRAM0)	• 40-bit data bus • SRAM and DRAM devices supported • Parity protection option • Write access protection if DMRAM1 not used • Failing address support if DMRAM1 not used • Accesses are performed in 1 clock cycle (+ 1 clock cycle for the write access if parity protection enable or write access protection is selected or DRAM implemented)
	01 000000 1F FFFFFF	Data Memory RAM (DMRAM1)	• 40-bit data bus • SRAM devices supported • Parity protection option • Accesses are performed in 1 clock cycle (+ 1 clock cycle for the write access if parity protection enable)
DMBANK1	20 000000 20 3FFFFF	IO Area 0	• 40-bit data bus • 4Mwords supported • Parity protection option • Programmable wait-state • Programmable automatic conversion to and from 32-bit data bus width • Failing address support • Accesses are performed in 2 clock cycles + number of wait-states (+ 1 clock cycle for the write access if parity protection enable)
	20 400000 20 7FFFFF	IO Area 1	Same as IO Area 0
	20 800000 20 BFFFFF	IO Area 2	Same as IO Area 0 + Bus Ready Controlled
	20 C00000 20 FFFFFF	IO Area 3	Same as IO Area 0 + Bus Ready Controlled
	21 000000 3F FFFFFF	T7904E Internal Registers	• 32-bit data bus • Accesses are performed in 1 clock cycle • Internal Parity Protection
DMBANK2	40 000000 41 FFFFFF	Extended Area (EA20)	• 40-bit data bus • Programmable wait-state • Parity protection option • Failing address support • Accesses are performed in 2 clock cycles + number of wait-states (+ 1 clock cycle for the write access if parity protection enable)
	42 000000 7F FFFFFF	Extended Area (EA21)	Same as EA20 except no failing address support
DMBANK3	80 000000 81 FFFFFF	Extended Area (EA30)	Same as EA20
	82 000000 FF FFFFFF	Extended Area (EA31)	Same as EA21

Dynamic memory access

- The T7904E supports the DSP21020 to access DRAM devices in DMBANK0. The T7904E selects the DRAM or SRAM configuration by reading the PMD(2) data bus during the last cycle of the reset phase:
  1. PMD(2) = 0: SRAM implementation
  2. PMD(2) = 1: DRAM implementation.

- The page size of the DRAM devices is done by reading the PMD(5-4) data bus in the last cycle of the reset phase:
  1. PMD(5-4) = 00: 512 words,
  2. PMD(5-4) = 01: 1024 words,
  3. PMD(5-4) = 10: 2048 words,
  4. PMD(5-4) = 11: 4096 words.

- When the reset phase is completed, the T7904E generates 8 DMRAS* before proper DRAM operation is achieved.
- DMRAS* is generated for Data Memory page mode initialization when DMPAGE input signal is asserted. During a page mode initialization, the T7904E generates DMTS* in order to three state Data Memory Bus of the DSP21020 and also DMACK to hold on the DSP21020. The T7904E generates the DRAM address bus according to the page size selection:
  1. PMD(5-4) = 00: DRAM row addresses are on DMA(8-0),
  2. PMD(5-4) = 01: DRAM row addresses are on DMA(9-0),
  3. PMD(5-4) = 10: DRAM row addresses are on DMA(10-0),
  4. PMD(5-4) = 11: DRAM row addresses are on DMA(11-0)
- DMCAS* is generated during a fast page mode access for the Data Memory Data DRAMs.
- The T7904E generates DMDWr* to manage a delayed write cycle on the DRAM devices that store the Data and the check bits or the parity bit of the Data Memory Interface.
- The T7904E provides automatic DRAM refresh according to a CAS* before RAS* refresh cycle. The refresh cycle period is set by programming the General Configuration Register
- One implicit extra wait-state is inserted during a DRAM write access.

Memory protection

- The Program Memory RAMs (PMBANK0 and PMBANK1) and the Data Memory RAMs (DMBANK0) can be protected with a parity bit. The protection is selected by reading the PMD(7-6) data bus in the last cycle of the reset phase:
  1. PMD(7-6) = 00: No Parity protection,
  2. PMD(7-6) = 01: Parity protection,
  3. PMD(7-6) = 10: No Parity protection,
  4. PMD(7-6) = 11: No Parity protection.
- The Data Memory RAM (DMBANK1, DMBANK2, DMANK3) can be protected with a parity bit. The protection is enable by programming UEConfReg.
- Parity: The T7904E implements:

1. a 48-bit even parity generator/checker for PMBANK0, PMBANK1. PMPar is the parity bit over the Program Memory data bus,
2. a 40-bit even parity generator/checker for DMBANK0. DMPar is the parity bit over the Data Memory data bus,
3. a 40-bit even parity generator/checker for DMBANK 1, 2 and 3. DMPar is the parity bit over the Data Memory data bus.

In case of parity protection, the T7904E generates DMDWr* and PMDWr* during write accesses. In addition to that, the T7904E inserts one implicit wait state during the write accesses.

In case of a parity error in PMBANK0 or PMBANK1, the T7904E sets the PMDataError flag (IPReg(1)) if GConfReg(0) is 0 or resets the system if GConfReg(0) is 1. The T7904E stores the failing Program Memory address and bank in FPMAReg.

In case of a parity error in DMBANK0, DMBANK1, DMBANK2 or DMBANK3, the T7904E sets the DMDataError flag (IPReg(2)) if GConfReg(1) is 0 or reset the system if GConfReg(1) is 1. The T7904E stores the failing Program Memory address and bank in FDMAReg.

The error detection mechanism do not overwrite FDMAReg and FDMAReg registers until they have been read. FPMAReg and FDMAReg are reset only by SysReset* assertion.

Write access protection

- The Program Memory RAMs (PMBANK0 and PMBANK1) and the Data Memory RAMs (DMBANK0) can be protected against write accesses. The write protection is selected by reading the PMD(8) data bit in the last cycle of the reset phase:
  1. PMD(8) = 0: No write protection selected,
  2. PMD(8) = 1: Write protection selected.
- The T7904E can protect up to 4 zones in the Program Memory and/or in the Data Memory against write accesses. The area to protect against write access is defined on a 512 word basis area. Each zone is defined by 2 registers: the Access Protection Segment Base Register and the Access Protection Segment End Register that defines the beginning and the end of the area that must be protected
- When write access protection is selected, the T7904E generates DMDWr* and PMDWr* during the write accesses. In addition to that, the T7904E inserts one implicit wait state during write accesses.
- In case of a write access protection error in the Program Memory, the T7904E:
  1. stores the failing address in FPMAReg,
  2. sets the flag PMProtAreaError of the IPReg(3),
  3. do not generate PMDWr*.
- In case of a write access protection error in the Data Memory, the T7904E:
  1. stores the failing address in FDMAReg,
  2. sets the flag DMProtAreaError of the IPReg(4),
  3. do not generate DMDWr*.

User Extension Interface

The User Extension Interface is a 40-bit data interface which consists in:

1. The pre-decoded IO Area in DMBANK1: IO Area 0 selected by IOSel0*, IO Area 1 selected by IOSel1*, IO Area2 selected by IOSel2* and IO Area 3 selected by IOSel3*,
2. DMBANK2,
3. DMBANK3.

- The T7904E provides:
  1. a write signal UEWr* and a read signal UERd* to allow connection of user extensions on the User Extension Interface without any glue logic,
  2. a Ready signal UERdy2 (resp. UERdy3*) dedicated to IO Area2 (resp. IO Area3) for the users that require extended time in addition to the wait-states programmed in UEConfReg to complete an access,
  3. a user extension enable signal UEEn* to enable the external user extension buffers. UEEn* is generated when accessing IO Area0, IO Area 1, IO Area2, IO Area 3, DMBANK2 or DMBANK3.
- The T7904E provides UEConfReg register to program the number of wait states required for the IO Area 0 access, the IO Area 1 access, the IO Area 2 access, the IO Area 3 access, the DMBANK2 and the DMBANK3.
- A bus time out function of 256 system clocks is provided by the T7904E. The bus time out counter starts when the access is initiated in IOArea2 or IOArea3 (falling edge of DMRd* or DMWr*). If UERdy2 or UERdy3* are not asserted before 256 system clock cycles, the T7904E rises the flag BusTimeOut of the IPReg(9). The T7904E stores the failing Data Memory address in FDMAReg.

Watchdog

- The Watchdog function consists of a Watchdog Timer. It is possible to program the timer by setting a specific value in the Watchdog Program Register. The register consists of one scaler field (bit(23-16)) and one counter field (bit(15-0)) corresponding directly to the scaler field and to the counter field of the watchdog timer. Reading the Watchdog Program Register returns the current value of the counters.
- As soon as the Program Memory Initialization is completed, the timer is enabled and starts running with the default value of the scaler and of the counter. A 6-bit implicit pre-scaler is performed on the scaler. By writing the Trap Door Set Register after reset, the timer is disabled. After the disabling of the watchdog timer, a write operation in the Watchdog Program Register starts the counter counting with the value of the specified field. The Watchdog cannot be disabled when the Watchdog Program Register has been written.
- If the timer is refreshed by writing the Watchdog Program Register before the counter reaches zero, the timer restarts counting with the new delay value. If the timer is not refreshed before the counter reaches zero, then the flag WatchdogTimeOut is set in IPReg(0) and the timer restarts counting a time out period programmed in the field (31-24) of the Watchdog Program Register. Then if the timer is reprogrammed before the time out period elapses again, the timer restarts counting with the new delay value. But if the timer is not reprogrammed before the time-out period elapses, then reset is asserted.

Timer

- The T7904E provides 2 programmable timers. When enable, the timer decrements a 32-bit counter which starting value n is programmed in the Timer Program Register (TPReg). Once n ClkOut clock cycles are elapsed, the flag TimerExp1 (resp. TimerExp2) is set in IPReg(8) (resp. IPReg(12)).
- Each timer is controlled separately by programming the Timer Control Register (TCReg) :
    4. TCiEn of TCReg enables the counter to start counting.
    5. ReloadTCiEn selects the mode of the counter: Once n clock cycles are elapsed, either the timer is reloaded with the programmed value n in TPReg and then it restarts or the timer stops.
    6. LoadTCi restarts the timer with the programmed value in TPReg if the timer is enable.
- It is possible to cascade timer1 and timer2 if CascadeEnable is set in TCReg. In this configuration, timer1 is not set TimerExp1. The 64-bit timer sets TimerExp2 when the timer reaches zero. When the timer1 and timer2 are cascaded, the 64-bit timer is fully controlled by TC2En, ReloadTC2En and LoadTC2 of TCReg.

Versatile IO port

- The T7904E provides a versatile IO port on the VIOP(15-0) bus. It is possible to define VIOP(15-0) as:

1. 2 synchronous serial links (input and output),
2. 2 asynchronous serial links (input and output),
3. Up to 16-bit input port,
4. Up to 4-bit dynamic output port + 12-bit static output port.

- The configuration of the VIOP(15-0) is performed by programming the following internal registers:
    1. the serial link configuration register (SLConfReg),
    2. the parallel input port configuration register (PIPConfReg),
    3. the parallel output port configuration register (POPConfReg).
- For the configuration of VIOP(15-0), SLConfReg has the highest priority, then PIPConfReg, and last POPConfReg has the lowest priority. The SOL configuration bits in SLConfReg have a highest priority than the UART configuration bits.

Synchronous input serial link

- The T7904E provides 2 synchronous serial input links (SIL0 and SIL1) featuring an input data valid strobe (DVALI), an input clock (CKI) and an input data (DI) that are defined by SLConfReg. As soon as DVALI is de-asserted, the SIL is reset. The MSB is received first. 8, 16 and 32-bit data format are possible for the serial input links by programming SLConfReg.
- Depending on the programation of SLConfReg (16 bit or 32 bit serial link), when DVALI is de-asserted, the being received byte(s) are filled with zeros to get a 16 or 32-bit word.
- The T7904E provides the data register of the 2 input serial links named Serial Link Input Register 0 and Serial Link Input Register 1.
- It is possible to clear the Input serial link including the associated FIFO flag by programming the Serial Link Status Register (SLStatusReg).
- SIL0 is coupled to a 258 x 32 words FIFO named FIFO00. The flag Empty FIFO is set when FIFO00 is empty (no word has been received). The flag Full FIFO is set when FIFO00 is full.
- SIL1 can be coupled to a 258 x 32 word FIFO named FIFO10.

- An interrupt is generated when a word has been received on SIL1 and the flag Data Ready 1 in SLStatusReg is set.

Synchronous output serial link

- The T7904E provides 2 synchronous serial output links (SOL0 and SOL1) featuring an output data valid strobe (DVALO), an input data ready signal (DR), an output clock (CKO), an output data (DO) and an output abort data transfer signal (AT) that is defined by SLConfReg. The MSB is transmitted first. 8, 16 and 32-bit data format is possible for the serial output links by programming SLConfReg.
- The clock rate of the 2 synchronous serial output links is defined by the Serial Link Clock Configuration Register (SLCConfReg).
- It is possible to abort a data transfer of the output serial link by programming the Serial Link Status Register (SLStatusReg), then the output abort data transfer signal (AT) is asserted until a next transfer is initialized and the output serial link including the associated FIFO flag are reset.
- SOL0 is coupled with a 256 x 32 words FIFO named FIFO01. The flag Full FIFO is set when FIFO01 is full. The flag Empty FIFO is set when SOL0 has no word to send.
- SOL1 can be coupled to a 256 x 32 word FIFO named FIFO11.
- An interrupt is generated when a word has been sent by SOL1 and the flag Transmit Register Empty (TRE1) in SLStatusReg is set.

Parallel input port

- The T7904E provides up to 16 bit input port that are enabled by programming the Parallel Input Port Configuration Register (PIPConfReg).
- The T7904E provides the data register of the Parallel Input Port named Parallel Input Port Register.
- The input data must be asserted at least 2 ClkOut periods to be taken into account. An interrupt is generated when a change is detected on the parallel input port.

Parallel output port

- The T7904E provides up to 16-bit output port which consists in 4 independent pulse generators + 12 discret outputs.
- The output port is enabled by programming the Parallel Output Port Configuration Register (POPConfReg).
- It is possible to define each pulse generator as a one shot pulse generator or as a cyclic pulse generator by programming POPConfReg.
- It is possible to define the polarity of the pulse by programming the Parallel Output Port Polarity Register (POPPReg).
- The delay and the length of each pulse are programmable in the Pulse Delay Control Register and in the Pulse Length Control Register.
- The T7904E provides the Parallel Output Register that allows to start or restart each pulse generator. It is possible to read the value of the discrete output port through the Parallel Output Register.
- The pulse generator on VIOP(15) can count even if disable in the POPConfReg. The pulse generator on VIOP(15) set the flag IPReg(31) in the Interrupt Pending Register when the pulse is elapsed

UART

- The T7904E provides two full duplex Universal Asynchronous Receiver Transmitter (UART). The data format of the UARTs is 8-bit word. It is possible to choose between even or odd parity or no parity, and between one or two stop bits by programming the SLConfReg.

- It is possible to interface the UART through an 8-bit data register or 32-bit data by programming the SLConfReg.
- The baud rate of the UART is set by programming the SLConfReg.
- The T7904E provides a dedicated UART register for each UART (UARTReg1 associated to UART1, UARTReg2 associated to UART2).
- To output a byte on the serial output (LSB first), the following procedure must be followed. First, the UART Status Register (UARTStatusReg) must be read to check that the transmitter register is empty. Then the word (8-bit or 32-bit) to be output is written in the right UART Register (UARTReg1 or 2). The word will be then automatically converted in a serial form also adding start bit, parity bit and stop bit if required. When the word has been sent on the serial interface a flag UARTRxTx is set in IPReg(11).
- The receiver converts serial start bit, data word (LSB first), parity and stop bit into parallel form and loads the data (8-bit or 32-bit) in the right UARTReg. Framing error (FE), parity error (PE) and overrun error (OE) are indicated in the UART Status Register (UARTStatusReg) and rise the UARTError flag in IPReg(10). A correct received word is indicated by Data Ready bit in the UARTStatusReg. When a word is received on the serial interface, a flag UARTRxTx (IPReg(11)) is issued. When the UARTReg is read, the corresponding FE, PE, OE and DataReady flag in the UARTStatusReg are cleared.
- It is possible to clear an UART by writing the Clear UART bit in UARTStatusReg.
- The formula to calculate the value of the scaler is:

$$Scaler = \frac{ClockFrequency}{(16*Baudrate*(2-UBR))}$$

FIFO

- The T7904E provides 4 FIFOs named FIFO00, FIFO01, FIFO10 and FIFO11. FIFO00 is permanently coupled to SIL0, FIFO01 is permanently coupled to SOL0.
- Each FIFO provides an empty, half full and full flag. Each FIFO flag can rise a flag in the Interrupt Pending Register when set.
- The mode of the FIFO10 and FIFO11 is defined by the FIFO Configuration Register (FIFOConfReg). Bit 0 of FIFOConfReg has the highest priority in the configuration of FIFO10. Bit 3 of FIFOConfReg has the lowest priority in the configuration of FIFO10. Bit 4 of FIFOConfReg has the highest priority in the configuration of FIFO11. Bit 7 of FIFOConfReg has the lowest priority in the configuration of FIFO11. Bit 2 and 3 have a highest priority than bit 4 and 5.

Table 3. FIFO mode description

FIFO 10 Mode Description	FIFO 11 Mode Description
FIFO10 (258 words of 32bit) coupled to Synchronous Serial Input Link 1: • As soon as a word is received in SSIL 1, then the received word is written in FIFO10 if the FIFO is not full, • The FIFO is read by the DSP thanks to FIFOOutReg10.	FIFO11 (256 words of 32bit) coupled to Synchronous Serial Output Link 1: • FIFO11 is written by the DSP thanks to FIFOInReg11, • As long as the FIFO is not empty, the words are sent by SOL1.
FIFO10 (258 words of 32bit) in Stand alone Mode (Read and write operations performed by DSP): • FIFOInReg10 is controlled by DSP, • FIFOOutReg10 is controlled by DSP.	FIFO11 (258 words of 32bit) in Stand alone Mode (Read and write operations performed by DSP): • FIFOInReg11 is controlled by DSP, • FIFOOutReg11 is controlled by DSP.

CRC accelerator

- The T7904E provides 2 16-bit field cyclic redundant code (CRC) accelerators generated with the polynom $X^{16} + X^{12} + X^5 + 1$ with the shift register being initialized to all ones before processing each frame.
- The CRC accelerators are enabled when they are written (CRC0 register, CRC1 register). The CRC accelerators are initialized when they are read (CRC0 register, CRC1 register).

Table 4. CRC mode description

CRC 0 Mode Description	CRC 1 Mode Description
CRC0 linked to Synchronous Serial Input Link 0: As long as DVALI is asserted, the received bits plus the 16 check bits at SIL0 input are clocked into the input of the CRC accelerator. For an error-free block, the CRC contents must be zero. As soon as DVALI is de-asserted, the content of the CRC is stored in the CRC register and the CRC accelerator is initialized.	CRC1 linked to Synchronous Serial Output Link 0: As long as SOL0 input buffer is not empty, the CRC accelerator is fed by the SOL0 output. As soon as SOL0 input buffer is empty, the input of the CRC accelerator is clamped to zero and the 16 check bits are emitted without any gap.

Reset

- Reset* is generated on SysReset* assertion, on WatchDogReset, on Error Reset or by writing the Software Reset Register (SRReg). The reset cause is memorized in GConfReg(24-23). The Reset* signal is asserted at least 32 system clock cycles.
- The System Clock ClkOut is provided during reset phase.
- The SysAv bit GConfReg(22) is reset:
  1. When Reset* is asserted by the T7904E,
  2. When a non correctable error is detected in the Program Memory Bank or in the Data Memory Bank,
  3. When a write protection access is done in a write protected area,
  4. When an internal hardware error in detected in the T7904E.

Interrupts

- The T7904E provides:
  1. an Interrupt Pending Register (IPReg) that memorizes all the interrupt sources,
  2. an Interrupt Vector Register (IVReg) identifying among all the interrupts that are memorized in IPReg, the interrupt that has the highest priority (lsb). When IVReg is read, the corresponding interrupt is cleared in IPReg. As soon as a bit in IPReg is set high, the T7904E asserts IRQ* if the interrupt is not masked
  3. an Interrupt Mask Register (IMReg) that allows to mask each interrupt individually. A masked interrupt is set in IPReg but is not be prioritized in IVReg and do not assert IRQ*. When writing IPReg, the bit in IPReg that are equal to one resets the corresponding interrupt in IPReg
  4. an Interrupt Force Register (IFReg) that allows to force each interrupt individually.
- The T7904E provides 4 External Interrupts input signals that are monitored by IPReg. The external interrupts are edge or level sensitive programmable. It is possible to set the polarity of the external interrupts by programming GConfReg.

Table 5. Priority level of all the interrupt sources

Interrupt source	Priority level	Interrupt vector value
Watch Dog Time Out	0	0x00
Parity Error in PMBANK0.	1	0x08
Parity Error in DMBANK0, 1, 2 or 3.	2	0x10
Write Access Protection Error in PMBANK0.	3	0x18
Write Access Protection Error in DMBANK0.	4	0x20
Internal Hardware Error	5	0x28
External Interrupt 0	6	0x30
External Interrupt 1	7	0x38
Timer1 has expired	8	0x40
Bus Time Out Error on the User Extension Interface	9	0x48
UART Error	10	0x50
UARTRXTX : A data word has been correctly received by the UART or a word has been sent.	11	0x58
Timer2 has expired	12	0x60
External Interrupt 2	13	0x68
External Interrupt 3	14	0x70
Not defined	15	0x78
Not defined	16	0x80
A word has been correctly received or a word has been sent (Synchronous Serial Link 1)	17	0x88
A change has been detected on Parallel Input Port	18	0x90
EF00 Empty Flag of FIFO 00 (SSIL link0)	19	0x98
HF00 Half Full Flag of FIFO 00 (SSIL link0)	20	0xA0
FF00 Full Flag of FIFO 00 (SSIL link0)	21	0xA8
EF01 Empty Flag of FIFO 01 (SSOL link0)	22	0xB0
HF01 Half Full Flag of FIFO 01 (SSOL link0)	23	0xB8
FF01 Full Flag of FIFO 01 (SSOL link0)	24	0xC0
EF10 Empty Flag of FIFO 10	25	0xC8
HF10 Half Full Flag of FIFO 10	26	0xD0
FF10 Full Flag of FIFO 10	27	0xD8

Interrupt source	Priority level	Interrupt vector value
EF11 Empty Flag of FIFO 11	28	0xE0
HF11 Half Full Flag of FIFO 11	29	0xE8
FF11 Full Flag of FIFO 11	30	0xF0
Pulse Generator 15 elapsed	31	0xF8

Clock

- The External Input clock ClkIn is divided by 2 to get ClkOut.

JTAG

- The T7904E implements the boundary scan circuitry in compliance with IEEE Standard Test Access Port and Boundary-Scan Architecture.
- The boundary register is 629 bits long. The function of each position in the scan path is given in annex 1.

Register description

- All T7904E internal registers are parity protected. If an internal parity error is detected, then the T7904E sets the flag HWError (IPReg(5)) if GConfReg(2) is 0 or reset the system if GConfReg(2) is 1.
- It is possible to lock all the configuration registers of the T7904E by writing the lock register with all ones, and to unlock all the configuration registers of the T7904E by writing the lock register with all zero.
- The T7904E register address map is given in the following table.

Table 6. Register Description

T7904E Register	Address (hex)	Lock
Access Protection Segment 0 Base Register (APS0Breg)	21 000000	Possible
Access Protection Segment 1 Base Register (APS1Breg)	21 000001	Possible
Access Protection Segment 2 Base Register (APS2Breg)	21 000002	Possible
Access Protection Segment 3 Base Register (APS3Breg)	21 000003	Possible
Access Protection Segment 0 End Register (APS0EReg)	21 000004	Possible
Access Protection Segment 1 End Register (APS1EReg)	21 000005	Possible
Access Protection Segment 2 End Register (APS2EReg)	21 000006	Possible
Access Protection Segment 3 End Register (APS3EReg)	21 000007	Possible
General Configuration Register (GConfReg)	21 000008	Possible
UE Configuration Register (UEConfReg)	21 000009	Possible
Failing Data Memory Address Register (FDMAReg)	21 00000A	Possible
Failing Program Memory Address Register (FPMAReg)	21 00000B	Possible
Interruption Vector Register (IVReg)	21 00000C	Not Applicable
Interruption Pending Register (IPReg)	21 00000D	Possible
Interruption Mask Register (IMReg)	21 00000E	Possible
Interruption Force Register (IFReg)	21 00000F	Possible

T7904E Register	Address (hex)	Lock
Software Reset Register (SSReg)	21 000010	Not Possible
Timer 1 Program Register (T1Preg)	21 000011	Possible
Timer 2 Program Register (T2Preg)	21 000012	Possible
Timer Control Register (TCReg)	21 000013	Not Possible
Watchdog Program Register (WPReg)	21 000014	Not Possible
Watchdog Trap Door Set Register (WTDSReg)	21 000015	Not Possible
Serial Link Configuration Register (SLConfReg)	21 000016	Possible
Serial Link Clock Configuration Register (SLCConfReg)	21 000017	Possible
Parallel Input Port Configuration Register (PIPConfReg)	21 000018	Possible
Parallel Output Port Configuration Register (POPConfReg)	21 000019	Possible
Parallel Output Port Polarity Register (POPPReg)	21 00001A	Possible
Serial Link Input Register 0 (SLIReg0)	21 00001B	Not Applicable
Serial Link Input Register 1 (SLIReg1)	21 00001C	Not Applicable
Serial Link Output Register 0 (SLOReg0)	21 00001D	Not Possible
Serial Link Output Register 1 (SLOReg1)	21 00001E	Not Possible
Serial Link Status Register (SLStatusReg)	21 00001F	Not Possible
Parallel Input Port Register (PIPReg)	21 000020	Not Applicable
Parallel Output Port Register (POPReg)	21 000021	Not Possible
Lock Register	21 000022	Not Possible
Not defined	21 000023- 21 00002E	
Pulse Delay Control Register 12 (PDCReg 12)	21 00002F	Possible
Pulse Delay Control Register 13 (PDCReg 13)	21 000030	Possible
Pulse Delay Control Register 14 (PDCReg 14)	21 000031	Possible
Pulse Delay Control Register 15 (PDCReg 15)	21 000032	Possible
Not defined	21 000033-21 00003E	
Pulse Length Control Register 12 (PLCReg 12)	21 00003F	Possible
Pulse Length Control Register 13 (PLCReg 13)	21 000040	Possible
Pulse Length Control Register 14 (PLCReg 14)	21 000041	Possible
Pulse Length Control Register 15 (PLCReg 15)	21 000042	Possible
UART Receive Transmit Register 1 (UARTReg1)	21 000043	Not Possible
UART Receive Transmit Register 2 (UARTReg2)	21 000044	Not Possible
UART Status Register (UARTStatusReg)	21 000045	Not Possible
Not defined	21 000046	
CRC0 Register (CRCReg0)	21 000047	Not Possible
CRC1 Register (CRCReg1)	21 000048	Not Possible

T7904E Register	Address (hex)	Lock
FIFO Configuration Register (FIFOConfReg)	21 000049	Possible
FIFO 10 Input Register (FIFOInReg10)	21 00004A	Not Possible
FIFO 10 Output Register (FIFOOutReg10)	21 00004B	Not Applicable
FIFO 11 Input Register (FIFOInReg11)	21 00004C	Not Possible
FIFO 11 Output Register (FIFOOutReg11)	21 00004D	Not Applicable

Table 7. Access Protection Segment 0 Base Register (APS0Breg)

Bits	Name	Reset Value	Function	r/w
15-0	SegBase 0	0000	Start Address of the Access Protection Segment 0. Only the 11 lsb are relevant for the Program Memory Interface, SegBase0(15-12) must be set to " 0000 ".	r/w
16	Bank	0	Selection of the Memory BANK to protect : Program Bank when 0 Data Bank when 1	r/w
17	APE	0	Access Protection Enable when 1	r/w

Table 8. Access Protection Segment 1 Base Register (APS1Breg)

Bits	Name	Reset Value	Function	r/w
15-0	SegBase 1	0000	Start Address of the Access Protection Segment 1. Only the 11 lsb are relevant for the Program Memory Interface, SegBase1(15-12) must be set to " 0000 ".	r/w
16	Bank	0	Selection of the Memory BANK to protect : Program Bank when 0 Data Bank when 1	r/w
17	APE	0	Access Protection Enable when 1	r/w

Table 9. Access Protection Segment 2 Base Register (APS2Breg)

Bits	Name	Reset Value	Function	r/w
15-0	SegBase 2	0000	Start Address of the Access Protection Segment 2. Only the 11 lsb are relevant for the Program Memory Interface, SegBase2(15-12) must be set to " 0000 ".	r/w
16	Bank	0	Selection of the Memory BANK to protect : Program Bank when 0 Data Bank when 1	r/w
17	APE	0	Access Protection Enable when 1	r/w

Table 10. Access Protection Segment 3 Base Register (APS3Breg)

Bits	Name	Reset Value	Function	r/w
15-0	SegBase 3	0000	Start Address of the Access Protection Segment 3. Only the 11 lsb are relevant for the Program Memory Interface, SegBase3(15-12) must be set to " 0000 ".	r/w
16	Bank	0	Selection of the Memory BANK to protect : Program Bank when 0 Data Bank when 1	r/w
17	APE	0	Access Protection Enable when 1	r/w

Table 11. Access Protection Segment 0 End Register (APS0EReg)

Bits	Name	Reset Value	Function	r/w
15-0	SegEnd 0	0000	End Address of the Access Protection Segment 0. Only the 11 lsb are relevant for the Program Memory Interface.	r/w

Table 12. Access Protection Segment 1 End Register (APS1EReg)

Bits	Name	Reset Value	Function	r/w
15-0	SegEnd 1	0000	End Address of the Access Protection Segment 1. Only the 11 lsb are relevant for the Program Memory Interface.	r/w

Table 13. Access Protection Segment 2 End Register (APS2EReg)

Bits	Name	Reset Value	Function	r/w
15-0	SegEnd 2	0000	End Address of the Access Protection Segment 2. Only the 11 lsb are relevant for the Program Memory Interface.	r/w

Table 14. Access Protection Segment 3 End Register (APS3EReg)

Bits	Name	Reset Value	Function	r/w
15-0	SegEnd 3	0000	End Address of the Access Protection Segment 3. Only the 11 lsb are relevant for the Program Memory Interface.	r/w

Table 15. General Configuration Register (GConfReg)

Bits	Name	Reset Value	Function	r/w
0	IntOrRst0	0	Interrupt or reset in case of Parity Error in PMBANK0: 0 : Reset 1 : Interrupt	r/w
1	IntOrRst1	0	Interrupt or reset in case of Parity Error in DMBANK0, 1, 2 or 3 : 0 : Reset 1 : Interrupt	r/w
2	IntOrRst2	0	Interrupt or reset in case of Internal Parity Error: 0 : Reset 1 : Interrupt	r/w
4-3	ACIO0	00	32-bit Automatic Conversion on IO Area0 : 00 : No conversion 01 : 8-bit conversion 10 : 16-bit conversion 11 : No conversion	r/w
6-5	ACIO1	00	32-bit Automatic Conversion on IO Area1 : 00 : No conversion 01 : 8-bit conversion 10 : 16-bit conversion 11 : No conversion	r/w
8-7	ACIO2	00	32-bit Automatic Conversion on IO Area2 : 00 : No conversion 01 : 8-bit conversion 10 : 16-bit conversion 11 : No conversion	r/w
10-9	ACIO3	00	32-bit Automatic Conversion on IO Area3 : 00 : No conversion 01 : 8-bit conversion 10 : 16-bit conversion 11 : No conversion	r/w
11	EISM0	0	External Interrupt 0 sensitivity mode 0 : level sensitive 1 : edge sensitive	r/w
12	EISM1	0	External Interrupt 1 sensitivity mode 0 : level sensitive 1 : edge sensitive	r/w
13	EISM2	0	External Interrupt 2 sensitivity mode 0 : level sensitive 1 : edge sensitive	r/w
14	EISM3	0	External Interrupt 3 sensitivity mode 0 : level sensitive 1 : edge sensitive	r/w

Bits	Name	Reset Value	Function	r/w
15	EIPM0	0	External Interrupt 0 polarity mode 0 : Falling edge or low level active 1 : Rising edge or high level active	r/w
16	EIPM1	0	External Interrupt 1 polarity mode 0 : Falling edge or low level active 1 : Rising edge or high level active	r/w
17	EIPM2	0	External Interrupt 2 polarity mode 0 : Falling edge or low level active 1 : Rising edge or high level active	r/w
18	EIPM3	0	External Interrupt 3 polarity mode 0 : Falling edge or low level active 1 : Rising edge or high level active	r/w
19	MPE	0	Memory Protection Enable for the Program Memory and DMBANK0 : 0 : the memory protection is done according to PMD(7-6) 1 : disable the memory protection.	r/w
21-20	DRP	11	DRAM refresh period : 00 : Refresh is performed every 160 clock periods 01 : Refresh is performed every 128 clock periods 10 : Refresh is performed every 96 clock periods 11 : Refresh is performed every 64 clock periods	r/w
22	SysAv	0	System available when high	r/w
24-23	Reset Cause		Reset Cause : 00 : System Reset 01 : Error Reset 10 : Watch Dog Reset 11 : Software Reset	r

Table 16. UE Configuration Register (UEConfReg)

Bits	Name	Reset Value	Function	r/w
1-0	POIO0	00	Protection Option for the IO Area 0 : 00 : No Parity protection 01 : Parity protection 10 : No Parity protection 11 : No Parity protection	r/w
3-2	POIO1	00	Protection Option for the IO Area 1 : 00 : No Parity protection 01 : Parity protection 10 : No Parity protection 11 : No Parity protection	r/w
5-4	POIO2	00	Protection Option for the IO Area 2 : 00 : No Parity protection 01 : Parity protection 10 : No Parity protection 11 : No Parity protection	r/w
7-6	POIO3	00	Protection Option for the IO Area 3 : 00 : No Parity protection 01 : Parity protection 10 : No Parity protection 11 : No Parity protection	r/w
9-8	PODMB2	00	Protection Option for the DMBank2 : 00 : No Parity protection 01 : Parity protection 10 : No Parity protection 11 : No Parity protection	r/w
11-10	PODMB3	00	Protection Option for the DMBank3 : 00 : No Parity protection 01 : Parity protection 10 : No Parity protection 11 : No Parity protection	r/w
14-12	WSIO0	111	Wait State Number for the IO Area 0	r/w
17-15	WSIO1	000	Wait State Number for the IO Area 1	r/w
20-18	WSIO2	000	Wait State Number for the IO Area 2	r/w
23-21	WSIO3	000	Wait State Number for the IO Area 3	r/w
26-24	WSB2	000	Wait State Number for the DMBANK 2	r/w
29-27	WSB3	000	Wait State Number for the DMBANK 3	r/w

Table 17. Failing Data Memory Address Register (FDMAReg)

Bits	Name	Reset Value	Function	r/w
24-0	FDMA	0000000	Failing Data Memory Address	r/w
26-25	FDMBK	00	Failing Data Memory Bank : 00 : Bank 0 01 : Bank 1 10 : Bank 2 11 : Bank 3	r/w

Table 18. Failing Program Memory Address Register (FPMAReg)

Bits	Name	Reset Value	Function	r/w
19-0	FPMA	00000	Failing Program Memory Address	r/w
20	FDMBK	0	Failing Program Memory Bank : 0 : Bank 0 1 : Bank 1	r/w

Table 19. Interruption Pending Register (IPReg)

Bits	Name	Reset Value	Function	r/w
0	WatchDogTimeOut	0	Generated by the WatchDog when the counter has elapsed.	r
1	PMDataError	0	Parity Error in Program Memory.	r
2	DMDataError	0	Parity Error in Data Memory.	r
3	PMProtAreaError	0	Access Protection Error in Program Memory.	r
4	DMProtAreaError	0	Access Protection Error in Data Memory.	r
5	HWError	0	Internal Hardware Error.	r
6	ExtIt0	0	External interrupt 0.	r
7	ExtIt1	0	External interrupt 1.	r
8	Timer 1	0	Generated by the Timer 1 when it reaches zero.	r
9	BusTimeOutError	0	Bus Time Out Error. No Ready has been received.	r
10	UARTError	0	Generated by the UARTs if an error is detected.	r
11	UARTRxTx	0	Generated by the UARTs each time a word has been correctly received or sent.	r
12	Timer 2	0	Interrupt generated by the Timer 2 when it reaches zero.	r
13	ExtIt2	0	External interrupt 2.	r
14	ExtIt3	0	External interrupt 3.	r
15	Not defined	0		r
16	Not defined	0		r
17	SSLRxTx	0	Generated by the synchronous serial link 1 when a word has been correctly received or sent.	r
18	PIC	0	Parallel Input Port Change.	r
19	EF00	1	Empty Flag FIFO 00 (SSIL link0).	r
20	HF00	0	Half Full Flag FIFO 00 (SSIL link0).	r
21	FF00	0	Full Flag FIFO 00 (SSIL link0).	r
22	EF01	1	Empty Flag FIFO 01 (SSOL link0).	r
23	HF01	0	Half Full Flag FIFO 01 (SSOL link0).	r
24	FF01	0	Full Flag FIFO 01 (SSOL link0).	r
25	EF10	1	Empty Flag of FIFO 10.	r
26	HF10	0	Half Full Flag of FIFO 10.	r

Bits	Name	Reset Value	Function	r/w
27	FF10	0	Full Flag of FIFO 10.	r
28	EF11	1	Empty Flag of FIFO 11.	r
29	HF11	0	Half Full Flag of FIFO 11.	r
30	FF11	0	Full Flag of FIFO 11.	r
31	GP15	0	Pulse Generator 15 interrupt.	r

Table 20. Interruption Mask Register (IMReg)

Bits	Name	Reset Value	Function	r/w
31-0	IM	FFFF	Masked interrupts : bit 0 = 0 : IPReg(0) is not masked bit 0 = 1 : IPReg(0) is masked ..... bit 31 = 0 : IPReg(31) is not masked bit 31 = 1 : IPReg(31) is masked	r/w

Table 21. Interruption Force Register (IFReg)

Bits	Name	Reset Value	Function	r/w
31-0	IF	0000	Forced interrupts : bit 0 = 0 : no action bit 0 = 1 : IPReg(0) is set ..... bit 31= 0 : no action bit 31 = 1 : IPReg(31) is set	w

Software Reset Register (SSReg)

Write only register. Writing this register asserts Reset*

Table 22. Timer 1 Program Register (T1PReg)

Bits	Name	Reset Value	Function	r/w
31-0	TC1	0xFFFFFFFF	Programmed value of the down counting 32-bit counter 1	w

Reading **T1PReg** returns the current value of the counter.

Table 23. Timer 2 Program Register (T2PReg)

Bits	Name	Reset Value	Function	r/w
31-0	TC2	0xFFFFFFFF	Programmed Value of the down counting 32-bit counter 2	w

Reading **T2PReg** returns the current value of the counter.

Table 24. Timer Control Register (TCReg)

Bits	Name	Reset Value	Function	r/w
0	TC1En	0	Timer Counter 1 Enable : 1 : Enable counting 0 : Hold Timer Counter Value	r/w
1	ReloadTC1En	0	Timer Counter 1 Reload Enable : 1 : Reload Counter when zero and restart 0 : Stop Counter when zero	r/w
2	LoadTC1	0	Timer Counter 1 Load : 1 : Load Counter with programmed value and restart if enable 0 : No function	w
3	TC2En	0	Timer Counter 2 Enable : 1 : Enable counting 0 : Hold Timer Counter Value	r/w
4	ReloadTC2En	0	Timer Counter 2 Reload Enable : 1 : Reload Counter when zero and restart 0 : Stop Counter when zero	r/w
5	LoadTC2	0	Timer Counter 2 Load : 1 : Load Counter with programmed value and restart if enable 0 : No function	w
6	Cascade	0	Cascade Timer 1 and Timer 2 to made a 64-bits timer when 1 (Timer 1 LSB, Timer 2 MSB)	r/w

Table 25. Watchdog Program Register (WPReg)

Bits	Name	Reset Value	Function	r/w
15-0	WDC	FFFF	Preset 16-bit counter value	r/w
23-16	WDS	FF	Preset 8-bit scaler value	r/w
31-24	WDR	FF	Preset 8-bit reset counter value	r/w

Reading **WPReg** returns the current value of the counter.

Watchdog Trap Door Set Register (WTDSReg)

Write only register with any data. Writing this register after reset but before the watchdog has elapsed will disable the watchdog. The watchdog will stay disabled until it is reprogrammed by writing WPReg

Table 26. Serial Link Configuration Register (SLConfReg)

Bits	Name	Reset Value	Function	r/w
0	PROTO0	0	Protocol selection of Serial Link 0 : 0 : not TTC-B01 1 : Slave TTC-B01	r/w
2-1	SSIL0	00	Synchronous Serial Input Link 0 Definition : 00 : Serial Input Link 0 disable 01 : 8-bit Serial Input Link 0 enable 10 : 16-bit Serial Input Link 0 enable 11 : 32-bit Serial Input Link 0 enable VIOP(0) : DVALI0 (input data valid strobe) VIOP(1) : CKI0 (input clock) VIOP(2) : DI0 (input data)	r/w
3	Not defined	0		r/w
5-4	SSIL1	10	Synchronous Serial Input Link 1 Definition : 00 : Serial Input Link 1 disable 01 : 8-bit Serial Input Link 1 enable 10 : 16-bit Serial Input Link 1 enable 11 : 32-bit Serial Input Link 1 enable VIOP(3) : DVALI1 (input data valid strobe) VIOP(4) : CKI1 (input clock) VIOP(5) : DI1 (input data)	r/w
7-6	SSOL0	00	Synchronous Serial Output Link 0 Definition : 00 : Serial Output Link 0 disable 01 : 8-bit Serial Output Link 0 enable 10 : 16-bit Serial Output Link 0 enable 11 : 32-bit Serial Output Link 0 enable VIOP(6) : DVALO0 (output data valid strobe) VIOP(7) : DR0 (input data ready strobe) VIOP(8) : CKO0 (output clock) VIOP(9) : DO0 (output data) VIOP(10) : AT0 (output abort data transfer)	r/w
9-8	SSOL1	00	Synchronous Serial Output Link 1 Definition : 00 : Serial Output Link 1 disable 01 : 8-bit Serial Output Link 1 enable 10 : 16-bit Serial Output Link 1 enable 11 : 32-bit Serial Output Link 1 enable VIOP(11) : DVALO1 (output data valid strobe) VIOP(12) : DR1 (input data ready strobe) VIOP(13) : CKO1 (output clock) VIOP(14) : DO1 (output data) VIOP(15) : AT1 (output abort data transfer)	r/w

Bits	Name	Reset Value	Function	r/w
10	UARTMODE	0	UART Mode : 0 : 8-bit data interface 1 : 32-bit data interface	r/w
11	UART 1	0	Asynchronous Serial Link 1 Enable 0 : disable 1 : enable VIOP(11) : Receive Data Channel VIOP(12) : Transmit Data Channel	r/w
12	UART 2	0	Asynchronous Serial Link 2 Enable 0 : disable 1 : enable VIOP(13) : Receive Data Channel VIOP(14) : Transmit Data Channel	r/w
13	UBR	0	UART baud rate. 0 : divide UART scaler baud rate by 2 1 : No change of UART scaler baud rate	r/w
14	UPE	1	UART parity enable. 0 : no parity 1 : parity enable	r/w
15	UP	1	UART parity. 0 : even parity 1 : odd parity	r/w
16	USB	0	UART stop bit. 0 : one stop bit 1 : two stop bits	r/w
24-17	Scaler	00000001	UART scaler	r/w

Table 27. Serial Link Clock Configuration Register (SLCConfReg)

Bits	Name	Reset Value	Function	r/w
3-0	SSLPS0	0001	Synchronous Serial Link Prescaler 0	r/w
11-4	SSLS0	00000001	Synchronous Serial Output Link Scaler 0	r/w
15-12	SSLPS1	0001	Synchronous Serial Link Prescaler 1	r/w
23-16	SSLS1	00000001	Synchronous Serial Output Link Scaler 1	r/w

Table 28. Parallel Input Port Configuration Register (PIPConfReg)

Bits	Name	Reset Value	Function	r/w
15-0	PIBE	0x0000	Parallel Input Bit Enable • 0 VIOP corresponding bit disable • 1 VIOP corresponding bit enable Parallel port can be defined on VIOP(15-0)	r/w

Table 29. Parallel Output Port Configuration Register (POPConfReg)

Bits	Name	Reset Value	Function	r/w
15-0	POBE	0x0000	Parallel Output Bit Enable 0 VIOP corresponding bit disable 1 VIOP corresponding bit enable Parallel port can be defined on VIOP(15-0)	r/w
27-16	Not defined	0x000		r
31-28	POBM	0x0	Parallel Output Bit Mode 0 One shot pulse 1 Cyclic pulse generator	r/w

Table 30. Parallel Output Port Polarity Register (POPPReg)

Bits	Name	Reset Value	Function	r/w
11-0	Not defined	0x000		r
15-12	POPP	0x0	Parallel Output Port Polarity 0 Pulse not inverted 1 Pulse inverted	r/w

Table 31. Serial Link Input Register 0 (SLIReg0)

Bits	Name	Reset Value	Function	r/w
31-0	SLIReg0	0x00000000	Data Register of Serial Input Link 0	r

Table 32. Serial Link Input Register 1 (SLIReg1)

Bits	Name	Reset Value	Function	r/w
31-0	SLIReg1	0x00000000	Data Register of Serial Input Link 1	r

Table 33. Serial Link Output Register 0 (SLOReg0)

Bits	Name	Reset Value	Function	r/w
31-0	SLOReg0	0x00000000	Data Register of Serial Output Link 0	w

Table 34. Serial Link Output Register 1 (SLOReg1)

Bits	Name	Reset Value	Function	r/w
31-0	SLOReg1	0x00000000	Data Register of Serial Output Link 1	w

Table 35. Serial Link Status Register (SLStatusReg)

Bits	Name	Reset Value	Function	r/w
0	CSIL0	0	Clear the Serial input link 0	w
1	CSOL0	0	Clear the Serial output link 0	w
2	DR1	0	Data Ready in the serial input link 1	r
3	TRE1	1	Transmitter Register Empty in the serial output link 1	r
4	CSIL1	0	Clear the Serial input link 1	w
5	CSOL1	0	Clear the Serial output link 1	w

Table 36. Parallel Input Port Register (PIPReg)

Bits	Name	Reset Value	Function	r/w
15-0	PIPReg	0x0000	Parallel Input Port Data	r

Table 37. Parallel Output Port Register (POPReg)

Bits	Name	Reset Value	Function	r/w
11-0	POPReg	0x000	Discrete Parallel Output Port 0 output 0 on corresponding VIOP bit if enable 1 output 1 on corresponding VIOP bit if enable	r/w
15-12	POPReg	0x0	Parallel Output Port Control 0 No action 1 Restart associated pulse generator	w

Table 38. Pulse Delay Control Register n (PDCReg n)
n can vary from 12 to 15 depending on the value of POPConfReg

Bits	Name	Reset Value	Function	r/w
31-0	PDCn	0x00000000	Value of the Pulse Delay for bit n of VIOP port if defined as a pulse generator	r/w

Table 39. Pulse Length Control Register n (PLCReg n)
n can vary from 12 to 15 depending on the value of POPConfReg

Bits	Name	Reset Value	Function	r/w
31-0	PLCn	0x00000000	Value of the Pulse Length for bit n of VIOP port if defined as a pulse generator	r/w

Table 40. UART Receive Transmit Register 1 (UARTReg1)

Bits	Name	Reset Value	Function	r/w
31-0	RTD1	0x00000000	Rx/Tx Data of UART1 (8-bit or 32-bit data register depending on SLConfReg)	r/w

Table 41. UART Receive Transmit Register 2 (UARTReg2)

Bits	Name	Reset Value	Function	r/w
31-0	RTD2	0x00000000	Rx/Tx Data of UART2 (8-bit or 32-bit data register depending on SLConfReg)	r/w

Table 42. UART Status Register (UARTStatusReg)

Bits	Name	Reset Value	Function	r/w
0	DR1	0	Data Ready in channel 1	r
1	TRE1	1	Transmitter Register Empty in channel 1	r
2	FE1	0	Framing Error in receiver 1	r
3	PE1	0	Parity Error in receiver 1	r
4	OE1	0	Overrun Error in receiver 1	r
5	CU1	0	Clear UART1	w
6	DR2	0	Data Ready in channel 2	r
7	TRE2	1	Transmitter Register Empty in channel 2	r
8	FE2	0	Framing Error in receiver 2	r
9	PE2	0	Parity Error in receiver 2	r
10	OE2	0	Overrun Error in receiver 2	r
11	CU2	0	Clear UART2	w

Table 43. CRC0 Register (CRCReg0)

Bits	Name	Reset Value	Function	r/w
15-0	CRC0	0x1111	CRC0 register (Reading this register resets it)	r

Table 44. CRC1 Register (CRCReg1)

Bits	Name	Reset Value	Function	r/w
15-0	CRC1	0x1111	CRC1 register (Reading this register resets it)	r

Table 45. FIFO Configuration Register (FIFOConfReg)

Bits	Name	Reset Value	Function	r/w
0	FSI0	0	FIFO10 coupled to SIL1 when 1	r/w
1	FSA0	0	FIFO10 in Stand Alone mode when 1	r/w
2	F20SAEXT0	0	FIFO10 in Stand Alone mode. The FIFO10 20-bit input data bus is connected to DFIFO(19-0) T7904E external port.	r/w
3	Not defined	0	Must be written to zero.	r/w
4	FSO1	0	FIFO11 coupled to SOL1 when 1	r/w
5	FSAO1	0	FIFO11 in Stand Alone mode when 1	r/w
6	F20SAEXT1	0	FIFO11 in Stand Alone mode. The FIFO11 20-bit output data bus is connected to DFIFO(19-0) T7904E external port.	r/w
7	Not defined	0	Must be written to zero.	r/w

Table 46. FIFO Input Register (FIFOInReg)

Bits	Name	Reset Value	Function	r/w
31-0	FIFOIn		Input Data of FIFO	w

Table 47. FIFO Output Register (FIFOOutReg)

Bits	Name	Reset Value	Function	r/w
31-0	FIFOOut		Output Data of FIFO	r

Signal description

Name	Type	Definition
DATA MEMORY Interface		
DMA(24-0)	I/O	Data Memory Address. The Data Memory Address bus is generated by the DSP21020 during a data memory access except During the Program Memory Initialization if performed by the T7904E through the User Extension Interface. On page boundary crossings, this address bus is the DRAM row address bus latched by the DMRAS* signal. It is then generated by the T7904E and the DSP21020 address bus is three stated thanks to DMTS* assertion.
DMAC(1-0)	O	Data Memory LSB Address. These address bits are generated by the T7904E during an access to an automatic 32-bit conversion area.
DMD(39-0)	I/O	Data Memory Data bus.
DMRD*	I/O	Data Memory Read strobe. This signal is asserted by the DSP21020 during a read access. The T7904E outputs the current value of DMRD* when the DSP21020 is high Z.
DMWR*	I/O	Data Memory Write strobe. This signal is asserted by the DSP21020 during a write access. The T7904E outputs the current value of DMWR* when the DSP21020 is high Z.
DMDWR*	O	Data Memory Data Write strobe. This signal is asserted by the T7904E in 3 configurations DRAM implementation, Write access protection (plus one implicit wait state), Parity bit protection (plus one implicit wait state).
DMTS*	O	Data Memory Three State Control. DMTS* is asserted to place the Data Memory address bus , data bus and control strobes of the DSP21020 in high impedance state.
DMACK	O	Data Memory Acknowledge. The T7904E asserts this signal when the Data Memory access is completed.
DMPAGE	I/O	Data Memory Page Boundary. This signal is asserted by the DSP21020 to signal that a Data Memory page boundary has been crossed.
DMS(3-0)	I/O	Data Memory Select lines. These pins are asserted by the DSP21020 as chip selects for the corresponding banks of data memory.
DMRAS*	O	Data Memory Row Address strobe. This signal is generated when a DRAM configuration is selected.
DMCAS*	O	Data Memory Column Address strobe. This signal is generated when a DRAM configuration is selected.
DMPar	I/O	Data Memory Parity Bit. If the parity memory protection is selected, when the DS21020 performs a write operation, the T7904E generates the DMPar parity bit on DMD(39-0) data bus. During a read access, the T7904E checks the data parity. If no data parity protection is selected, DMPar is three-stated.

PROGRAM MEMORY Interface		
PMA(19-0)	I/O	Program Memory Address. The Program Memory Address bus is generated by the DSP21020 during a program memory access except during the Program Memory Initialization if performed by the T7904E.
PMD(47-0)	I/O	Program Memory Data bus. PMD(9) must be connected to a 10k Pull-Up.
PMRD*	I/O	Program Memory Read strobe. This signal is asserted by the DSP21020 during a read access. The T7904E outputs the current value of PMRD* when the DSP21020 is high Z.
PMWR*	I/O	Program Memory Write strobe. This signal is asserted by the DSP21020 during a write access. The T7904E outputs the current value of PMWR* when the DSP21020 is high Z.
PMDWR*	O	Program Memory Data Write strobe. This signal is asserted by the T7904E in 2 configurations Write access protection (plus one implicit wait state), Parity bit protection (plus one implicit wait state),
PMTS*	O	Program Memory Three State Control. PMTS* is asserted to place the Program Memory address bus, data bus and control strobes of the DSP21020 in high impedance state.
PMACK	O	Program Memory Acknowledge. The T7904E asserts this signal when the Program Memory access is completed.
PMS(1-0)	I/O	Program Memory Select lines.
PMPar	I/O	Program Memory ParityBit. If the parity memory protection is selected, when the DS21020 performs a write operation, the T7904E generates the parity bit on PMPar. During a read access, the T7904E checks the data parity. If no memory protection is selected, PMPar is three-stated.
Clocks, Reset and Miscellaneous		
ClkIn	I	Input clock. The frequency of this clock is divided to be distributed to the system.
ClkOut	O	System Clock. It is a 50% duty cycle clock used for clocking the DSP21020.
SysReset*	I	System Hardware Reset. Assertion of this pin resets the T7904E and activates Reset* low.
Reset*	O	Reset pin. This pin is asserted low to reset the DSP21020. This occurs when either SysReset* is asserted or when the T7904E detects an error or on the generation of the software reset command by the DSP21020.
SysAv	O	System available. This signal is asserted high as long as no error is detected by the T7904E.
TestMode, ScanMode, Test Scan and T1Scan	I	Test Mode Enable. Must be tied to zero.
JTAG Interface		
TCK	I	Test Clock. Provides a clock for the JTAG boundary scan.
TMS	I	Test Mode Select. Used to control the JTAG state machine.
TDI	I	Test Data Input. Provides serial data for the boundary scan logic.
TDO	O	Test Data Output. Serial data output of the boundary scan logic.
TRST*	I	Test Reset. Resets the test state machine.

User Extension Interface		
IOSel*(3-0)	O	IO Chip Select .
UEWr*	O	User Extension Write Strobe.
UERd*	O	User Extension Read Strobe.
UERdy2	I	User Extension Data Ready. Indicates that the User Extension access in IO Area 2 is completed. (Active high)
UERdy3*	I	User Extension Data Ready. Indicates that the User Extension access in IO Area 3 is completed. (Active low)
UEEn*	O	User Extension Enable. This signal is asserted when an access to bank 1, 2 or 3 is performed. It is used as an enable signal for the Data Memory extension bus buffer.
VIO port		
VIOP(15-0)	IO	Versatile IO Port
Interrupt Interface		
IRQ*	O	Interrupt Request. T7904E interrupt request to the DSP21020.
ExtIT(3-0)	I	External Interrupt.

The following table shows the T7904E pin states after reset and after PMI.

Pin Name	Value after reset	Value after PMI
DMA(24-0)	Output depending on PMI mode	Input
DMAC(1-0)	Output, driven , value undefined	Output, driven , value undefined
DMD(39-0)	Bidirectional	Bidirectional, High impedance
DMRD*	Output driven high	Input
DMWR*	Output driven high	Input
DMDWR*	Output driven high	Output driven high
DMTS*	Output driven high	Input
DMACK	Output driven low	Output driven low
DMPAGE	Output driven low	Input
DMS(3-0)	Input	Input
DMPar	Bidirectional, High impedance	Bidirectional, High impedance
PMA(19-0)	Output depending on PMI mode	Input
PMD(47-0)	Bidirectional, value depending on PMI mode	Bidirectional, High impedance
PMRD*	Output driven high	Input
PMWR*	Output driven high	Input
PMDWR*	Output driven high	Output driven high
PMTS*	Output driven high	Input
PMACK	Output driven low	Output driven low
PMPar	Bidirectional, value depending on PMI mode	Bidirectional, High impedance
ClkOut	Output	Output
SysAv	Output driven low	Output
Reset*	Output driven high	Output driven high
IOSel*(3-0)	output driven high, except IOSel*(0) depending on PMI mode	Output driven high
UEWr*	Output driven high	Output driven high
UERd*	Output driven, value depending on PMI mode	Output driven high
UEEn*	Output driven, value depending on PMI mode	Output driven high
VIOP(15-0)	Bidirectional, High impedance	Bidirectional, High impedance

Pin Name	Value after reset	Value after PMI
IRQ*	Output driven high	Output driven high
TDO	Output depending on TRST* and TCK	

Characteristics

Electrical interfaces

The following data is provided for information only. Forguaranteed value refer to Atmel procurement specification.

Table 48. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
Vdd	Supply voltage	-0.5	7	V
Vi	Input voltage	-0.5	Vdd + 0.5V	V
Ts	Storage temperature	-65	150	°C
Tj	Maximum junction temperature		165	°C
Rqjc	Thermal resistance		10	°C/W

Table 49. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
Vdd	Supply voltage	4.5	5.0	5.5	V
To	Operating temperature	-55	25	125	°C
Vi	Input Voltage	0	Vdd	Vdd	V
Vo	Output Voltage	0	Vdd	Vdd	V

Table 50. DC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
Vil	Input low voltage			0.8	V
Vih	Input high voltage		2.2		V
Vol	Output voltage low level	Vdd = Min Iol = 3 mA		0.4	V
Voh	Output voltage high level	Vdd = Min Ioh = -3 mA	2.4		V
Ioz	Output leakage current	Vdd = Max 0 ≤ Vout ≤ Vdd	-5	5	uA
Iiz	Input leakage current	Vdd = Max 0 ≤ Vin ≤ Vdd	-5	5	uA
Isc	output short circuit current (one output at a time during 1s max)	Vdd = Max Vout = 0v		48	mA
Iccop	Dynamic Supply current	Vdd = Max f = 40MHz (ClkIn)		350	mA

Capacitance ratings

Parameters	Description	Max (pF)
Cin	Input capacitance	5
Cout	Output capacitance	7
Cio	Input/output bus capacitance	10

AC characteristics

Table 51. Clock and Reset

Symbol	Description	Ref. Edge	Spec		Unit
			min	max	
T/2	Clk frequency (divided by 2 in the T7904E to get ClkOut) : With parity protection Without parity protection			 35 40	 MHz MHz
t01	Reset Assertion Time		2T		

Figure 4. Clock and Reset

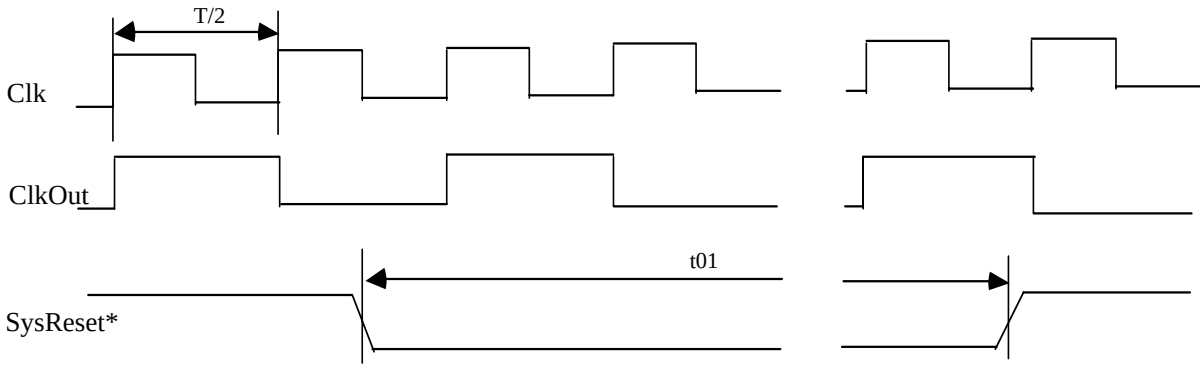


Table 52. Fast Page Mode Read Cycle

Symbol	Description	Ref. Edge	Spec		Unit
			min	max	
t10	DMCAS* delay	ClkOut +	3T/8	3T/8 + 10	ns
t11	DMCAS* de-assertion time	ClkOut +	T/8	T/8 + 10	ns

Figure 5. DRAM Fast Page Mode Read cycle

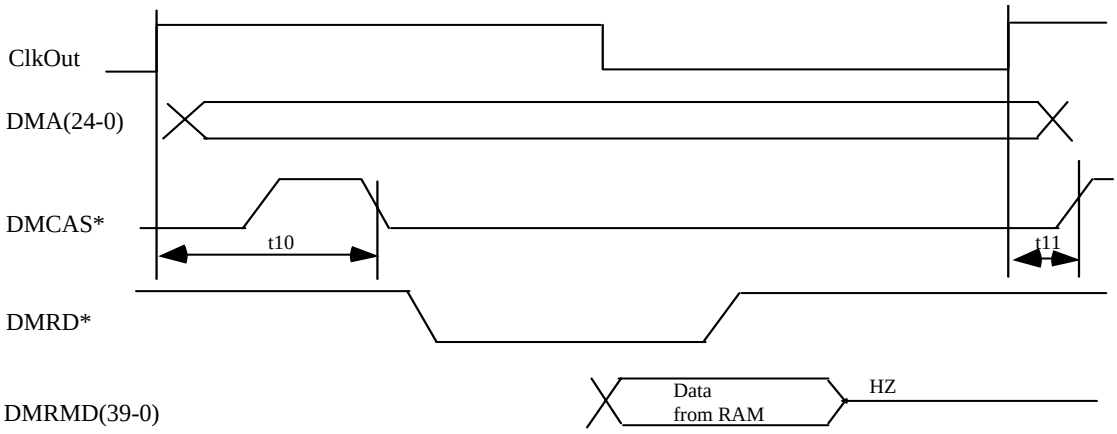
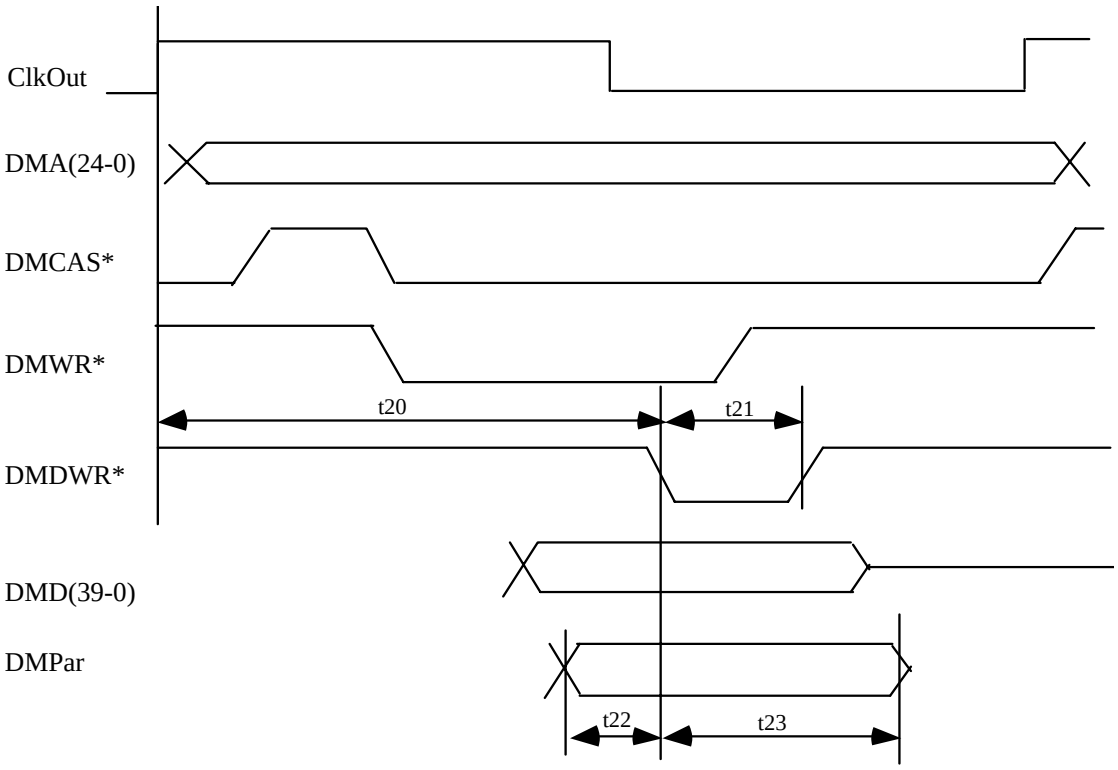


Table 53. Fast Page Mode Delayed Write Cycle

Symbol	Description	Ref. Edge	Spec		Unit
			min	max	
t20	DMDWR* falling edge: One implicit extra wait-state	ClkOut +	11T/8	11T/8+15	ns
t21	Data Write Strobe width		T/4	T/4	ns
t22	Data including parity bit Set Up	DMDWR*-	0		ns
t23	Data including parity bit Hold Time	DMDWR*-	10		ns

Figure 6. DRAM Fast Page Mode Delayed Write cycle



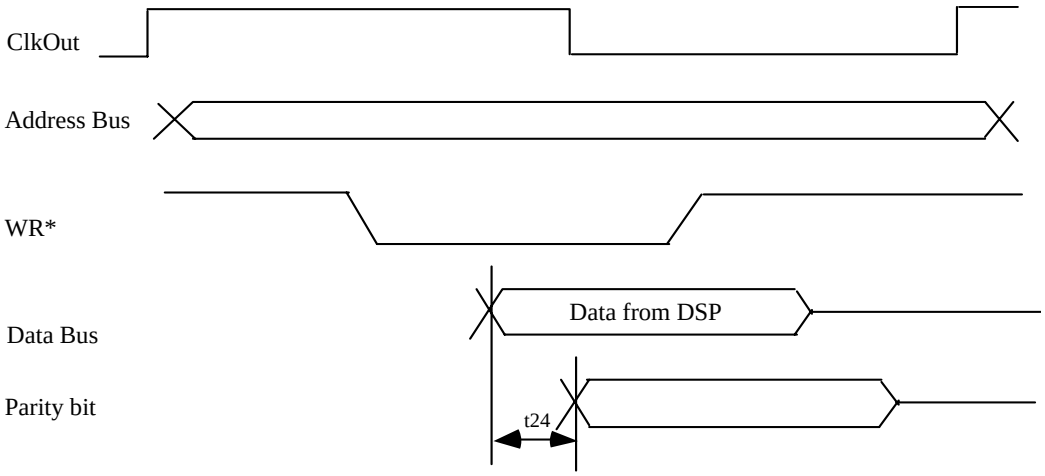
SRAM Read Cycle

Refer to TSC21020 Data Sheet for chronogram and timing

Table 54. Parity protected SRAM Write Cycle

Symbol	Description	Ref. Edge	Spec		Unit
			min	max	
t24	Parity generation time	Data Bus		15	ns

Figure 7. SRAM Write cycle (Parity protected)

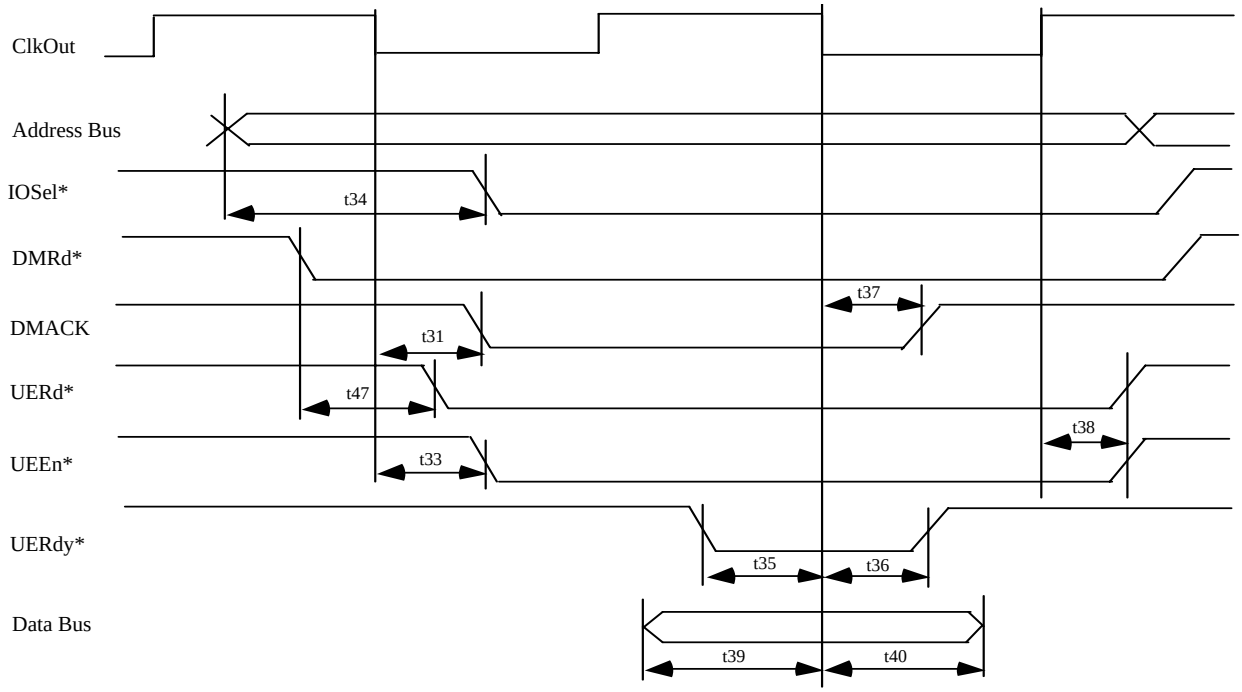


- Address bus is PMA(19-0) or DMA(19-0),
- WR* is PMWR*, DMWR*,
- DWR* is PMDWR*, DMDWR*,
- Data bus is PMD(47-0), DMD(39-0),
- Parity bit is PMPar, DMPar.

Table 55. User Extension Read Cycle

Symbol	Description	Ref. Edge	Spec		Unit
			min	max	
t31	DMACK output delay (falling edge)	ClkOut -		15	ns
t33	UEEn* output delay (falling edge)	ClkOut -		3/2 T/4 + 15	ns
t34	IOSel* output delay	Address Change		17	ns
t35	UERdy* set up	ClkOut -	1/2 T/4		ns
t36	UERdy* hold time	ClkOut -	2 T/4	T	ns
t37	DMACK output delay (rising edge)	ClkOut -		10	ns
t38	UERd*, UEEn* output delay (rising edge)	ClkOut +		1/2 T/4 + 15	ns
t39	Data Bus set up	ClkOut -	5		ns
t40	Data Bus hold time	ClkOut -	25		ns
t43	Data Bus Output Delay in case of Automatic Conversion	ClkOut -		-1/2 T/4 + 15	ns
t46	DMAC(1-0) output delay	ClkOut +		25	ns
t47	UERd* output delay (falling edge)	DMRd*-		15	ns

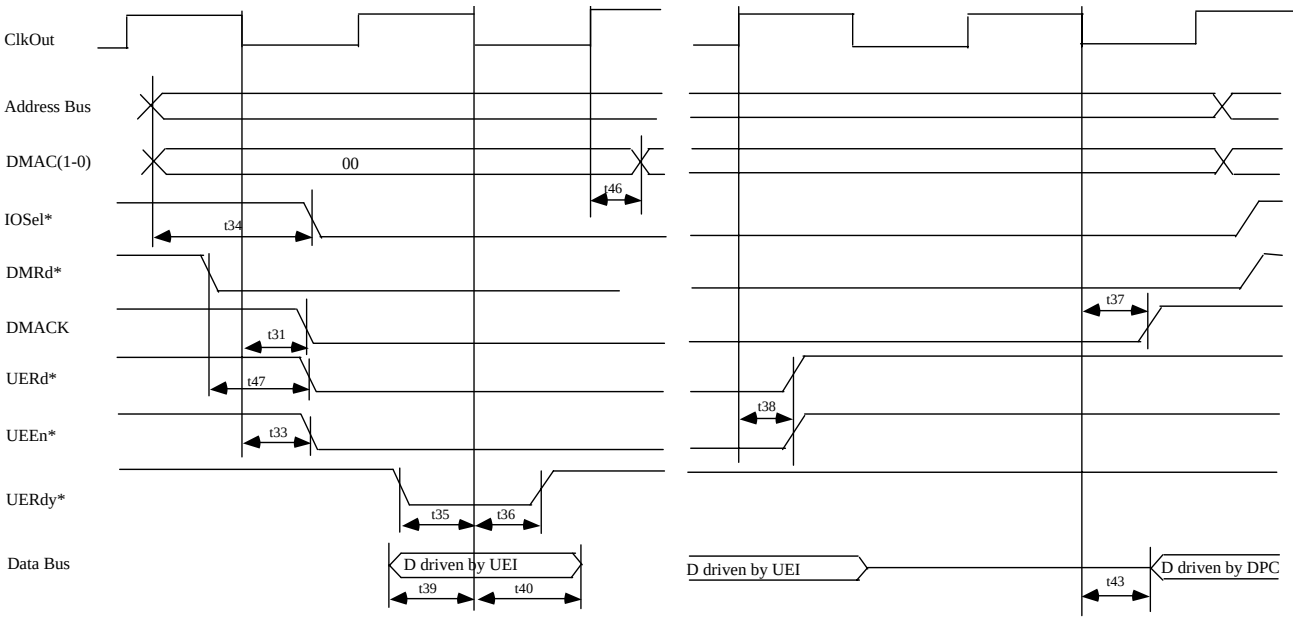
Figure 8. User Extension Read Cycle without Automatic Conversion



User Extension Read Cycle with Automatic Conversion

- UERdy* stands for UERdy2 or UERdy3*. It must be asserted only in case of access in IO Area2 or IO Area3.

Figure 9. User Extension Read Cycle with Automatic Conversion



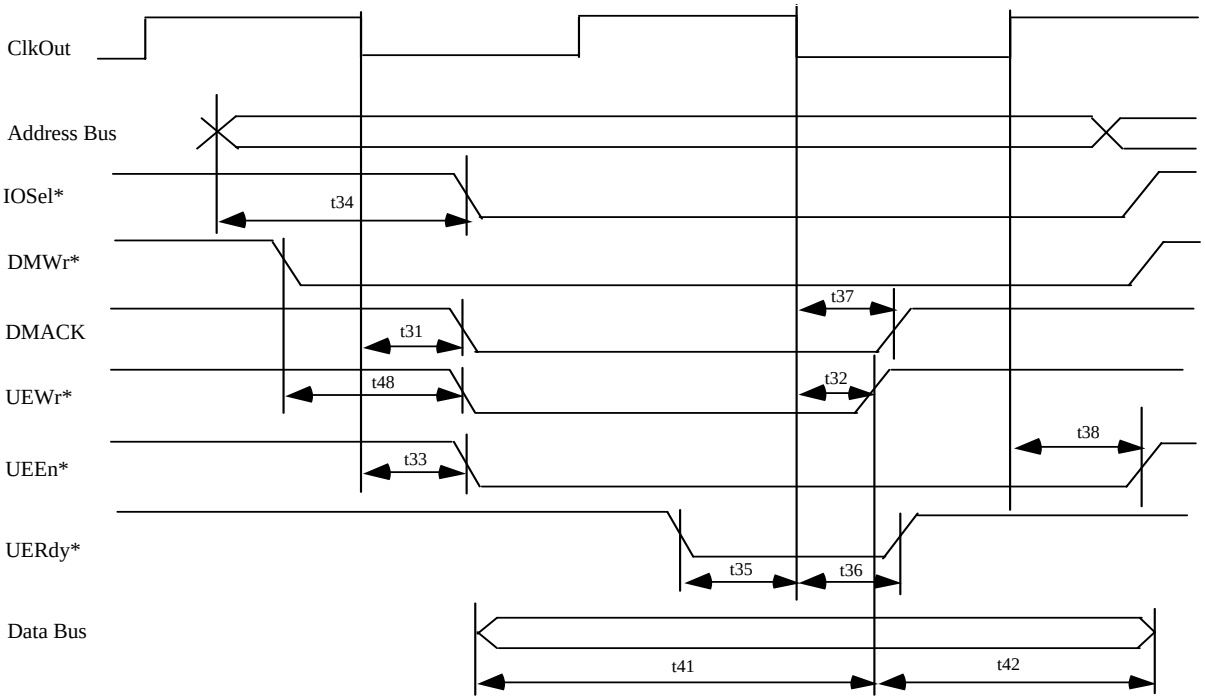
First byte or first 16-bit word is read by the DPC (2 Clk Out periods if zero wait-state)

2 last Clk Out periods dedicated to the data concatenation by the DPC, and then to the data sampling by the DSP

Table 56. User Extension Write Cycle

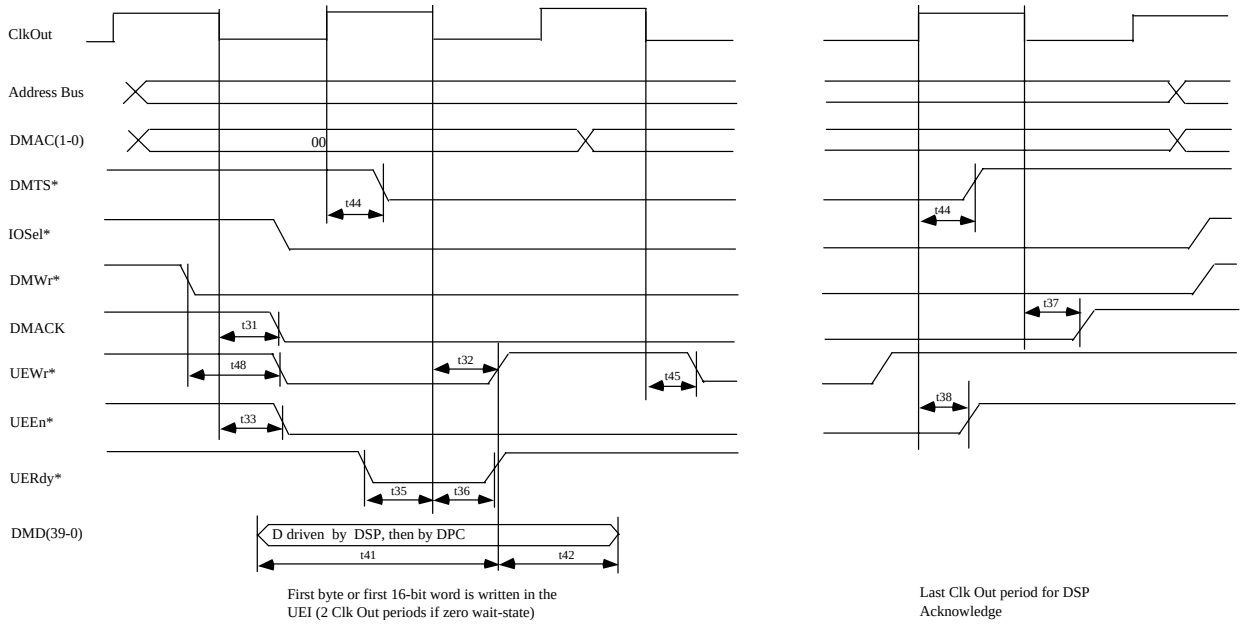
Symbol	Description	Ref. Edge	Spec		Unit
			min	max	
t31	DMACK output delay (falling edge)	ClkOut -		15	ns
t32	UEWr* output delay (rising edge)	ClkOut -		1/2 T/4 + 15	
t33	UEEn* output delay (falling edge)	ClkOut -		3/2 T/4 + 15	ns
t37	DMACK output delay (rising edge)	ClkOut -		10	ns
t38	UEEn* output delay (rising edge)	ClkOut +		1/2 T/4 + 15	ns
t41	Data Set Up	UEWr* +	5/2 T/4		ns
t42	Data Hold Time	UEWr* +	5		ns
t44	DMTS* output delay in case of Automatic Conversion	ClkOut +	0	3/2 T/4 + 15	ns
t45	UEWr* output delay (falling edge) in case of Automatic Conversion	ClkOut -		1/2 T/4 + 15	ns
t48	UEWr* output delay (falling edge)	DMWr* -		15	ns

Figure 10. User Extension Write Cycle Without Automatic Conversion



- UERdy* stands for UERdy2 or UERdy3*. It must be asserted only in case of access in IO Area2 or IO Area3.

Figure 11. User Extension Write Cycle with Automatic Conversion



- UERdy* stands for UERdy2 or UERdy3*. It must be asserted only in case of access in IO Area2 or IO Area3.

Table 57. User Extension Read Cycle during Program Memory Initialization

Symbol	Description	Ref. Edge	Spec		Unit
			min	max	
t46	UERd* output delay	ClkOut -		15	ns
t47	Address Bus Active output delay	ClkOut +		10	ns
t48	Address Bus HZ output delay	ClkOut +		10	ns

Figure 12. User Extension Read Cycle during Program Memory Initialization

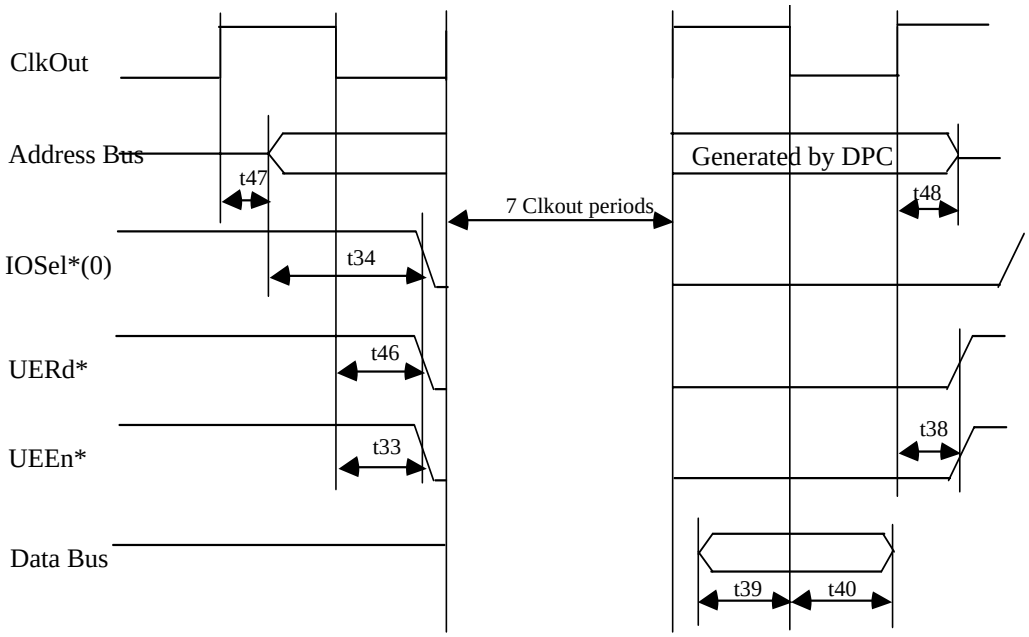


Table 58. General Purpose IO Port

Symbol	Description	Ref. Edge	Spec		Unit
			min	max	
t50	CKO/CKI period (Tck)		T		ns
t51	DO0 output delay	DVALO +		Tck + 15	ns
t52	DOn output delay	CKO -	-5	10	ns
t53	CKO/CKI output delay	DVALO + DVALI +	2 Tck		ns
t54	CKO/CKI output delay	DRO +	2 Tck		ns
t55	DIn set up	CKI +	10		ns
t56	Din hold	CKI +	10		ns
t57	CKO falling edge to DVALO falling edge	CKO -	2 Tck		ns
t57	CKI rising edge to DVALI falling edge	CKI +	20		ns

Figure 13. Synchronous Output Serial Link

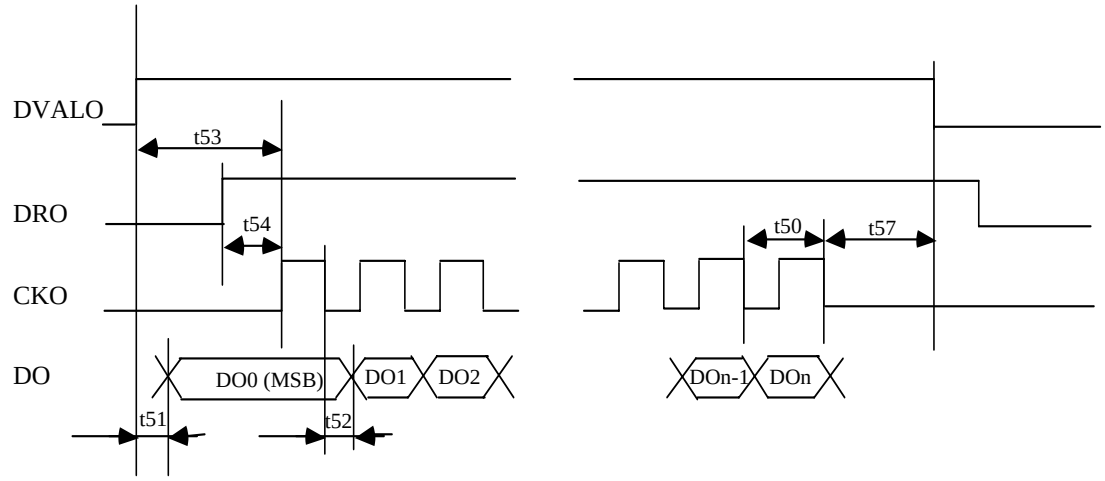


Figure 14. Synchronous Input Serial Link

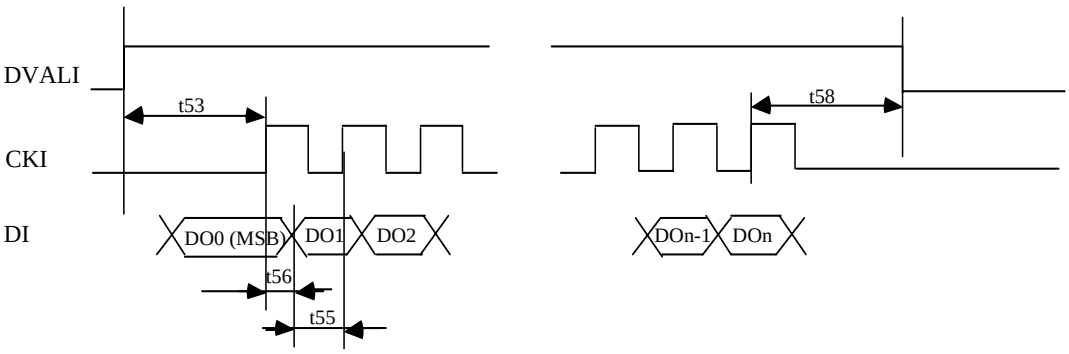
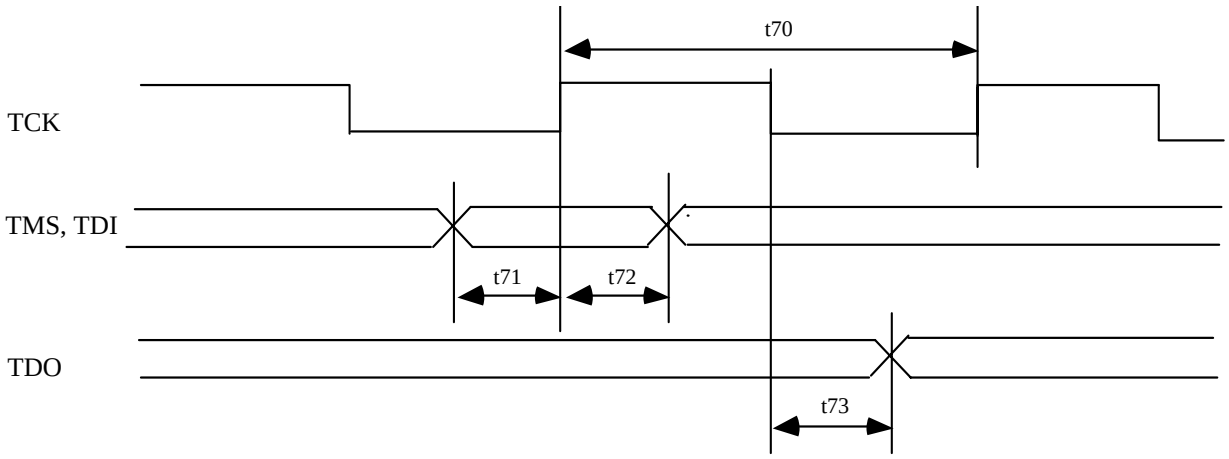


Table 59. JTAG interface

Symbol	Description	Ref. Edge	Spec		Unit
			min	max	
t70	TCK period		T		ns
t71	TDI, TMS set-up	TCK +	5		ns
t72	TDI, TMS hold	TCK +	6		ns
t73	TDO output delay	TCK -		15	ns

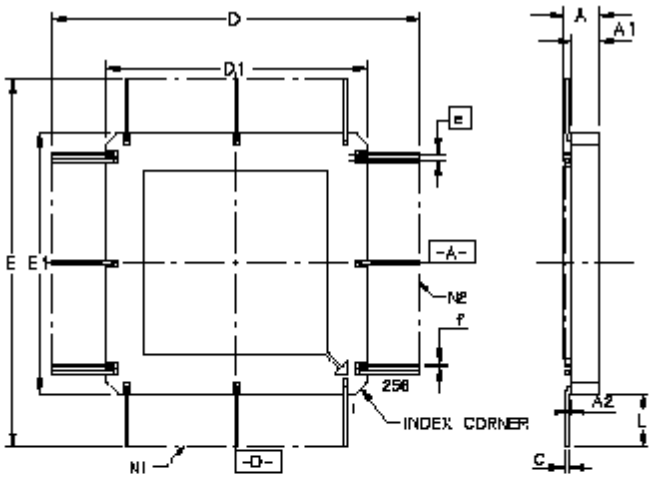
Figure 15. JTAG interface



Mechanical interfaces

Packaging

The T7904E can be procured in a 256 pin MQFPF ceramic package.



	mm		mils	
	Min	Max	Min	Max
A	2.41	3.18	.095	.125
C	0.10	0.20	.004	.008
D	53.23	55.74	2.095	2.195
D1	36.83	37.34	1.450	1.470
E	53.23	55.74	2.095	2.195
E1	36.83	37.34	1.450	1.470
e	0.508 BSC		.020 BSC	
r	0.15	0.25	.008	.010
A1	2.08	2.56	.081	.101
A2	0.05	0.36	.002	.014
L	8.20	9.20	.323	.362
N1	64		64	
N2	64		64	

Table 60. Pin Assignment

Pin	Function	Buffer Type	Pin	Function	Buffer Type	Pin	Function	Buffer Type
64	PMD(25)	BIOT6	37	PMD(46)	BIOT6	11	VCC	
62	PMD(26)	BIOT6	35	PMD(47)	BIOT6	12	PMPar	BIOT6
63	PMD(27)	BIOT6	38	VSS		9	PMRD*	BIOT3
60	PMD(28)	BIOT6	33	VSS		10	PMWR*	BIOT3
61	PMD(29)	BIOT6	36	PMA(0)	BIOT3	7	PMDWR*	BOUT6
58	VSSB		34	PMA(1)	BIOT3	8	PMTS*	BOUT3
59	VSSA		31	PMA(2)	BIOT3	5	PMACK	BOUT6
56	VSSB		32	PMA(3)	BIOT3	3	PMS*(0)	BIOT3
57	PMD(30)	BIOT6	29	PMA(4)	BIOT3	6	PMS*(1)	BIOT3
54	PMD(31)	BIOT6	30	PMA(5)	BIOT3	1	VSS	
55	PMD(32)	BIOT6	27	PMA(6)	BIOT3	4	VSSPLLA	
53	PMD(33)	BIOT6	28	PMA(7)	BIOT3	2	VCCPLLA	
52	PMD(34)	BIOT6	25	PMA(8)	BIOT3	256	PLLOUT	
51	PMD(35)	BIOT6	26	PMA(9)	BIOT3	254	VSSPLL	
50	PMD(36)	BIOT6	23	PMA(10)	BIOT3	252	VCCPLL	
49	PMD(37)	BIOT6	24	PMA(11)	BIOT3	255	VSS	
48	PMD(38)	BIOT6	21	PMA(12)	BIOT3	250	ClkIn	BINTTL
47	PMD(39)	BIOT6	22	PMA(13)	BIOT3	253	ClkOut	BIOT6
46	VCC		19	PMA(14)	BIOT3	248	SysReset*	BINTTL
45	VCC		20	PMA(15)	BIOT3	251	Reset*	BOUT3
44	PMD(40)	BIOT6	17	PMA(16)	BIOT3	246	SysAv	BOUT3
43	PMD(41)	BIOT6	18	PMA(17)	BIOT3	249	TESTMODE	BINTTL
41	PMD(42)	BIOT6	15	PMA(18)	BIOT3	244	SCANMODE	BINTTL
42	PMD(43)	BIOT6	16	PMA(19)	BIOT3	247	TESTSCAN	BINTTL
39	PMD(44)	BIOT6	13	VCC		242	T1SCAN	BINTTL
40	PMD(45)	BIOT6	14	VCC		245	TCK	BINTTL
240	TMS	BINTUP	210	IOSel*(0)	BOUT3	180	DMD(17)	BIOT6
243	TDI	BINTUP	209	IOSel*(1)	BOUT3	179	DMD(18)	BIOT6
238	TDO	B3STA3	208	IOSel*(2)	BOUT3	178	DMD(19)	BIOT6
236	TRST*	BINTUP	207	IOSel*(3)	BOUT3	177	VCC	
241	IRQ*	BOUT3	205	UEWr*	BOUT3	176	VCC	
239	ExtIT(0)	BINTTL	206	UERd*	BOUT3	175	VCC	
234	ExtIT(1)	BINTTL	204	UERdy2	BINTTL	174	DMD(20)	BIOT6
237	ExtIT(2)	BINTTL	203	UERdy3*	BINTTL	171	DMD(21)	BIOT6

Pin	Function	Buffer Type	Pin	Function	Buffer Type	Pin	Function	Buffer Type
232	ExtIT(3)	BINTTL	202	UEEn*	BOUT3	170	DMD(22)	BIOT6
235	VIOP(0)	BIOT3	201	VCC		167	DMD(23)	BIOT6
230	VIOP(1)	BIOT3	200	VCC		166	DMD(24)	BIOT6
233	VCC		199	DMD(0)	BIOT6	164	DMD(25)	BIOT6
228	VCC		197	DMD(1)	BIOT6	163	DMD(26)	BIOT6
231	VIOP(2)	BIOT3	198	DMD(2)	BIOT6	162	DMD(27)	BIOT6
229	VIOP(3)	BIOT3	195	DMD(3)	BIOT6	161	DMD(28)	BIOT6
226	VIOP(4)	BIOT3	196	DMD(4)	BIOT6	160	DMD(29)	BIOT6
227	VIOP(5)	BIOT3	193	DMD(5)	BIOT6	158	VSS	
224	VIOP(6)	BIOT3	194	DMD(6)	BIOT6	157	VSS	
225	VIOP(7)	BIOT3	192	DMD(7)	BIOT6	156	VSS	
223	VIOP(8)	BIOT3	190	DMD(8)	BIOT6	155	DMD(30)	BIOT6
222	VIOP(9)	BIOT3	191	DMD(9)	BIOT6	153	DMD(31)	BIOT6
221	VIOP(10)	BIOT3	188	VSS		154	DMD(32)	BIOT6
220	VSS		189	VSS		151	DMD(33)	BIOT6
219	VSS		186	DMD(10)	BIOT6	152	DMD(34)	BIOT6
218	VSS		187	DMD(11)	BIOT6	149	DMD(35)	BIOT6
217	VIOP(11)	BIOT3	184	DMD(12)	BIOT6	150	DMD(36)	BIOT6
216	VIOP(12)	BIOT3	185	DMD(13)	BIOT6	147	DMD(37)	BIOT6
215	VIOP(13)	BIOT3	183	DMD(14)	BIOT6	148	DMD(38)	BIOT6
212	VIOP(14)	BIOT3	182	DMD(15)	BIOT6	145	DMD(39)	BIOT6
211	VIOP(15)	BIOT3	181	DMD(16)	BIOT6	143	DMAC(0)	BOUT3
146	DMAC(1)	BOUT3	121	DMA(22)	BIOT3	89	PMD(9)	BIOT6
144	VCC		116	DMA(23)	BIOT3	88	VSS	
141	VCC		119	DMA(24)	BIOT3	87	VSS	
142	DMA(0)	BIOT3	114	VSS		86	PMD(10)	BIOT6
139	DMA(1)	BIOT3	117	VSS		85	PMD(11)	BIOT6
140	DMA(2)	BIOT3	112	DMPar	BIOT6DN	84	PMD(12)	BIOT6
137	DMA(3)	BIOT3	115	DMRD*	BIOT3	81	PMD(13)	BIOT6
138	DMA(4)	BIOT3	110	DMWR*	BIOT3	79	PMD(14)	BIOT6
135	DMA(5)	BIOT3	113	DMDWR*	BOUT6	76	PMD(15)	BIOT6
136	DMA(6)	BIOT3	111	DMTS*	BOUT3	75	PMD(16)	BIOT6
133	DMA(7)	BIOT3	108	DMACK	BOUT6	74	PMD(17)	BIOT6
134	DMA(8)	BIOT3	109	DMPAGE	BIOT3	73	PMD(18)	BIOT6
131	DMA(9)	BIOT3	106	DMS*(0)	BIOT3	72	PMD(19)	BIOT6

Pin	Function	Buffer Type	Pin	Function	Buffer Type	Pin	Function	Buffer Type
132	DMA(10)	BIOT3	107	DMS*(1)	BIOT3	71	VCC	
129	DMA(11)	BIOT3	104	DMS*(2)	BIOT3	70	VCC	
130	DMA(12)	BIOT3	105	DMS*(3)	BIOT3	69	PMD(20)	BIOT6
NC	NC		102	DMRAS*	BOUT3	67	PMD(21)	BIOT6
NC	NC		100	DMCAS*	BOUT6	68	PMD(22)	BIOT6
NC	NC		103	VCC		65	PMD(23)	BIOT6
NC	NC		98	VCC				
NC	NC		101	VCC				
128	DMA(13)	BIOT3	99	PMD(0)	BIOT6			
126	DMA(14)	BIOT3	96	PMD(1)	BIOT6			
124	DMA(15)	BIOT3	97	PMD(2)	BIOT6			
127	DMA(16)	BIOT3	94	PMD(3)	BIOT6			
122	DMA(17)	BIOT3	95	PMD(4)	BIOT6			
125	DMA(18)	BIOT3	93	PMD(5)	BIOT6			
120	DMA(19)	BIOT3	92	PMD(6)	BIOT6			
123	DMA(20)	BIOT3	91	PMD(7)	BIOT6			
118	DMA(21)	BIOT3	90	PMD(8)	BIOT6			

Abbreviations

ASIC	Application Specific Integrated Circuit
CRC	Cyclic Redundancy Code
DPC	DSP Peripheral Controller
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
DSP	Digital Signal Processing
PMI	Program Memory Initialization
SEU	Single Event Upsets
SIL	Serial Input Link
SOL	Serial Output Link
SRAM	Static RAM
TAP	Test Access Port
UEI	User Extension Interface

Annex 1 : Boundary register

628 IRQ_N output
627 RorW_N + observe_only
626 ExtIT(0) observe_only
625 EFlag_N + output
624 ExtIT(1) observe_only
623 HFlag_N + output
622 ExtIT(2) observe_only
621 FFlag_N + output
620 ExtIT(3) observe_only
619 DFIFO(0) + output X 617
618 DFIFO(0) + observe_only
617 control + DFIFO Output Enable
616 VIOP(0) output X 614
615 VIOP(0) observe_only
614 control VIOP(0) Output Enable
613 DFIFO(1) + output X 617
612 DFIFO(1) + observe_only
611 VIOP(1) output X 609
610 VIOP(1) observe_only
609 control VIOP(1) Output Enable
608 DFIFO(2) + output X 617
607 DFIFO(2) + observe_only
606 VIOP(2) output X 604
605 VIOP(2) observe_only
604 control VIOP(2) Output Enable
603 DFIFO(3) + output X 617
602 DFIFO(3) + observe_only
601 VIOP(3) output X 599
600 VIOP(3) observe_only
599 control VIOP(3) Output Enable
598 DFIFO(4) + output X 617
597 DFIFO(4) + observe_only
596 VIOP(4) output X 594
595 VIOP(4) observe_only
594 control VIOP(4) Output Enable
593 DFIFO(5) + output X 617
592 DFIFO(5) + observe_only
591 VIOP(5) output X 589
590 VIOP(5) observe_only
589 control VIOP(5) Output Enable
588 DFIFO(6) + output X 617
587 DFIFO(8) + output X 617
577 DFIFO(8) + observe_only
576 VIOP(8) output X 574
575 VIOP(8) observe_only
574 control VIOP(8) Output Enable
573 DFIFO(9) + output X 617
572 DFIFO(9) + observe_only
571 VIOP(9) output X 569
570 VIOP(9) observe_only
569 control VIOP(9) Output Enable
568 DFIFO(10) + output X 617
567 DFIFO(10) + observe_only
566 VIOP(10) output X 564
565 VIOP(10) observe_only
564 control VIOP(10) Output Enable
563 DFIFO(11) + output X 617
562 DFIFO(11) + observe_only
561 VIOP(11) output X 559
560 VIOP(11) observe_only
559 control VIOP(11) Output Enable
558 DFIFO(12) + output X 617
557 DFIFO(12) + observe_only
556 VIOP(12) output X 554
555 VIOP(12) observe_only
554 control VIOP(12) Output Enable
553 DFIFO(13) + output X 617
552 DFIFO(13) + observe_only
551 VIOP(13) output X 549
550 VIOP(13) observe_only
549 control VIOP(13) Output Enable
548 DFIFO(14) + output X 617
547 DFIFO(14) + observe_only
546 VIOP(14) output X 544
545 VIOP(14) observe_only
544 control VIOP(14) Output Enable
543 DFIFO(15) + output X 617
542 DFIFO(15) + observe_only
541 VIOP(15) output X 539
540 VIOP(15) observe_only
539 control VIOP(15) Output Enable
538 DFIFO(16) + output X 617
537 DFIFO(16) + observe_only
536 IOSel_N(0) output
535 DFIFO(17) + output X 617
534 DFIFO(17) + observe_only

533 IOSel_N(1) output
532 DFIFO(18) + output X 617
531 DFIFO(18) + observe_only
530 IOSel_N(2) output
529 DFIFO(19) + output X 617
528 DFIFO(19) + observe_only
527 IOSel_N(3) output
526 UEWR_N output
525 UERD_N output
524 UERdy2 observe_only
523 UERdy3_N observe_only
522 UEEn_N output
521 DMRMD(0) + output X 519
520 DMRMD(0) + observe_only
519 control + DMRMD Output Enable
518 DMD(0) output X 516
517 DMD(0) observe_only
516 control DMD Output Enable
515 DMRMD(1) + output X 519
514 DMRMD(1) + observe_only
513 DMD(1) output X 516
512 DMD(1) observe_only
511 DMRMD(2) + output X 519
510 DMRMD(2) + observe_only
509 DMD(2) output X 516
508 DMD(2) observe_only
507 DMRMD(3) + output X 519
506 DMRMD(3) + observe_only
505 DMD(3) output X 516
504 DMD(3) observe_only
503 DMRMD(4) + output X 501
502 DMRMD(4) + observe_only
501 control + DMRMD Output Enable
500 DMD(4) output X 498
499 DMD(4) observe_only
498 control DMD Output Enable
497 DMRMD(5) + output X 519
496 DMRMD(5) + observe_only
495 DMD(5) output X 516
494 DMD(5) observe_only
493 DMRMD(6) + output X 519
492 DMRMD(6) + observe_only
491 DMD(6) output X 516
490 DMD(6) observe_only
489 DMRMD(7) + output X 519
488 DMRMD(7) + observe_only
487 DMD(7) output X 516
486 DMD(7) observe_only
485 DMRMD(8) + output X 519
484 DMRMD(8) + observe_only
483 DMD(8) output X 516
482 DMD(8) observe_only
481 DMRMD(9) + output X 519
480 DMRMD(9) + observe_only
479 DMD(9) output X 516
478 DMD(9) observe_only
477 DMRMD(10) + output X 519
476 DMRMD(10) + observe_only
475 DMD(10) output X 516
474 DMD(10) observe_only
473 DMRMD(11) + output X 519
472 DMRMD(11) + observe_only
471 DMD(11) output X 516
470 DMD(11) observe_only
469 DMRMD(12) + output X 519
468 DMRMD(12) + observe_only
467 DMD(12) output X 516
466 DMD(12) observe_only
465 DMRMD(13) + output X 519
464 DMRMD(13) + observe_only
463 DMD(13) output X 516
462 DMD(13) observe_only
461 DMRMD(14) + output X 519
460 DMRMD(14) + observe_only
459 DMD(14) output X 516
458 DMD(14) observe_only
457 DMRMD(15) + output X 519
456 DMRMD(15) + observe_only
455 DMD(15) output X 516
454 DMD(15) observe_only
453 DMRMD(16) + output X 519
452 DMRMD(16) + observe_only
451 DMD(16) output X 516
450 DMD(16) observe_only
449 DMRMD(17) + output X 519
448 DMRMD(17) + observe_only
447 DMD(17) output X 516
446 DMD(17) observe_only
445 DMRMD(18) + output X 519
444 DMRMD(18) + observe_only
443 DMD(18) output X 516
442 DMD(18) observe_only
441 DMRMD(19) + output X 519
440 DMRMD(19) + observe_only
439 DMD(19) output X 498
438 DMD(19) observe_only

437 DMRMD(20) + output X 519
436 DMRMD(20) + observe_only
435 DMD(20) output X 516
434 DMD(20) observe_only
433 DMRMD(21) + output X 519
432 DMRMD(21) + observe_only
431 DMD(21) output X 516
430 DMD(21) observe_only
429 DMRMD(22) + output X 519
428 DMRMD(22) + observe_only
427 DMD(22) output X 516
426 DMD(22) observe_only
425 DMRMD(23) + output X 519
424 DMRMD(23) + observe_only
423 DMD(23) output X 516
422 DMD(23) observe_only
421 DMRMD(24) + output X 519
420 DMRMD(24) + observe_only
419 DMD(24) output X 498
418 DMD(24) observe_only
417 DMRMD(25) + output X 501
416 DMRMD(25) + observe_only
415 DMD(25) output X 516
414 DMD(25) observe_only
413 DMRMD(26) + output X 501
412 DMRMD(26) + observe_only
411 DMD(26) output X 516
410 DMD(26) observe_only
409 DMRMD(27) + output X 519
408 DMRMD(27) + observe_only
407 DMD(27) output X 498
406 DMD(27) observe_only
405 DMRMD(28) + output X 519
404 DMRMD(28) + observe_only
403 DMD(28) output X 516
402 DMD(28) observe_only
401 DMRMD(29) + output X 501
400 DMRMD(29) + observe_only
399 DMD(29) output X 516
398 DMD(29) observe_only
397 DMRMD(30) + output X 519
396 DMRMD(30) + observe_only
395 DMD(30) output X 498
394 DMD(30) observe_only
393 DMRMD(31) + output X 501
392 DMRMD(31) + observe_only
391 DMD(31) output X 516
390 DMD(31) observe_only

389 DMRMD(32) + output X 519
388 DMRMD(32) + observe_only
387 DMD(32) output X 498
386 DMD(32) observe_only
385 DMRMD(33) + output X 501
384 DMRMD(33) + observe_only
383 DMD(33) output X 516
382 DMD(33) observe_only
381 DMRMD(34) + output X 519
380 DMRMD(34) + observe_only
379 DMD(34) output X 516
378 DMD(34) observe_only
377 DMRMD(35) + output X 519
376 DMRMD(35) + observe_only
375 DMD(35) output X 498
374 DMD(35) observe_only
373 DMRMD(36) + output X 501
372 DMRMD(36) + observe_only
371 DMD(36) output X 498
370 DMD(36) observe_only
369 DMRMD(37) + output X 519
368 DMRMD(37) + observe_only
367 DMD(37) output X 516
366 DMD(37) observe_only
365 DMRMD(38) + output X 501
364 DMRMD(38) + observe_only
363 DMD(38) output X 516
362 DMD(38) observe_only
361 DMRMD(39) + output X 519
360 DMRMD(39) + observe_only
359 DMD(39) output X 516
358 DMD(39) observe_only
357 DMAC(0) output
356 DMAC(1) output
355 DMA(0) output X 353
354 DMA(0) observe_only
353 control DMA Output Enable
352 DMA(1) output X 353
351 DMA(1) observe_only
350 DMA(2) output X 353
349 DMA(2) observe_only
348 DMA(3) output X 353
347 DMA(3) observe_only
346 DMA(4) output X 353
345 DMA(4) observe_only
344 DMA(5) output X 353
343 DMA(5) observe_only
342 DMA(6) output X 353

341 DMA(6) observe_only
340 DMA(7) output X 353
339 DMA(7) observe_only
338 DMA(8) output X 353
337 DMA(8) observe_only
336 DMA(9) output X 353
335 DMA(9) observe_only
334 DMA(10) output X 353
333 DMA(10) observe_only
332 DMA(11) output X 353
331 DMA(11) observe_only
330 DMA(12) output X 353
329 DMA(12) observe_only
328 DMA(13) output X 353
327 DMA(13) observe_only
326 DMA(14) output X 353
325 DMA(14) observe_only
324 DMA(15) output X 353
323 DMA(15) observe_only
322 DMA(16) output X 353
321 DMA(16) observe_only
320 DMA(17) output X 353
319 DMA(17) observe_only
318 DMA(18) output X 353
317 DMA(18) observe_only
316 DMA(19) output X 353
315 DMA(19) observe_only
314 DMA(20) output X 353
313 DMA(20) observe_only
312 DMA(21) output X 353
311 DMA(21) observe_only
310 DMA(22) output X 353
309 DMA(22) observe_only
308 DMA(23) output X 353
307 DMA(23) observe_only
306 DMA(24) output X 353
305 DMA(24) observe_only
304 DMPar output X 302
303 DMPar observe_only
302 control DMPar Output Enable
301 DMCB(1) + output X 519
300 DMCB(1) + observe_only
299 DMRD_N output X 353
298 DMRD_N observe_only
297 DMCB(2) + output X 519
296 DMCB(2) + observe_only
295 DMWR_N output X 353
294 DMWR_N observe_only
293 DMCB(3) + output X 519
292 DMCB(3) + observe_only
291 DMDWR_N output
290 DMCB(4) + output X 519
289 DMCB(4) + observe_only
288 DMTS_N output
287 DMCB(5) + output X 519
286 DMCB(5) + observe_only
285 DMACK output
284 DMCB(6) + output X 519
283 DMCB(6) + observe_only
282 DMPAGE output X 353
281 DMPAGE observe_only
280 DMS_N(0) output X 353
279 DMS_N(0) observe_only
278 DMS_N(1) output X 353
277 DMS_N(1) observe_only
276 DMS_N(2) output X 353
275 DMS_N(2) observe_only
274 DMS_N(3) output X 353
273 DMS_N(3) observe_only
272 DMRAS_N output
271 DMCAS_N output
270 PMRMD(0) + output X 268
269 PMRMD(0) + observe_only
268 control PMRMD Output Enable
267 PMD(0) output X 265
266 PMD(0) observe_only
265 control PMD Output Enable
264 PMRMD(1) + output X 268
263 PMRMD(1) + observe_only
262 PMD(1) output X 265
261 PMD(1) observe_only
260 PMRMD(2) + output X 268
259 PMRMD(2) + observe_only
258 PMD(2) output X 265
257 PMD(2) observe_only
256 PMRMD(3) + output X 268
255 PMRMD(3) + observe_only
254 PMD(3) output X 265
253 PMD(3) observe_only
252 PMRMD(4) + output X 268
251 PMRMD(4) + observe_only
250 PMD(4) output X 265
249 PMD(4) observe_only
248 PMRMD(5) + output X 268
247 PMRMD(5) + observe_only
246 PMD(5) output X 265

245 PMD(5) observe_only
244 PMRMD(6) + output X 268
243 PMRMD(6) + observe_only
242 PMD(6) output X 265
241 PMD(6) observe_only
240 PMRMD(7) + output X 268
239 PMRMD(7) + observe_only
238 PMD(7) output X 265
237 PMD(7) observe_only
236 PMRMD(8) + output X 268
235 PMRMD(8) + observe_only
234 PMD(8) output X 265
233 PMD(8) observe_only
232 PMRMD(9) + output X 268
231 PMRMD(9) + observe_only
230 PMD(9) output X 265
229 PMD(9) observe_only
228 PMRMD(10) + output X 268
227 PMRMD(10) + observe_only
226 PMD(10) output X 265
225 PMD(10) observe_only
224 PMRMD(11) + output X 268
223 PMRMD(11) + observe_only
222 PMD(11) output X 265
221 PMD(11) observe_only
220 PMRMD(12) + output X 268
219 PMRMD(12) + observe_only
218 PMD(12) output X 265
217 PMD(12) observe_only
216 PMRMD(13) + output X 268
215 PMRMD(13) + observe_only
214 PMD(13) output X 265
213 PMD(13) observe_only
212 PMRMD(14) + output X 268
211 PMRMD(14) + observe_only
210 PMD(14) output X 265
209 PMD(14) observe_only
208 PMRMD(15) + output X 268
207 PMRMD(15) + observe_only
206 PMD(15) output X 265
205 PMD(15) observe_only
204 PMRMD(16) + output X 268
203 PMRMD(16) + observe_only
202 PMD(16) output X 265
201 PMD(16) observe_only
200 PMRMD(17) + output X 268
199 PMRMD(17) + observe_only
198 PMD(17) output X 265
197 PMD(17) observe_only
196 PMRMD(18) + output X 268
195 PMRMD(18) + observe_only
194 PMD(18) output X 265
193 PMD(18) observe_only
192 PMRMD(19) + output X 268
191 PMRMD(19) + observe_only
190 PMD(19) output X 265
189 PMD(19) observe_only
188 PMRMD(20) + output X 268
187 PMRMD(20) + observe_only
186 PMD(20) output X 265
185 PMD(20) observe_only
184 PMRMD(21) + output X 268
183 PMRMD(21) + observe_only
182 PMD(21) output X 265
181 PMD(21) observe_only
180 PMRMD(22) + output X 268
179 PMRMD(22) + observe_only
178 PMD(22) output X 265
177 PMD(22) observe_only
176 PMRMD(23) + output X 268
175 PMRMD(23) + observe_only
174 PMD(23) output X 265
173 PMD(23) observe_only
172 PMRMD(24) + output X 268
171 PMRMD(24) + observe_only
170 PMD(24) output X 265
169 PMD(24) observe_only
168 PMRMD(25) + output X 268
167 PMRMD(25) + observe_only
166 PMD(25) output X 265
165 PMD(25) observe_only
164 PMRMD(26) + output X 268
163 PMRMD(26) + observe_only
162 PMD(26) output X 265
161 PMD(26) observe_only
160 PMRMD(27) + output X 268
159 PMRMD(27) + observe_only
158 PMD(27) output X 265
157 PMD(27) observe_only
156 PMRMD(28) + output X 268
155 PMRMD(28) + observe_only
154 PMD(28) output X 265
153 PMD(28) observe_only
152 PMRMD(29) + output X 268
151 PMRMD(29) + observe_only
150 PMD(29) output X 265

149 PMD(29) observe_only
148 PMRMD(30) + output X 146
147 PMRMD(30) + observe_only
146 control PMRMD Output Enable
145 PMD(30) output X 265
144 PMD(30) observe_only
143 PMRMD(31) + output X 146
142 PMRMD(31) + observe_only
141 PMD(31) output X 265
140 PMD(31) observe_only
139 PMRMD(32) + output X 146
138 PMRMD(32) + observe_only
137 PMD(32) output X 135
136 PMD(32) observe_only
135 control PMD Output Enable
134 PMRMD(33) + output X 146
133 PMRMD(33) + observe_only
132 PMD(33) output X 135
131 PMD(33) observe_only
130 PMRMD(34) + output X 146
129 PMRMD(34) + observe_only
128 PMD(34) output X 135
127 PMD(34) observe_only
126 PMRMD(35) + output X 146
125 PMRMD(35) + observe_only
124 PMD(35) output X 135
123 PMD(35) observe_only
122 PMRMD(36) + output X 146
121 PMRMD(36) + observe_only
120 PMD(36) output X 135
119 PMD(36) observe_only
118 PMRMD(37) + output X 146
117 PMRMD(37) + observe_only
116 PMD(37) output X 135
115 PMD(37) observe_only
114 PMRMD(38) + output X 146
113 PMRMD(38) + observe_only
112 PMD(38) output X 135
111 PMD(38) observe_only
110 PMRMD(39) + output X 146
109 PMRMD(39) + observe_only
108 PMD(39) output X 135
107 PMD(39) observe_only
106 PMRMD(40) + output X 146
105 PMRMD(40) + observe_only
104 PMD(40) output X 135
103 PMD(40) observe_only
102 PMRMD(41) + output X 146
101 PMRMD(41) + observe_only
100 PMD(41) output X 135
99 PMD(41) observe_only
98 PMRMD(42) + output X 146
97 PMRMD(42) + observe_only
96 PMD(42) output X 135
95 PMD(42) observe_only
94 PMRMD(43) + output X 146
93 PMRMD(43) + observe_only
92 PMD(43) output X 135
91 PMD(43) observe_only
90 PMRMD(44) + output X 146
89 PMRMD(44) + observe_only
88 PMD(44) output X 135
87 PMD(44) observe_only
86 PMRMD(45) + output X 146
85 PMRMD(45) + output X 135
79 PMD(46) observe_only
78 PMRMD(47) + output X 146
77 PMRMD(47) + observe_only
76 PMD(47) output X 135
75 PMD(47) observe_only
74 PMA(0) output X 72
73 PMA(0) observe_only
72 control PMA Output Enable
71 PMA(1) output X 72
70 PMA(1) observe_only
69 PMA(2) output X 72
68 PMA(2) observe_only
67 PMA(3) output X 72
66 PMA(3) observe_only
65 PMA(4) output X 72
64 PMA(4) observe_only
63 PMA(5) output X 72
62 PMA(5) observe_only
61 PMA(6) output X 72
60 PMA(6) observe_only
59 PMA(7) output X 72
58 PMA(7) observe_only
57 PMA(8) output X 72
56 PMA(8) observe_only
55 PMA(9) output X 72
54 PMA(9) observe_only
53 PMA(10) output X 72
52 PMA(10) observe_only
51 PMA(11) output X 72
50 PMA(11) observe_only
49 PMA(12) output X 72

48 PMA(12) observe_only
47 PMA(13) output X 72
46 PMA(13) observe_only
45 PMA(14) output X 72
44 PMA(14) observe_only
43 PMA(15) output X 72
42 PMA(15) observe_only
41 PMA(16) output X 72
40 PMA(16) observe_only
39 PMA(17) output X 72
38 PMA(17) observe_only
37 PMA(18) output X 72
36 PMA(18) observe_only
35 PMA(19) output X 72
34 PMA(19) observe_only
33 PMPar output X 31
32 PMPar observe_only
31 control PMPar Output Enable
30 PMCB(1) + output X 268
29 PMCB(1) + observe_only
28 PMRD_N output X 72
27 PMRD_N observe_only
26 PMCB(2) + output X 268
25 PMCB(2) + observe_only
24 PMWR_N output X 72
23 PMWR_N observe_only
22 PMCB(3) + output X 268
21 PMCB(3) + observe_only
20 PMDWR_N output
19 PMCB(4) + output X 268
18 PMCB(4) + observe_only
17 PMTS_N output
16 PMCB(5) + output X 268
15 PMCB(5) + observe_only
14 PMACK output
13 PMCB(6) + output X 268
12 PMCB(6) + observe_only
11 PMS_N(0) output X 72
10 PMS_N(0) observe_only
9 PMS_N(1) output X 72
8 PMS_N(1) observe_only
7 ClkIn observe_only
6 SysRes_N observe_only
5 Reset_N output
4 SysAv output
3 TestMode observe_only
2 ScanMode observe_only
1 TestScan observe_only
0 T1Scan input

Note: + signals available on the die, not on the package. Can be set to any state during scan.

Ordering information

Part-number	Temperature range	Package	Flow
T7904EK2-E	+25°C	MQFPF256	Engineering Samples
T7904EK2	-55° to +125°C	MQFPF256	MIL
T7904EK2/883*	-55° to +125°C	MQFPF256	MIL 883 B
T7904EK2S/883*	-55° to +125°C	MQFPF256	MIL 883 S
T7904EK2SC	-55° to +125°C	MQFPF256	SCC C
T7904EK2SB	-55° to +125°C	MQFPF256	SCC B
T7904EK2MQ	-55° to +125°C	MQFPF256	QML Q
T7904EK2SV	-55° to +125°C	MQFPF256	QML V
T7904EDD-E	+25°	Die	Engineering Samples
T7904EDDMQ	-55° to +125°	Die	QML Q
T7904EDDSV	-55° to +125°	Die	QML V

Note: (*)contact factory

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