

200mA PCI LDO

FEATURES

- Glitch-Free Transition Between Input Sources
- Automatic Input Source Selection
- External PMOS Bypass Switch Control
- Built-In 5V Detector
- 1% Regulated Output Voltage Accuracy
- 200mA Load Current Capability
- Kelvin Sense Input
- Low Dropout Voltage (240mV @ Full Load)
- Low Ground Current, Independent of Load

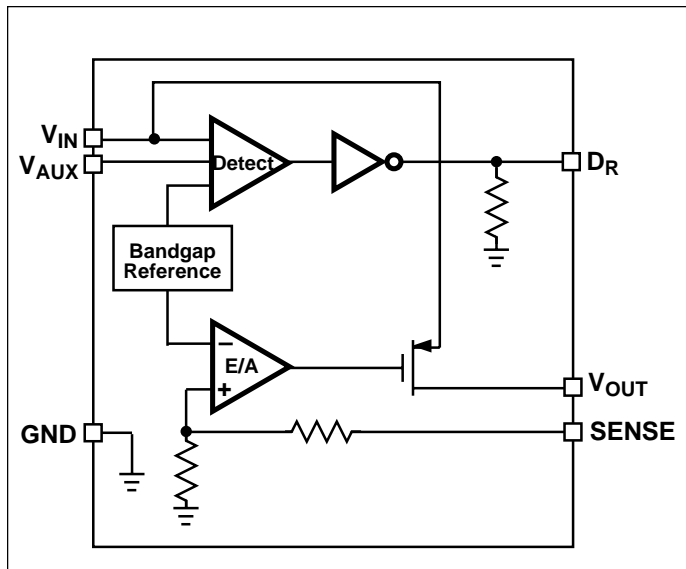
APPLICATIONS

- PCMCIA
- COMPAQ PCI
- PCI
- Network Interface Cards (NICs)
- Cardbus™ Technology

ORDERING INFORMATION

Part No.	Package	Temperature Range (Tj)
TC1266VOA	8-Pin SOIC (Narrow)	-5°C to +125°C
TC1266VUA	8-Pin MSOP	-5°C to +125°C

BLOCK DIAGRAM

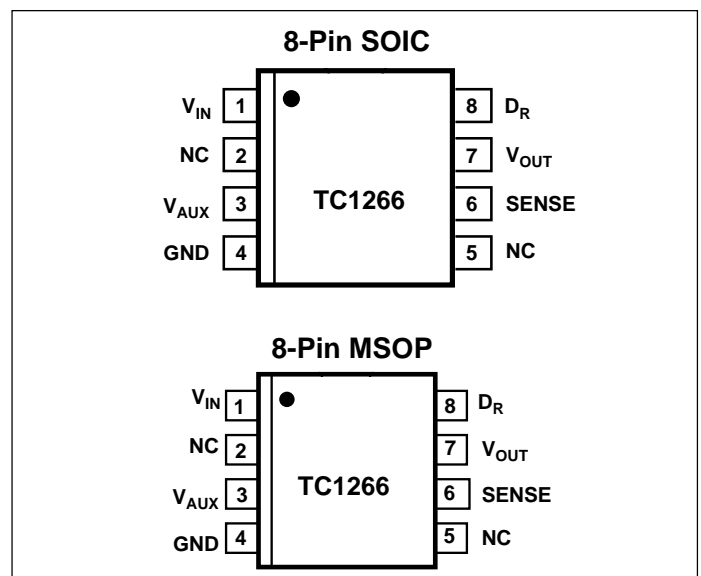


GENERAL DESCRIPTION

The TC1266 is an application-specific, low dropout regulator (LDO) specifically intended for use in PCI peripheral card applications complying with PCI Power Management (PCI 2.0). It provides an uninterrupted, 3.3V, 200mA (max) output voltage when the main (5V) or auxiliary (3.3V) input voltage supplies are present.

The TC1266 consists of an LDO, a voltage threshold detector, external switchover logic and gate drive circuitry. It functions as a conventional LDO as long as the voltage on the main supply input (V_{IN}) is above the lower threshold (3.90V typ). Should the voltage on V_{IN} fall below the lower threshold the LDO is disabled, and an external P-channel MOSFET is automatically turned on, connecting the auxiliary supply input to V_{OUT} , and ensuring an uninterrupted 3.3V output. The main supply is automatically selected if both the main and auxiliary input supplies are present, and transition from one input supply to the other is guaranteed glitch-free. High integration, automatic secondary supply switchover, Kelvin sensing, and small size make the TC1266 the optimum LDO for PCI 2.0 applications.

PIN CONFIGURATION



TC1266

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (V_{IN}) -0.5V to + 7V (Max)
Auxiliary Supply Voltage (V_{AUX}) -0.5V to + 7V (Max)
LDO Output Current (I_{OUT}) 200mA
Operating Temperature Range (T_A) -5°C to +70°C
Storage Temperature Range (T_{STG}) -65°C to +150°C
Lead Temperature (Soldering, 10 Sec) 300 °C
Thermal Impedance Junction-to-Ambient (θ_{JA}) 130°C/W for SOIC
ESD Rating 2 KV

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: $T_A = +25^\circ\text{C}$, $V_{IN} = 5\text{V}$, $V_{AUX} = 3.3\text{V}$, $I_{OUT} = 0.1\text{mA}$, $C_{OUT} = 4.7\mu\text{F}$, unless otherwise specified. Values in **BOLD** apply over full operating temperature range.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Supply Voltage	$V_{AUX} = 0\text{V}$	4.3	5.0	5.5	V
I_{GND}	GROUND Current	$V_{AUX} = 0\text{V}$, (Note 6) $V_{AUX} = 3.3\text{V}$, (Note 6)	—	230	450	μA
			—	260	500	
I_{VIN}	Reverse Leakage from V_{AUX}	$V_{AUX} = 3.6\text{V}$, $V_{IN} = 0\text{V}$, $I_{OUT} = 0\text{mA}$	—	-0.1	-1.0	μA
V_{AUX}	Supply Voltage		3.0	3.3	3.6	V
$I_{Q(AUX)}$	Quiescent Current	$V_{IN} = 0\text{V}$, $I_{OUT} = 0\text{mA}$	—	50	70	μA
		$V_{IN} = 5\text{V}$, $I_{OUT} = 0\text{mA}$	—	—	100	
			—	60	80	
			—	—	120	
I_{VAUX}	Reverse Leakage from V_{IN}	$V_{IN} = 5.5\text{V}$, $V_{AUX} = 0\text{V}$, $I_{OUT} = 0\text{mA}$	—	-0.1	-1.0	μA
$V_{TH(LO)}$	5V Detector Low Threshold Voltage	V_{IN} Falling (Notes 2, 3)	—	3.90	—	V
			3.75	—	4.05	
V_{HYST}	5V Detector Hysteresis Voltage	(Notes 2, 3)	—	260	—	mV
			200	—	300	
$V_{TH(HI)}$	5V Detector High Threshold Voltage	V_{IN} Rising (Notes 2, 3)	—	4.15	—	V
			4.0	—	4.30	
V_{OUT}	LDO Output Voltage	$I_{OUT} = 20\text{mA}$	—	3.300	—	V
		$4.3\text{V} \leq V_{IN} \leq 5.5\text{V}$, $0\text{mA} \leq I_O \leq 200\text{mA}$	3.234	—	3.366	
		$3.75\text{V} \leq V_{IN} \leq 4.3\text{V}$, $0\text{mA} \leq I_{OUT} \leq 200\text{mA}$ (Note 4)	3.000	—	—	
I_{OUT}	Output Current		200	—	—	mA
$REG_{(LINE)}$	Line Regulation	$V_{IN} = 4.3\text{V}$ to 5.5V	—	0.05	—	%
			-0.5	—	0.5	
$REG_{(LOAD)}$	Load Regulation	$I_{OUT} = 0.1\text{mA}$ to 200mA	—	0.05	—	%
			-0.5	—	0.5	

ELECTRICAL CHARACTERISTICS: $T_A = +25^\circ\text{C}$, $V_{IN} = 5\text{V}$, $V_{AUX} = 3.3\text{V}$, $I_{OUT} = 0.1\text{mA}$, $C_{OUT} = 4.7\mu\text{F}$, unless otherwise specified. Values in **BOLD** apply over full operating temperature range.

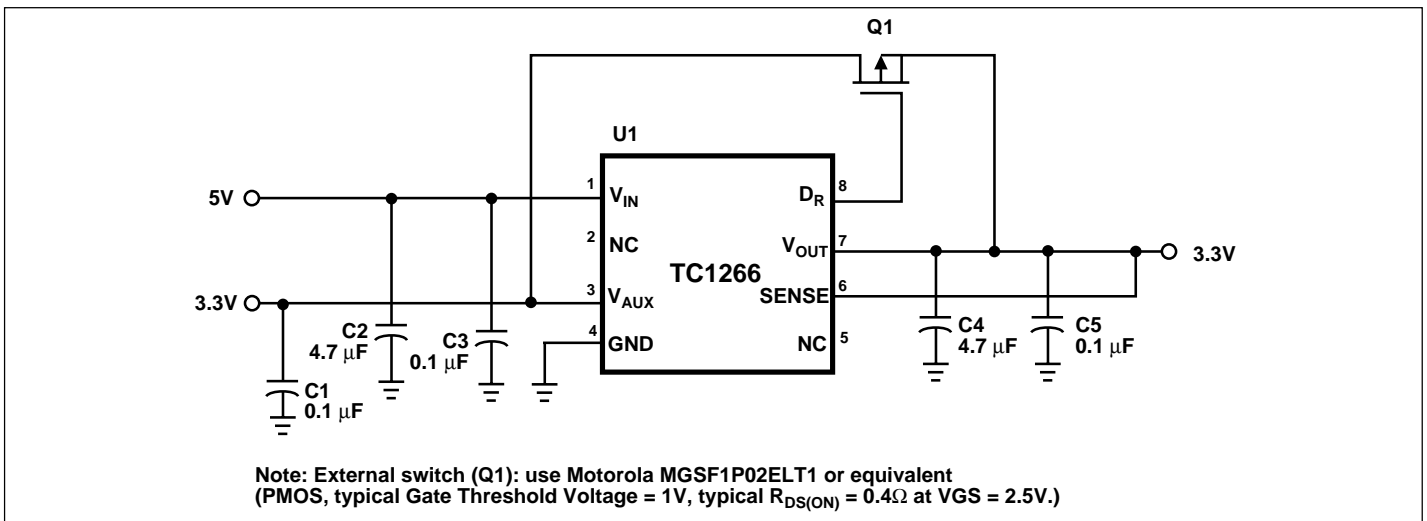
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{DR}	Drive Voltage	$4.3\text{V} \leq V_{IN} \leq 5.5\text{V}$, $I_{DR}=200\mu\text{A}$	$V_{IN} - 0.2$	$V_{IN} - 0.1$	—	V
			$V_{IN} - 0.3$	—	—	
		$V_{IN} < V_{TH(LO)}$, $I_{DR} = 200\mu\text{A}$	—	35	150	mV
			—	—	200	
$I_{DR(PK)}$	Peak Drive Current	Sinking: $V_{IN} = 3.75\text{V}$, $V_{DR} = 1\text{V}$; Sourcing: $V_{IN} = 4.3\text{V}$, $V_{IN}-V_{DR} = 2\text{V}$	7	—	—	mA
			6	—	—	
t_{DH}	Drive High Delay (Notes 1,5)	$C_{DR} = 1.2\text{ nF}$, V_{IN} ramping up, measured from $V_{IN} = V_{TH(HI)}$ to $V_{DR} = 2\text{V}$	—	4	—	μsec
			—	—	8	
t_{DL}	Drive Low Delay (Notes 1,5)	$C_{DR} = 1.2\text{ nF}$, V_{IN} ramping down, measured from $V_{IN} = V_{TH(LO)}$ to $V_{DR} = 2\text{V}$	—	0.6	1.5	μsec
			—	—	3.0	

- NOTES:**
1. Guaranteed by design.
 2. See 5V Detect Thresholds on page 4.
 3. Recommended source impedance for 5V supply; $\leq 0.25\Omega$. This will ensure that $I_{OUT} \times R_{SOURCE} < V_{HYST}$, thus avoiding D_R toggling during 5V detect threshold transitions.
 4. In application circuit below.
 5. See timing diagram on page 4.
 6. Ground current is independent of I_{LOAD} .

PIN DESCRIPTION

Pin Number	Name	Description
1	V_{IN}	Main Input Supply for the TC1266, nominally 5V.
2	NC	Not connected.
3	V_{AUX}	Auxiliary Input Supply, nominally 3.3V.
4	GND	Logic and power ground.
5	NC	Not connected.
6	SENSE	Sense Pin for V_{OUT} . Connect to V_{OUT} at the load to minimize voltage drop across PCB traces.
7	V_{OUT}	LDO 3.3V output.
8	D_R	Driver output for external P-channel MOSFET pass element.

APPLICATION CIRCUIT



TC1266

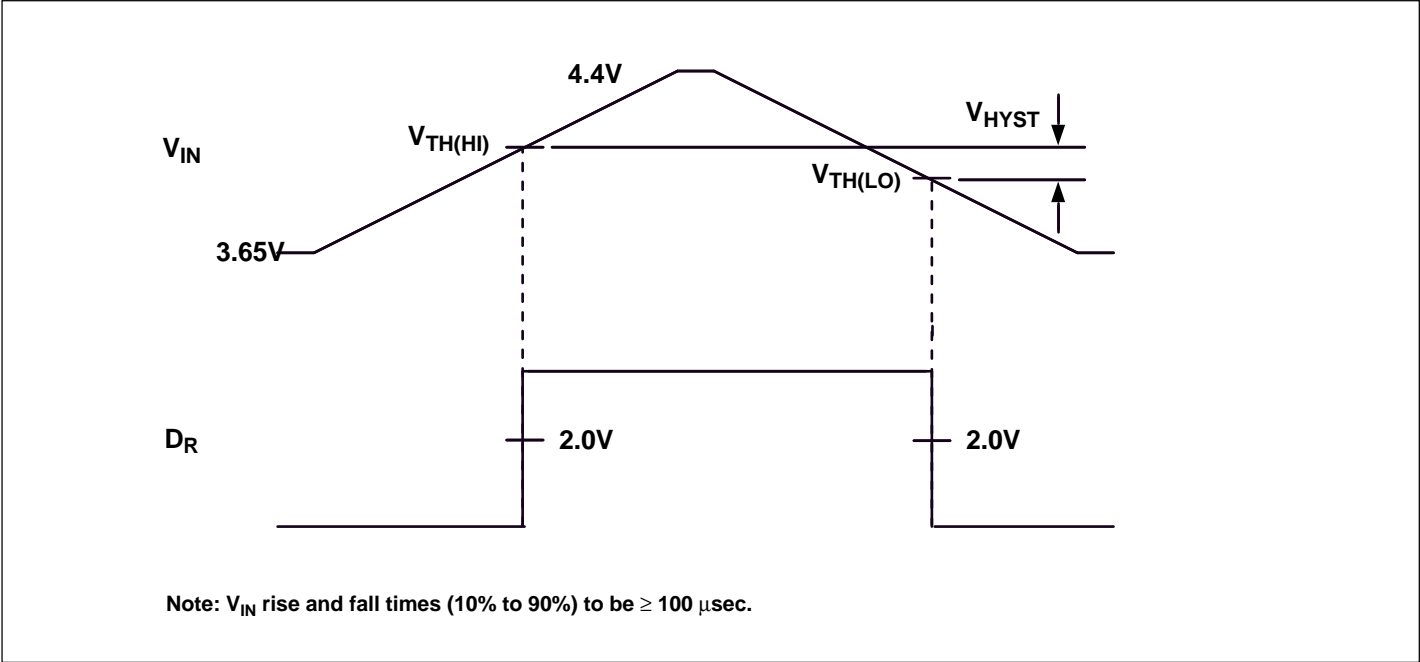


Figure 1. 5V Detect Threshold

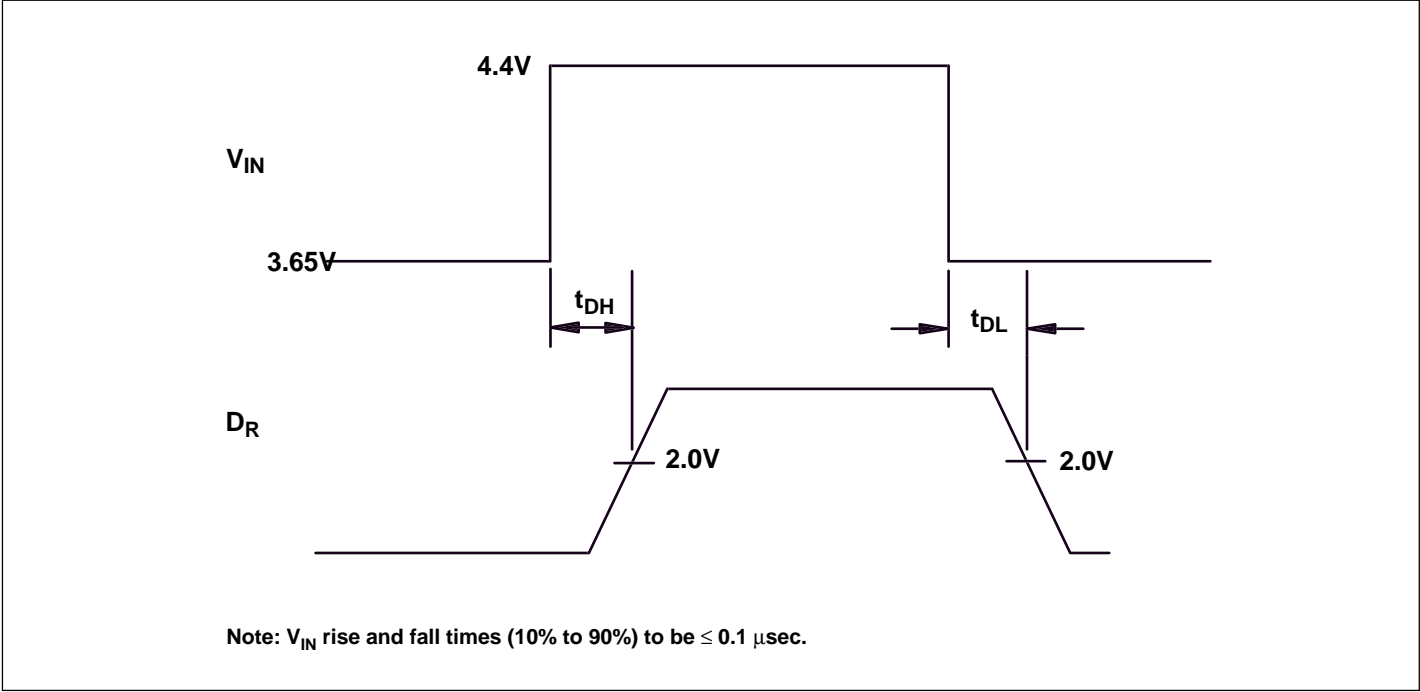
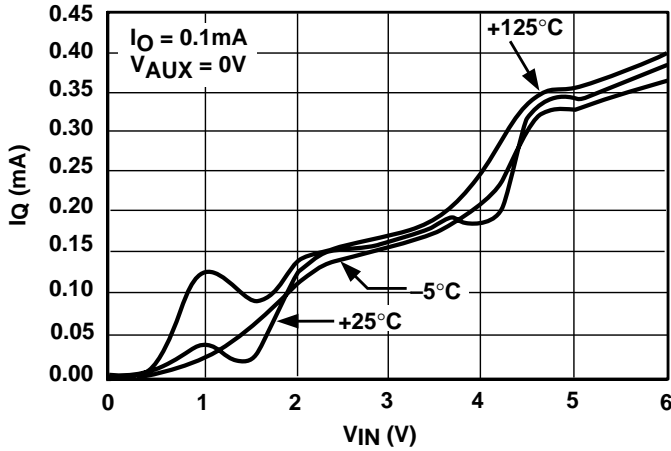


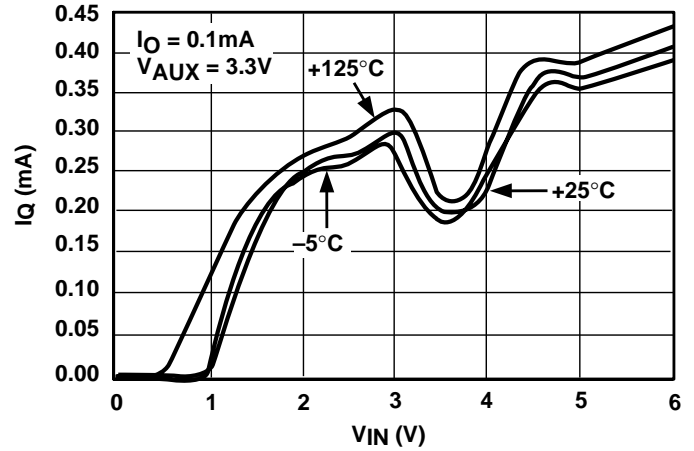
Figure 2. Timing Diagram

TYPICAL CHARACTERISTICS

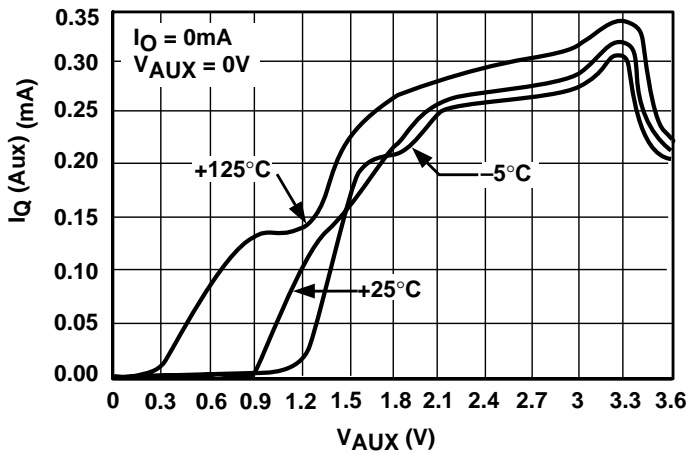
I_Q vs. V_{IN} vs. Junction Temperature



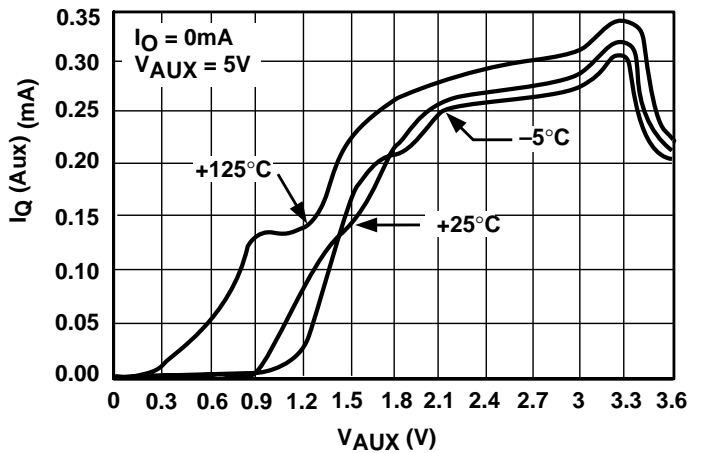
I_Q vs. V_{IN} vs. Junction Temperature



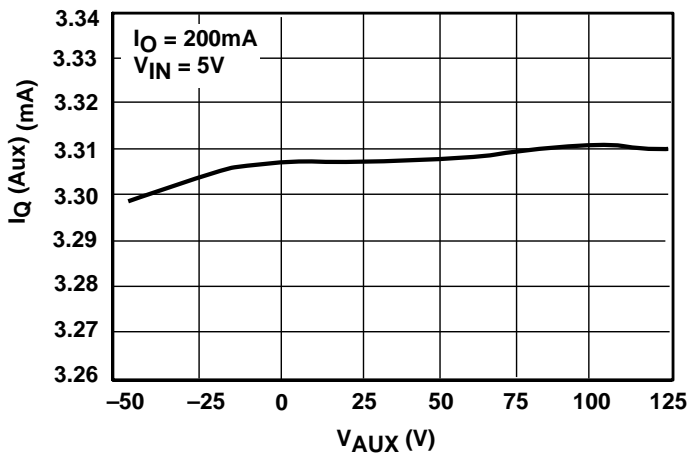
I_Q (Aux) vs. V_{AUX} vs. Junction Temperature



I_Q (Aux) vs. V_{AUX} vs. Junction Temperature



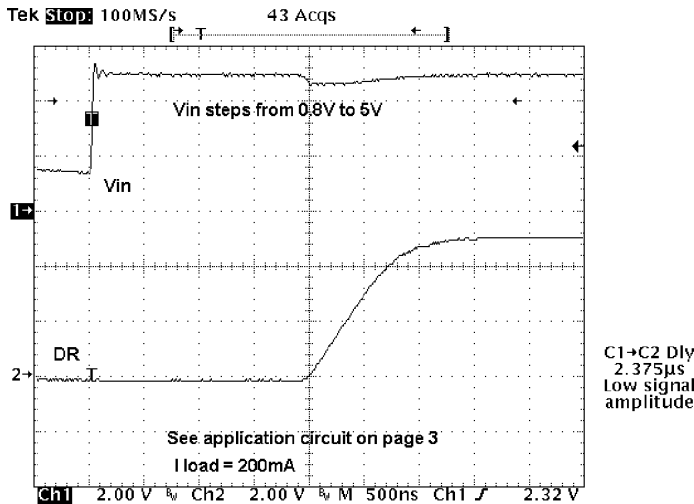
LDO Output Voltage vs. Junction Temperature



TC1266

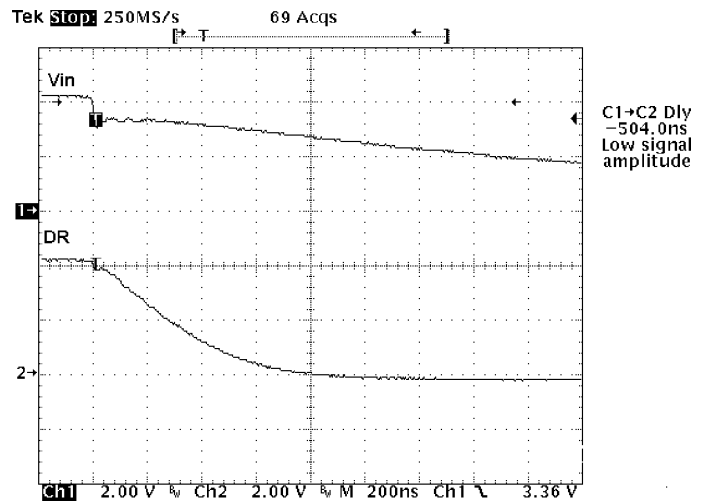
TYPICAL CHARACTERISTICS (CONT.)

Drive High Delay



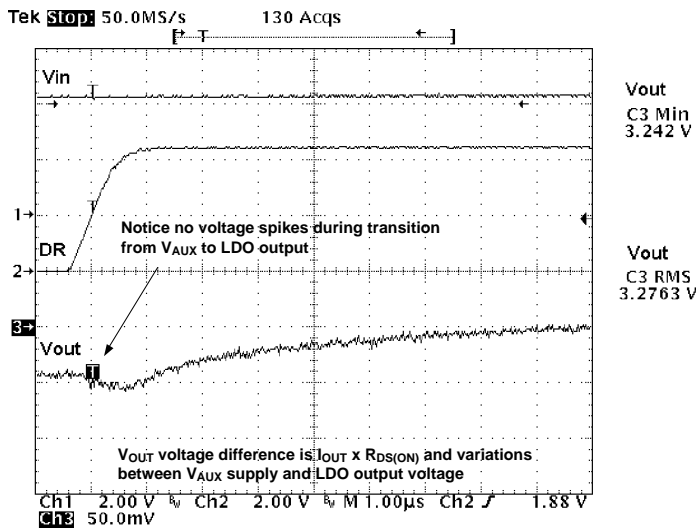
Trace 1: V_{IN} stepping for 0.8V to 5V
Trace 2: D_R going high at $V_{TH(Hi)}$
 $T_{dH} = < 4\mu S$

Drive Low Delay



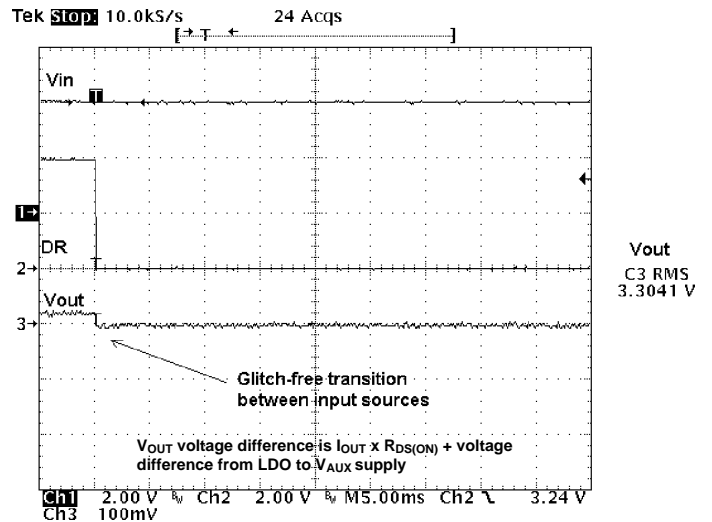
Trace 1: V_{IN} stepping for 5.5V to 0V
Trace 2: D_R going low
 $T_{dL} = < 600nS$

V_O (min) with V_{IN} Rising



Trace 1: V_{IN} – 3A charging a $1500\mu F$ capacitor
Trace 2: D_R going high at $V_{TH(Hi)}$
Trace 3: V_{OUT} , offset 3.3V. $V_{OUT} (min) = 3.24V$
 $I_{LOAD} = 20mA$

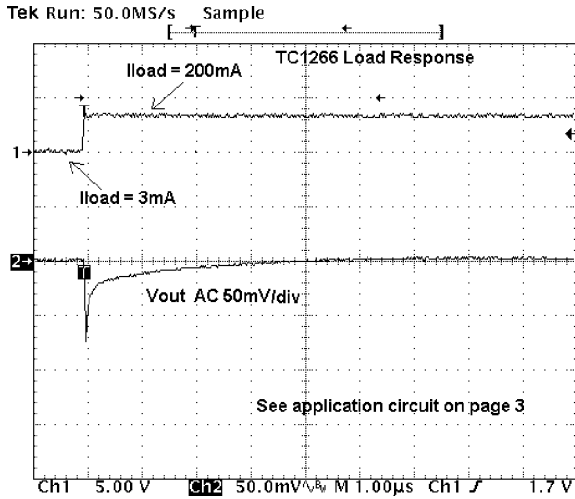
V_O (min) with V_{IN} Falling



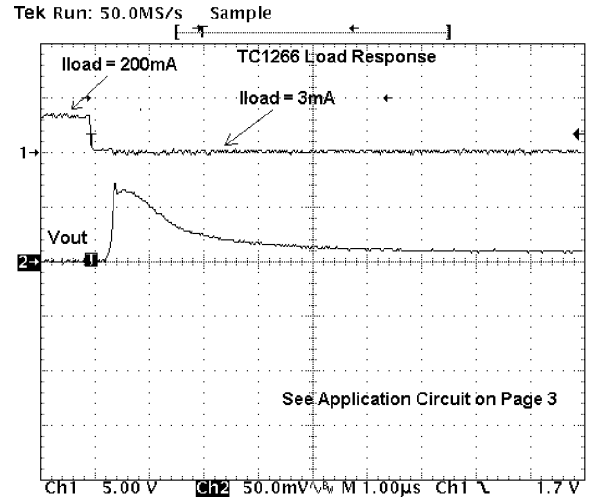
Trace 1: V_{IN} – discharging a $1500\mu F$ capacitor
Trace 2: D_R going low at $V_{TH(LO)}$
Trace 3: V_{OUT} , offset 3.3V. $V_{OUT} (min) = 3.14V$
 $I_{LOAD} = 20mA$

LOAD REGULATION

Load Response Rising Edge



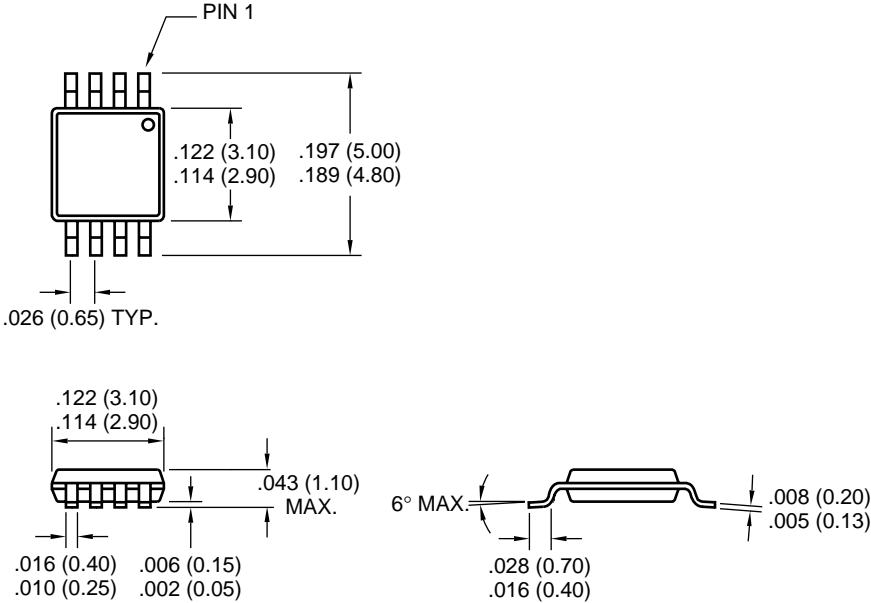
Load Response Falling Edge



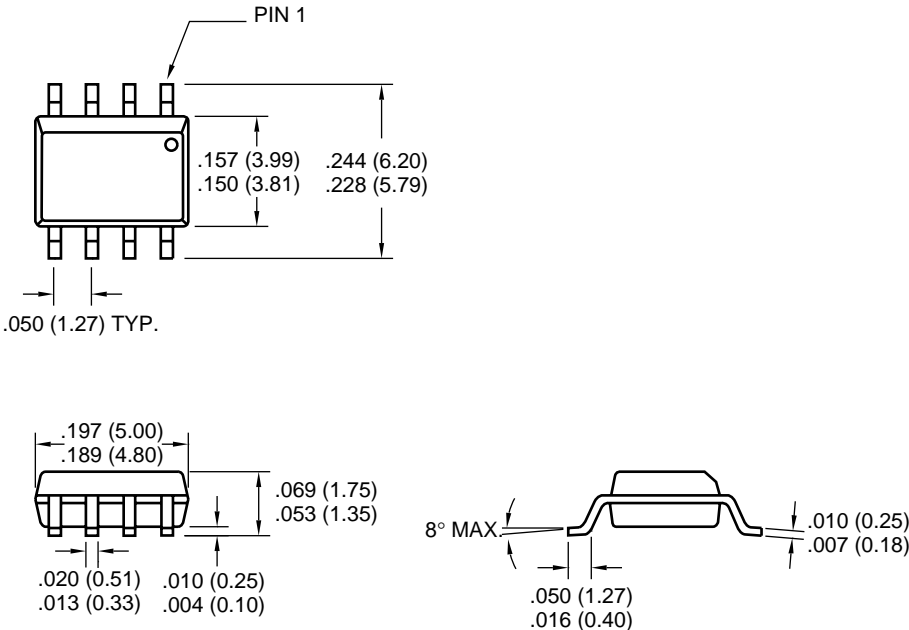
TC1266

PACKAGE DIMENSIONS

8-Pin MSOP



8-Pin SOIC (Narrow)



Dimensions: inches (mm)



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