

**TC74HC221AP, TC74HC221AF, TC74HC221AFN**

**DUAL MONOSTABLE MULTIVIBRATOR**

The TC74HC221A is a high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

There are two trigger inputs,  $\overline{A}$  input (Negative edge), and B input (Positive edge). These inputs are valid for a slow rise/fall time signal ( $t_r = t_f = 1\text{sec.}$ ) as they are schmitt trigger inputs. This device may also be triggered by using  $\overline{\text{CLR}}$  input (Positive edge).

After triggering, the output stays in a MONOSTABLE state for a time period determined by the external resistor and capacitor ( $R_x, C_x$ ). A low level at the  $\overline{\text{CLR}}$  input breaks this state.

Limits for  $C_x$  and  $R_x$  are:

- External capacitor,  $C_x$  ..... No limit
- External resistor,  $R_x$  .....  $V_{CC} = 2.0\text{V}$  more than  $5\text{k}\Omega$   
 $V_{CC} \geq 3.0\text{V}$  more than  $1\text{k}\Omega$

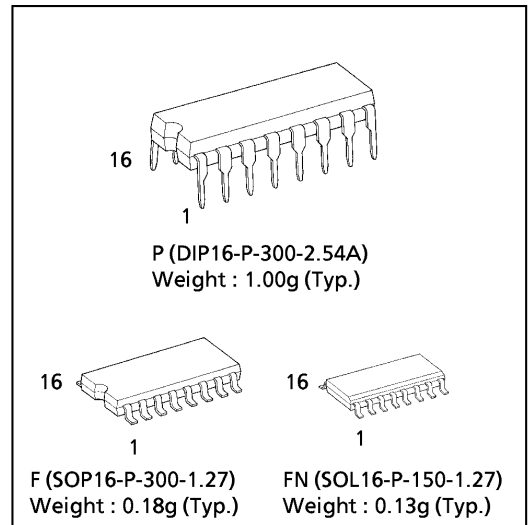
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

**FEATURES:**

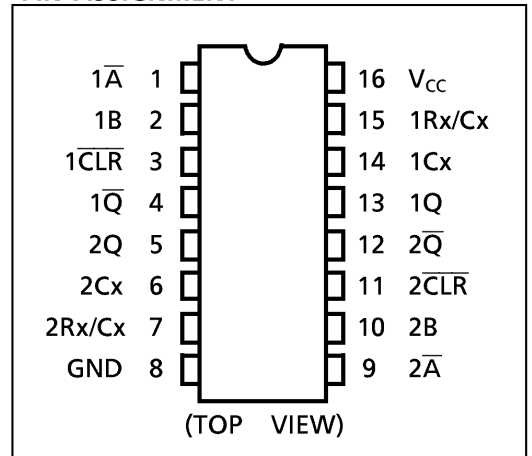
- High Speed.....  $t_{pd} = 25\text{ns}$  (typ.) at  $V_{CC} = 5\text{V}$
- Low Power Dissipation
  - Standby by State .....  $I_{CC} = 4\mu\text{A}$ (Max.) at  $T_a = 25^\circ\text{C}$
  - Active State .....  $I_{CC} = 700\mu\text{A}$ (Max.) at  $T_a = 25^\circ\text{C}$
- High Noise Immunity.....  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance...  $|I_{OH}| = I_{OL} = 4\text{mA}$ (Min.)
- Balanced Propagation Delays.....  $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range...  $V_{CC}$  (opr.) =  $2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS221

Note: In the case of using only one circuit,  $\overline{\text{CLR}}$  should be tied to GND,  $R_x / C_x \cdot C_x \cdot Q \cdot \overline{Q}$  should be tied to OPEN, the other inputs should be tied to  $V_{CC}$  or GND.

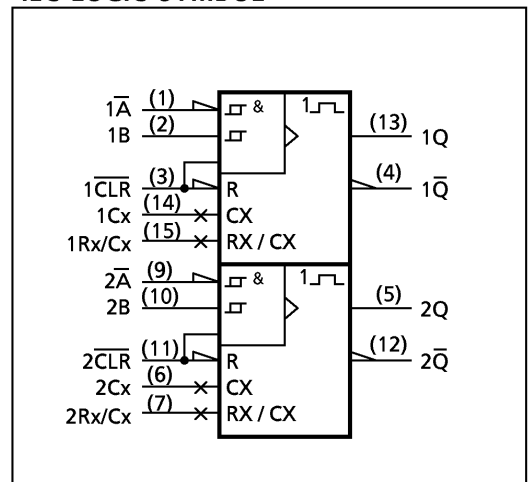
(Note) The JEDEC SOP (FN) is not available in Japan.



**PIN ASSIGNMENT**



**IEC LOGIC SYMBOL**

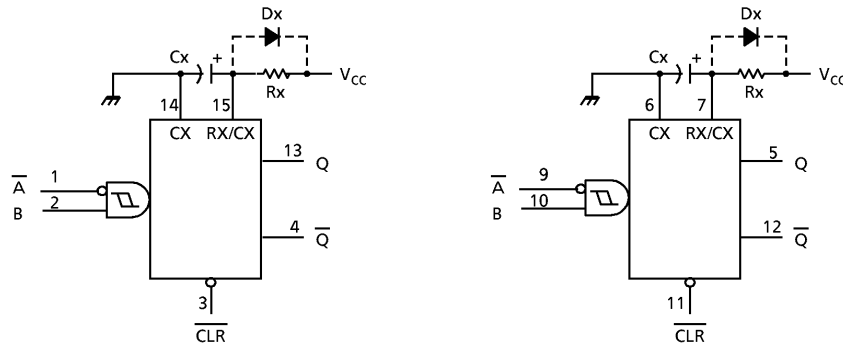


TRUTH TABLE

INPUTS			OUTPUTS		FUNCTION
$\bar{A}$	B	$\overline{\text{CLR}}$	Q	$\bar{Q}$	
	H	H			OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L		H			OUTPUT ENABLE
L	H				OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X : Don't Care

BLOCK DIAGRAM



Notes: (1) Cx, Rx, Dx are external Capacitor, Resistor, and Diode, respectively.

(2) External clamping diode, Dx;

The external capacitor is charged to V<sub>CC</sub> level in the wait state, i.e. when no trigger is applied.

If the supply voltage is turned off, Cx is discharges mainly through the internal (parasitic) diode. If Cx is sufficiently large and V<sub>CC</sub> drops rapidly, there will be some possibility of damaging the IC through in rush current or latch-up. If the capacitance of the supply voltage filter is large enough and V<sub>CC</sub> drops slowly, the in rush current is automatically limited and damage to the IC is avoided.

The maximum value of forward current through the parasitic diode is ±20mA.

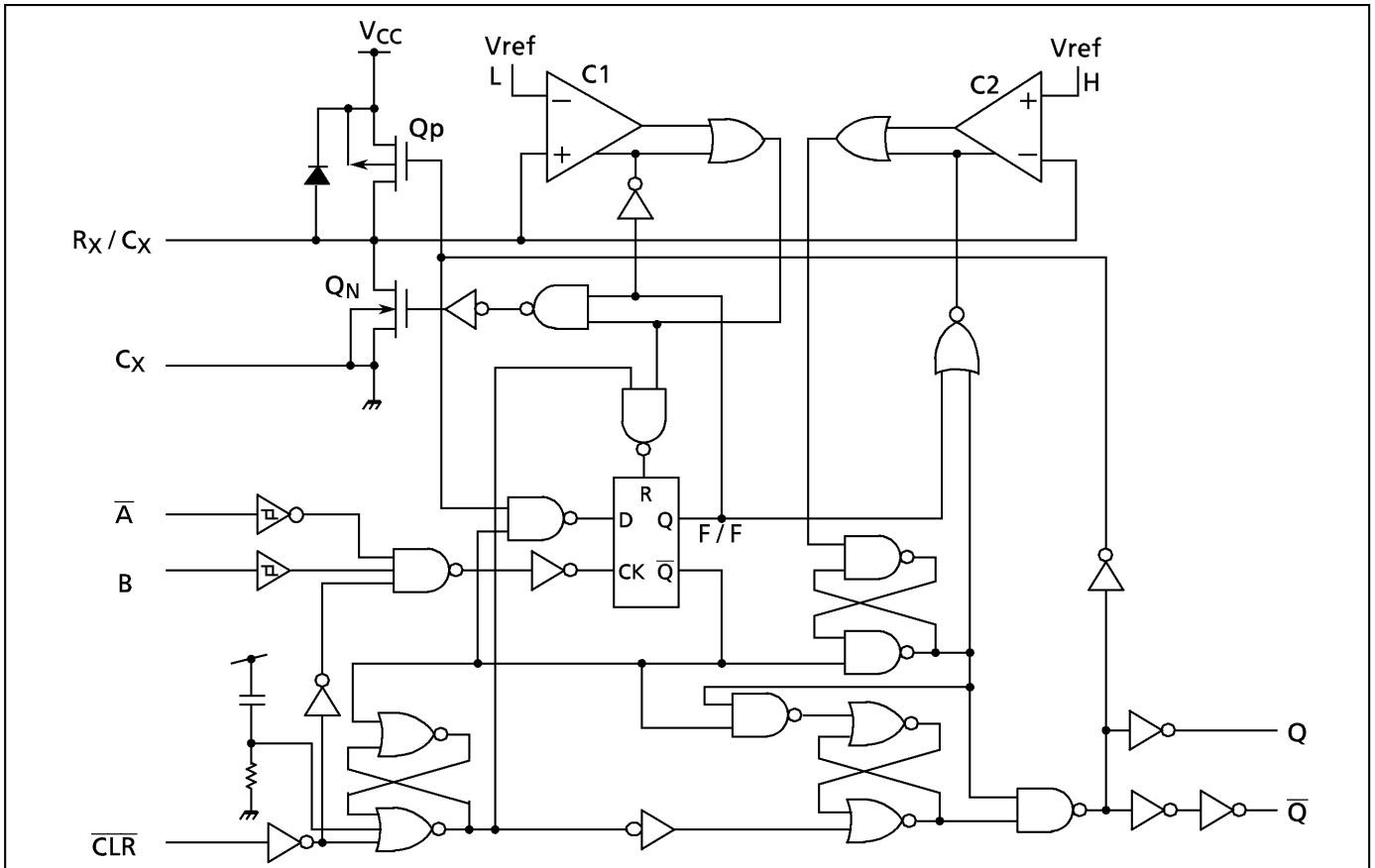
In the case of a large Cx, the limit of fall time of the supply voltage is determined as follows:

$$t_f \geq (V_{CC} - 0.7) C_x / 20\text{mA}$$

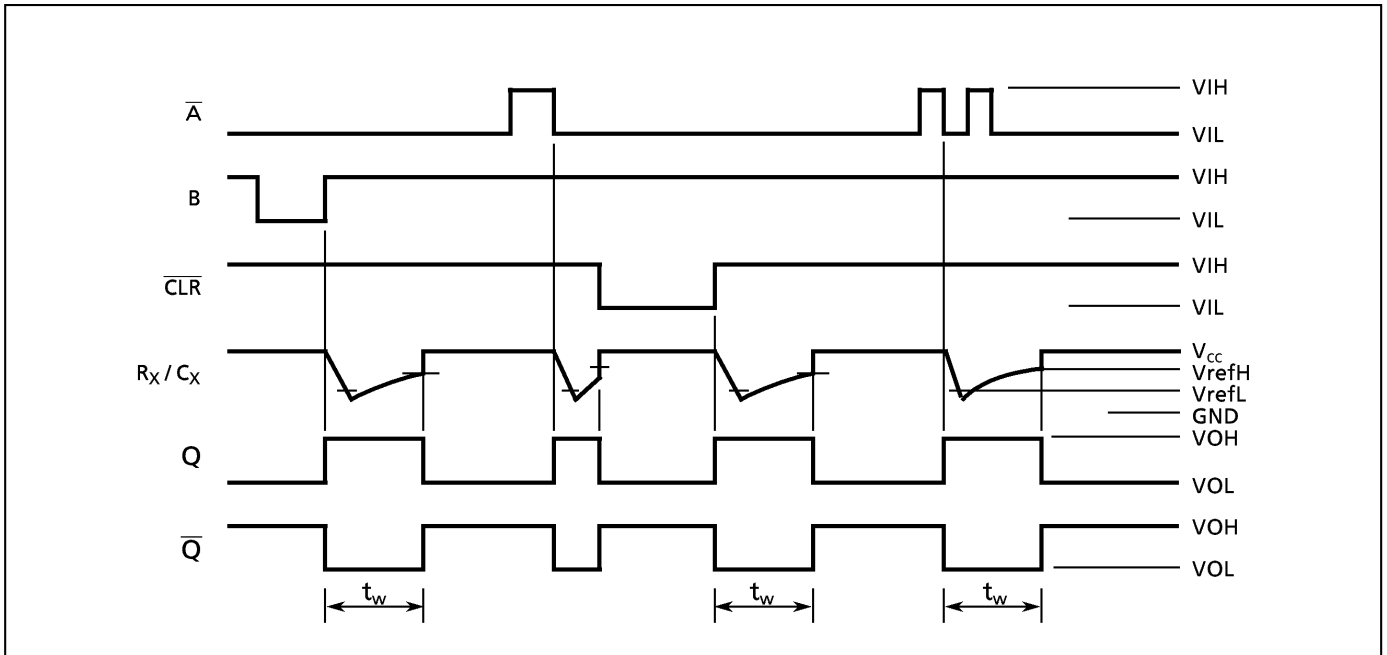
(t<sub>f</sub> is the time between the supply voltage turn off and the supply voltage reaching 0.4 V<sub>CC</sub>.)

In the even a system does not satisfy the above condition, an external clamping diode (Dx) is needed to protect the IC from rush current.

SYSTEM DIAGRAM



TIMING CHART



## FUNCTIONAL DESCRIPTION

## (1)Stand-by State

The external capacitor (Cx) is fully charged to  $V_{CC}$  in the stand-by state. That means, before triggering, the  $Q_P$  and  $Q_N$  transistors which are connected to the Rx/Cx node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies turn off. The total supply current is only leakage current.

## (2)Trigger operation

Trigger operation is effective in any of the following three cases. First the condition where the  $\overline{A}$  input is low, and the B input has a rising signal; second, where the B input is high, and the  $\overline{A}$  input has a falling signal; and third, where the  $\overline{A}$  input is low and the B input is high, and the  $\overline{CLR}$  input has a rising signal.

After a trigger becomes effective, comparators C1 and C2 start operating, and  $Q_N$  is turned on. The external capacitor discharges through  $Q_N$ . The voltage level at the Rx/Cx node drops. If the Rx/Cx voltage level falls to the internal reference voltage  $V_{refL}$ , the output of C1 becomes low. The flip-flop is then reset and  $Q_N$  turns off. At that moment C1 stops but C2 continues operating.

After  $Q_N$  turns off, the voltage at the Rx/Cx node starts rising at a rate determined by the time constant of external capacitor Cx and resistor Rx.

Upon the triggering, output Q becomes high, following some delay time of the internal F/F and gates. It stays high even if the voltage of Rx/Cx changes from falling to rising. When Rx/Cx reaches the internal reference voltage  $V_{refH}$ , the output of C2 becomes low, the output Q goes low and C2 stops its operation. That means, after triggering, when the voltage level of the Rx/Cx node reaches  $V_{refH}$ , the IC returns to its MONOSTABLE state.

With large values of Cx and Rx, and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse,  $t_w$  (OUT), is as follows:

$$t_w(\text{OUT}) = 1.0 C_x R_x$$

## (3)Reset operation

In normal operation,  $\overline{CLR}$  input is held high. If  $\overline{CLR}$  is low, a trigger has no effect because the Q output is held low and trigger control F/F is reset. Also,  $Q_P$  turns on and Cx is charge rapidly to  $V_{CC}$ .

This means if  $\overline{CLR}$  input is set low, the IC goes into a wait state.

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7	V
DC Input Voltage	$V_{IN}$	-0.5~ $V_{CC}+0.5$	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC}+0.5$	V
Input Diode Current	$I_{IK}$	$\pm 20$	mA
Output Diode Current	$I_{OK}$	$\pm 20$	mA
DC Output Current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ / Ground Current	$I_{CC}$	$\pm 50$	mA
Power Dissipation	$P_D$	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	$T_{stg}$	-65~150	°C

\*500mW in the range of  $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$ . From  $T_a = 65^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  a derating factor of  $-10\text{mW}/^{\circ}\text{C}$  shall be applied until 300mW.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	2~6	V
Input Voltage	$V_{IN}$	0~ $V_{CC}$	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time (CLR Only)	$t_r, t_f$	0~1000 ( $V_{CC} = 2.0\text{V}$ ) 0~500 ( $V_{CC} = 4.5\text{V}$ ) 0~400 ( $V_{CC} = 6.0\text{V}$ )	ns
External Capacitor	$C_x$	No Limitation *	F
External Resistor	$R_x$	$\geq 5\text{K} * (V_{CC} = 2.0\text{V})$ $\geq 1\text{K} * (V_{CC} \geq 3.0\text{V})$	$\Omega$

\* The maximum allowable values of  $C_x$  and  $R_x$  are a function of leakage of capacitor  $C_x$ , the leakage of TC74HC221A, and leakage due to board layout and surface resistance.

Susceptibility to externally induced noise signals may occur for  $R_x > 1\text{M}\Omega$ .

**DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V <sub>IH</sub>		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V	
Low - Level Input Voltage	V <sub>IL</sub>		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V	
High - Level Output Voltage (Q, $\bar{Q}$ )	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
			6.0	5.9	6.0	—	5.9	—		
			4.5	4.18	4.31	—	4.13	—		
			6.0	5.68	5.80	—	5.63	—		
Low - Level Output Voltage (Q, $\bar{Q}$ )	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
			6.0	—	0.0	0.1	—	0.1		
			4.5	—	0.17	0.26	—	0.33		
			6.0	—	0.18	0.26	—	0.33		
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	6.0	—	—	± 0.1	—	± 1.0	μA	
Rx / Cx Terminal Off - State Current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	6.0	—	—	± 0.1	—	± 1.0		
Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	6.0	—	—	4.0	—	40.0		
Active - State * Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND Rx / Cx = 0.5 V <sub>CC</sub>	2.0	—	45	200	—	260	μA	
			4.5	—	400	500	—	650	μA	
			6.0	—	0.7	1.0	—	1.3	mA	

\* : per circuit

**TIMING REQUIREMENTS ( Input t<sub>r</sub> = t<sub>f</sub> = 6ns )**

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	Ta = 25°C		Ta = -40~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width	t <sub>W(L)</sub> t <sub>W(H)</sub>		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Clear Width	t <sub>W(L)</sub>		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 15pF, V<sub>CC</sub> = 5V, Ta = 25°C, Input t<sub>r</sub> = t<sub>f</sub> = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t <sub>TLH</sub> t <sub>THL</sub>		—	4	8	ns
Propagation Delay Time ( $\bar{A}$ , B—Q, $\bar{Q}$ )	t <sub>pLH</sub> t <sub>pHL</sub>		—	25	36	
Propagation Delay Time (CLR TRIGGER—Q, $\bar{Q}$ )	t <sub>pLH</sub> t <sub>pHL</sub>		—	25	41	
Propagation Delay Time ( $\bar{CLR}$ —Q, $\bar{Q}$ )	t <sub>pLH</sub> t <sub>pHL</sub>		—	16	27	

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50pF, Input t<sub>r</sub> = t<sub>f</sub> = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT	
			V <sub>CC</sub> (V)	MIN.	TYP.	MAX.	MIN.		MAX.
Output Transition Time	t <sub>TLH</sub> t <sub>THL</sub>		2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation Delay Time ( $\bar{A}$ , B—Q, $\bar{Q}$ )	t <sub>pLH</sub> t <sub>pHL</sub>		2.0	—	102	210	—	265	ns
			4.5	—	30	42	—	53	
			6.0	—	24	36	—	45	
Propagation Delay Time (CLR TRIGGER—Q, $\bar{Q}$ )	t <sub>pLH</sub> t <sub>pHL</sub>		2.0	—	102	235	—	295	ns
			4.5	—	30	47	—	59	
			6.0	—	24	40	—	50	
Propagation Delay Time ( $\bar{CLR}$ —Q, $\bar{Q}$ )	t <sub>pLH</sub> t <sub>pHL</sub>		2.0	—	67	160	—	200	ns
			4.5	—	20	32	—	40	
			6.0	—	16	27	—	34	
Output Pulse Width	tw <sub>OUT</sub>	Cx = 28pF Rx = 6KΩ (V <sub>CC</sub> = 2V)	2.0	—	700	2000	—	2500	ns
			4.5	—	250	400	—	500	
			6.0	—	210	340	—	425	
		Cx = 0.01μF Rx = 10KΩ	2.0	90	110	130	90	130	μs
			4.5	95	105	115	95	115	
			6.0	95	105	115	95	115	
		Cx = 0.1μF Rx = 10KΩ	2.0	0.9	1.0	1.2	0.9	1.2	ms
			4.5	0.9	1.0	1.1	0.9	1.1	
			6.0	0.9	1.0	1.1	0.9	1.1	
Output Pulse Width Error Between Circuits (In same Package)	Δtw <sub>OUT</sub>		—	±1	—	—	—	%	
Input Capacitance	C <sub>IN</sub>		—	5	10	—	10	pF	
Power Dissipation Capacitance	C <sub>PD</sub> (1)		—	174	—	—	—		

Note (1) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

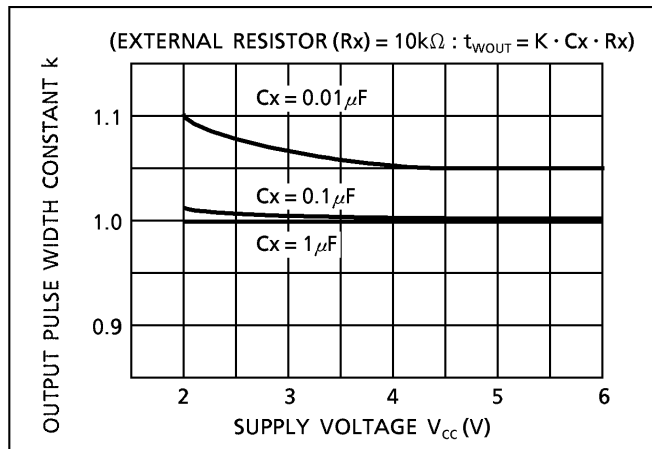
Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot \text{Duty} / 100 + I_{CC} / 2 \text{ (per circuit)}$$

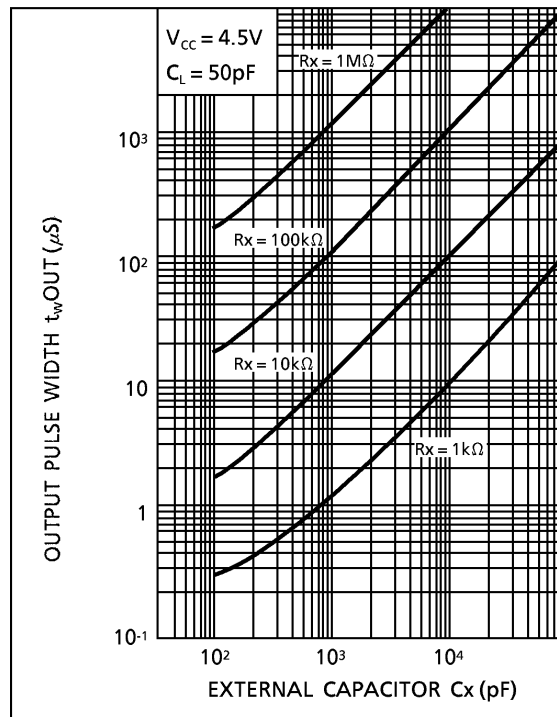
(I<sub>CC</sub>' : Active Supply Current)

(Duty : %)

OUTPUT PULSE WIDTH CONSTANT K- SUPPLY VOLTAGE ( TYPICAL )



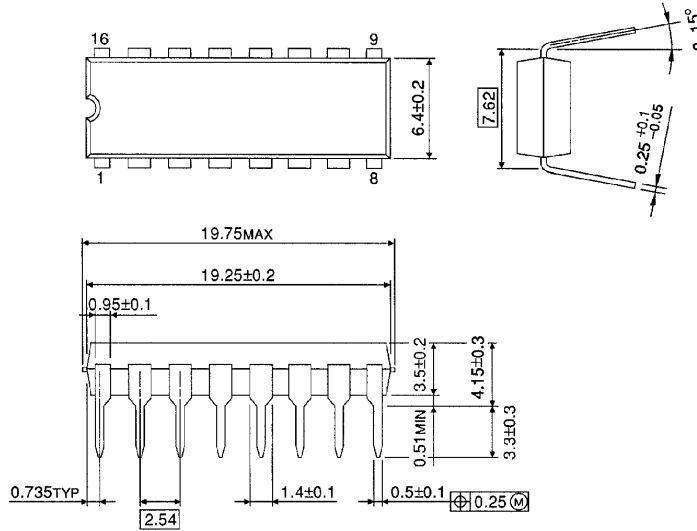
$t_{wOUT} - Cx$  CHARACTERISTICS ( TYP. )





**DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)**

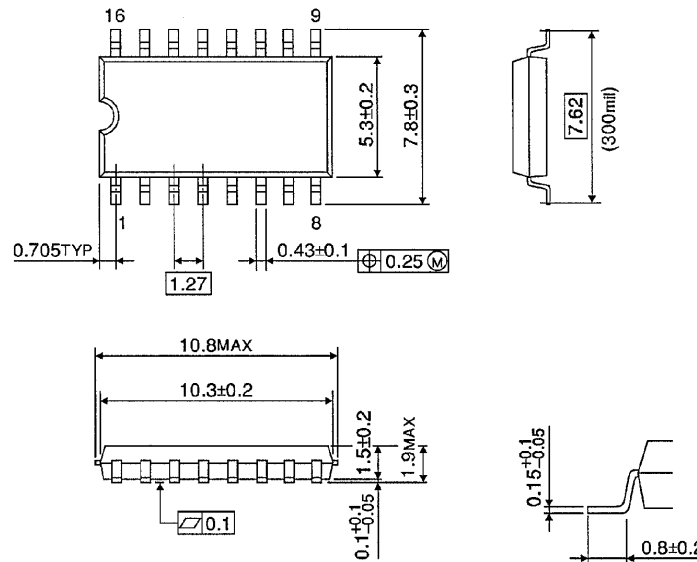
Unit in mm



Weight : 1.00g (Typ.)

**SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)**

Unit in mm

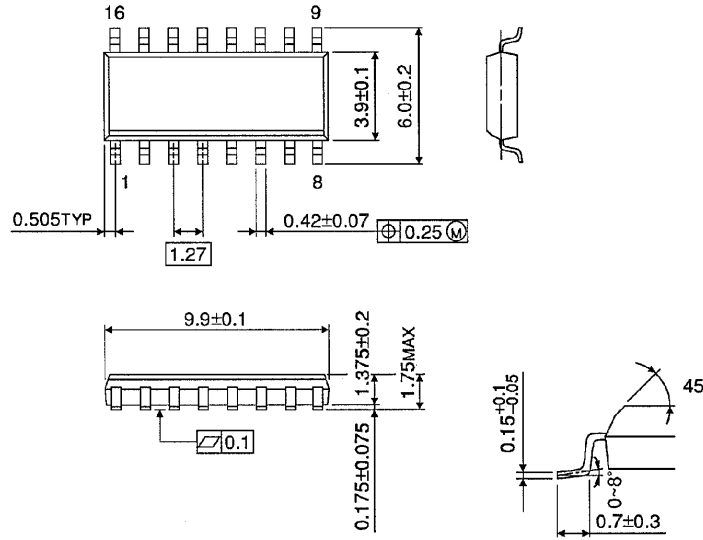


Weight : 0.18g (Typ.)

**SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150 -1.27)**

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

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000707EBA

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