TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74LCX540F,TC74LCX540FW,TC74LCX540FT

Low-Voltage Octal Bus Buffer (inverted) with 5-V Tolerant Inputs and Outputs

Note: xxxFW (JEDEC SOP) is not available in Japan.

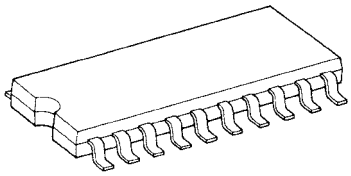
The TC74LCX540F/FW/FT is a high-performance CMOS octal bus buffer. Designed for use in 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3 V) V_{CC} applications, but it could be used to interface to 5 V supply environment for both inputs and outputs.

The TC74LCX540F/FW/FT is an inverting 3-state buffer having two active-low output enables. When either $\overline{OE}1$ or $\overline{OE}2$ are high, the terminal outputs are in the high-impedance state. This device is designed to be used with 3-state memory address drivers, etc.

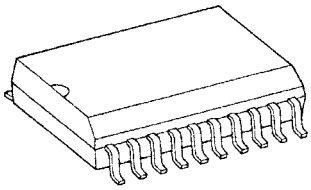
All inputs are equipped with protection circuits against static discharge.

TC74LCX540F



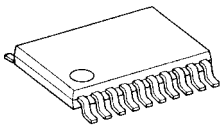
SOP20-P-300-1.27

TC74LCX540FW



SOL20-P-300-1.27

TC74LCX540FT



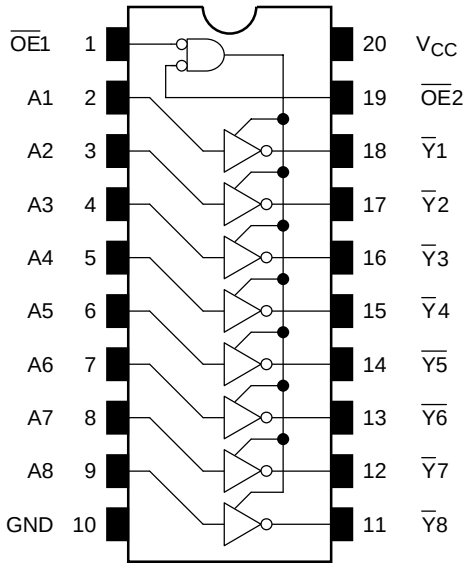
TSSOP20-P-0044-0.65

Weight
SOP20-P-300-1.27: 0.22 g (typ.)
SOL20-P-300-1.27: 0.46 g (typ.)
TSSOP20-P-0044-0.65: 0.08 g (typ.)

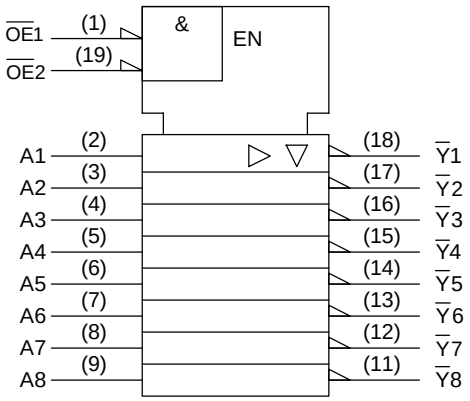
Features

- Low-voltage operation: V_{CC} = 2.0 to 3.6 V
- High-speed operation: t_{pd} = 6.5 ns (max) (V_{CC} = 3.0 to 3.6 V)
- Output current: $|I_{OH}|/I_{OL}$ = 24 mA (min) (V_{CC} = 3.0 V)
- Latch-up performance: ±500 mA
- Available in JEDEC SOP, JEITA SOP and TSSOP
- Power-down protection provided on all inputs and outputs
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 540 type

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

Inputs			Outputs
$\overline{OE}1$	$\overline{OE}2$	An	
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

X: Don't care

Z: High impedance

Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.5 to 7.0	V
DC input voltage	V_{IN}	−0.5 to 7.0	V
DC output voltage	V_{OUT}	−0.5 to 7.0 (Note 1) −0.5 to V_{CC} + 0.5 (Note 2)	V
Input diode current	I_{IK}	−50	mA
Output diode current	I_{OK}	±50 (Note 3)	mA
DC output current	I_{OUT}	±50	mA
Power dissipation	P_D	180	mW
DC V_{CC}/ground current	I_{CC}/I_{GND}	±100	mA
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Output in OFF state

Note 2: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 3: $V_{OUT} < GND$, $V_{OUT} > VCC$

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	2.0 to 3.6	V
		1.5 to 3.6 (Note 4)	
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to 5.5 (Note 5)	V
		0 to V_{CC} (Note 6)	
Output current	I_{OH}/I_{OL}	±24 (Note 7)	mA
		±12 (Note 8)	
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 9)	ns/V

Note 4: Data retention only

Note 5: Output in OFF state

Note 6: High or low state

Note 7: V_{CC} = 3.0 to 3.6 V

Note 8: V_{CC} = 2.7 to 3.0 V

Note 9: V_{IN} = 0.8 to 2.0 V, V_{CC} = 3.0 V

Electrical Characteristics

DC Characteristics (Ta = –40 to 85°C)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	H-level	V_{IH}	—		2.7 to 3.6	2.0	—	V
	L-level	V_{IL}	—		2.7 to 3.6	—	0.8	
Output voltage	H-level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA	2.7 to 3.6	V_{CC} − 0.2	—	V
				I_{OH} = −12 mA	2.7	2.2	—	
				I_{OH} = −18 mA	3.0	2.4	—	
				I_{OH} = −24 mA	3.0	2.2	—	
	L-level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.7 to 3.6	—	0.2	
				I_{OL} = 12 mA	2.7	—	0.4	
				I_{OL} = 16 mA	3.0	—	0.4	
				I_{OL} = 24 mA	3.0	—	0.55	
Input leakage current		I_{IN}	V_{IN} = 0 to 5.5 V		2.7 to 3.6	—	±5.0	μA
3-state output off-state current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 5.5 V		2.7 to 3.6	—	±5.0	μA
Power off leakage current		I_{OFF}	V_{IN}/V_{OUT} = 5.5 V		0	—	10.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		2.7 to 3.6	—	10.0	μA
			V_{IN}/V_{OUT} = 3.6 to 5.5 V		2.7 to 3.6	—	±10.0	
Increase in I_{CC} per input		ΔI_{CC}	V_{IH} = V_{CC} − 0.6 V		2.7 to 3.6	—	500	

AC Characteristics (Ta = –40 to 85°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Propagation delay time	t_{pLH} t_{pHL}	Figure 1, Figure 2	2.7	—	7.5	ns
			3.3 ± 0.3	1.5	6.5	
Output enable time	t_{pZL} t_{pZH}	Figure 1, Figure 3	2.7	—	9.5	ns
			3.3 ± 0.3	1.5	8.5	
Output disable time	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	2.7	—	8.5	ns
			3.3 ± 0.3	1.5	7.5	
Output to output skew	t_{osLH} t_{osHL}	(Note 10)	2.7	—	—	ns
			3.3 ± 0.3	—	1.0	

Note 10: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

Dynamic Switching Characteristics
(Ta = 25°C, input: $t_r = t_f = 2.5$ ns, $C_L = 50$ pF, $R_L = 500\ \Omega$)

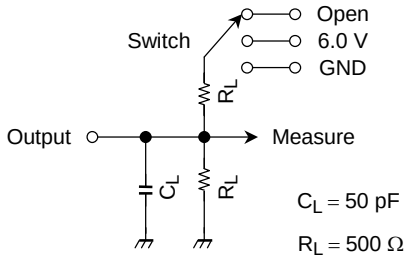
Characteristics		Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Quiet output maximum dynamic	V_{OL}	V_{OLP}	V_{IH} = 3.3 V, V_{IL} = 0 V	3.3	0.8	V
Quiet output minimum dynamic	V_{OL}	$\|V_{OLV}\|$	V_{IH} = 3.3 V, V_{IL} = 0 V	3.3	0.8	V

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Input capacitance	C_{IN}	—	3.3	7	pF
Output capacitance	C_{OUT}	—	3.3	8	pF
Power dissipation capacitance	C_{PD}	f_{IN} = 10 MHz (Note 11)	3.3	40	pF

Note 11: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.
Average operating current can be obtained by the equation:
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per bit)

AC Test Circuit



Parameter	Switch
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	6.0 V
t_{pHZ}, t_{pZH}	GND

Figure 1

AC Waveform

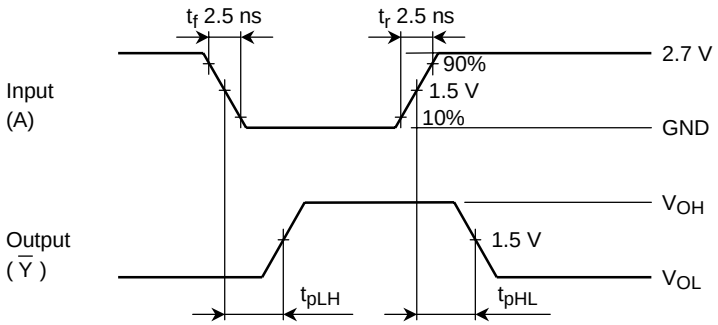


Figure 2 t_{pLH}, t_{pHL}

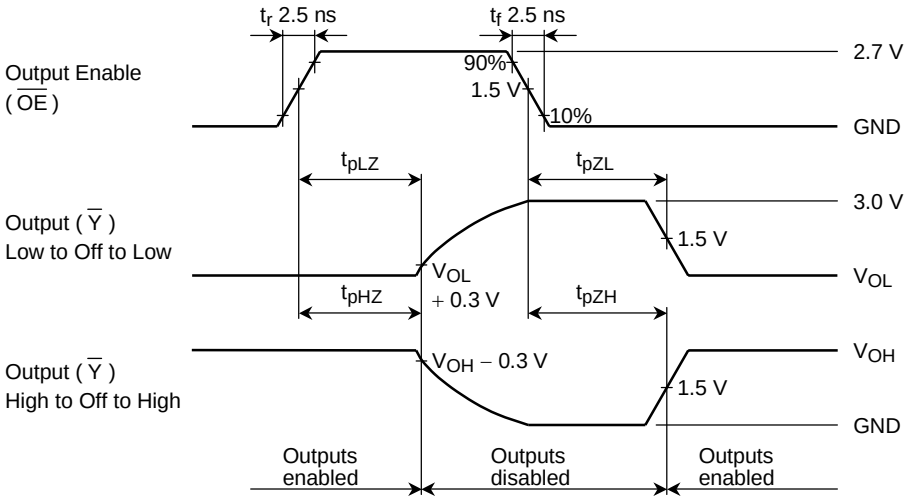
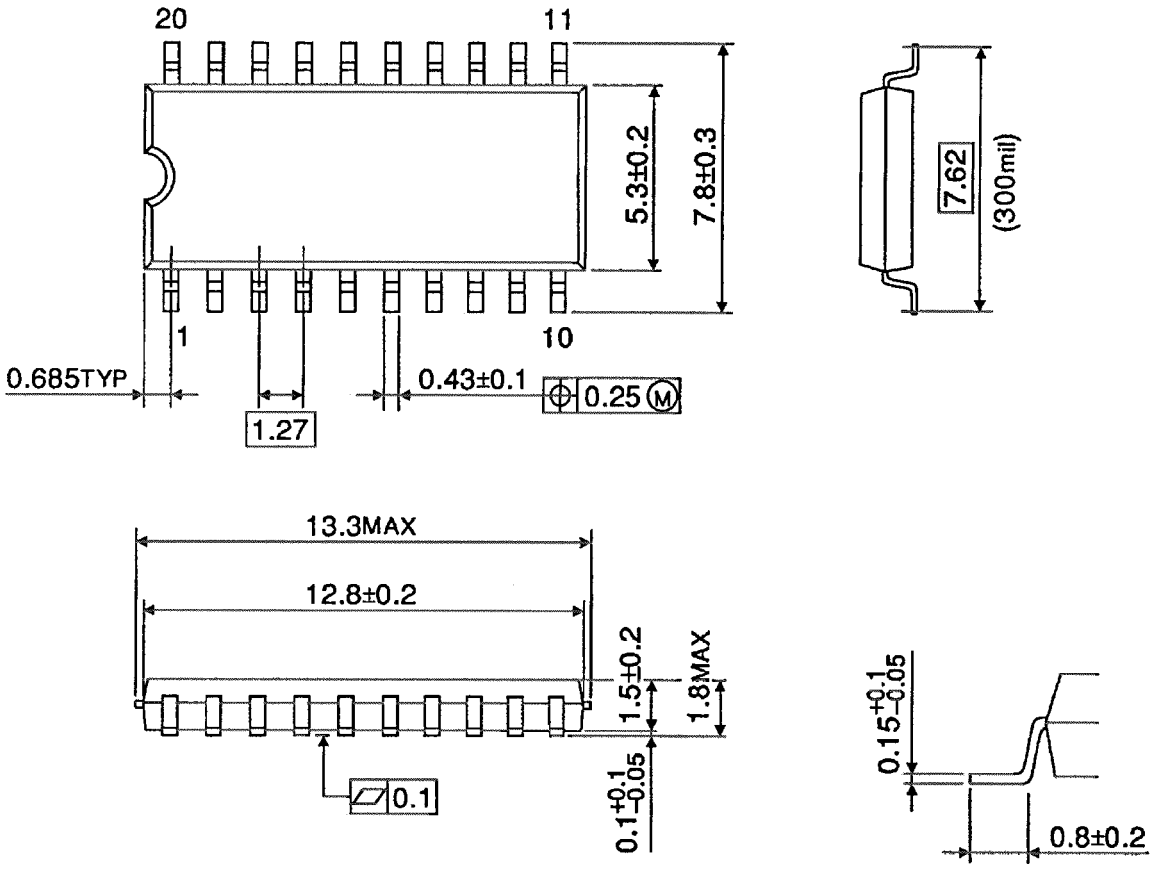


Figure 3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

Package Dimensions

SOP20-P-300-1.27 Unit : mm



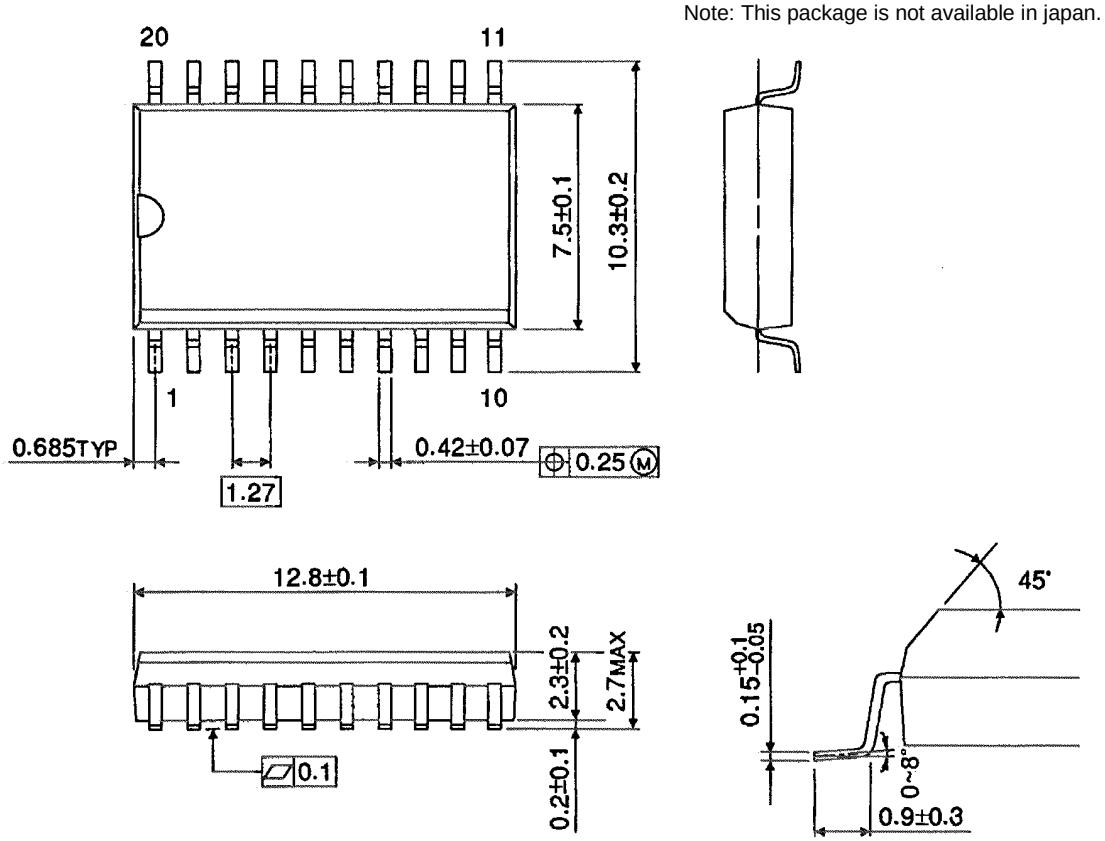
Weight: 0.22 g (typ.)

Package Dimensions

SOL20-P-300-1.27

Unit : mm

Note: This package is not available in japan.

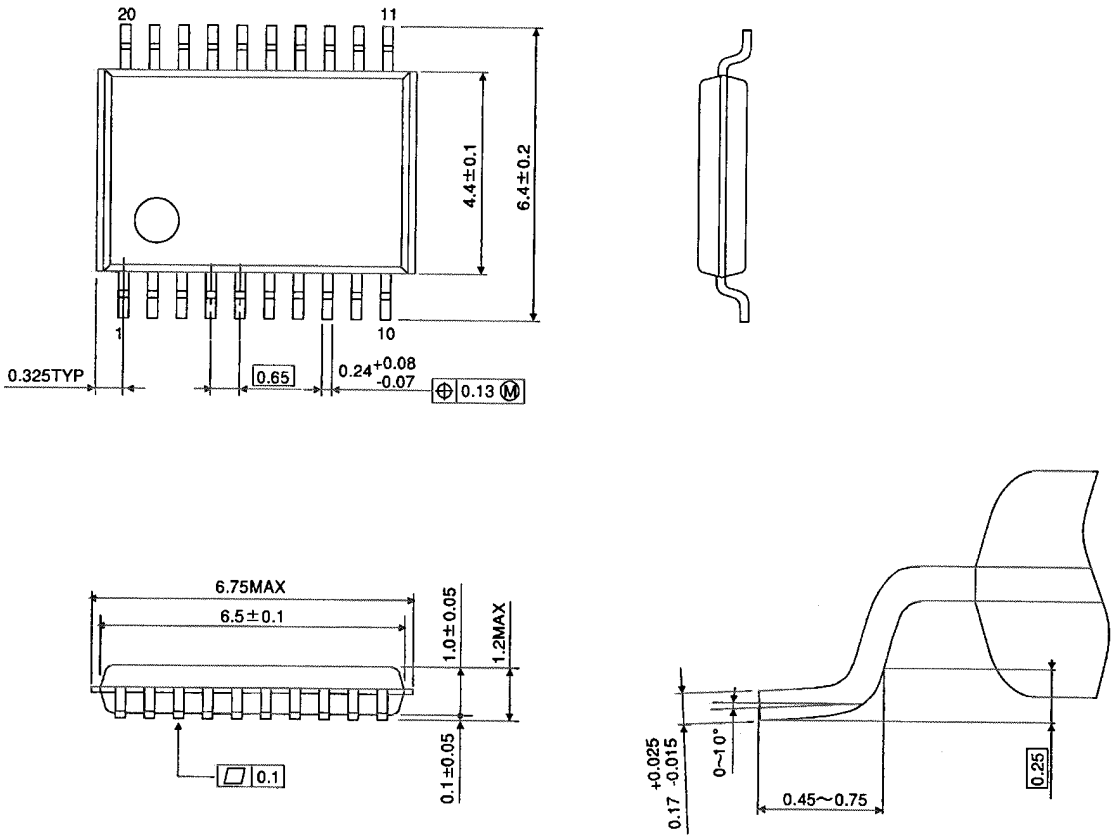


Weight: 0.46 g (typ.)

Package Dimensions

TSSOP20-P-0044-0.65

Unit : mm



Weight: 0.08 g (typ.)

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