TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74LVX174F,TC74LVX174FN,TC74LVX174FT

Hex D-Type Flip-Flop with Clear

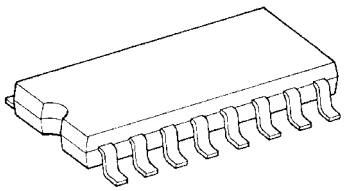
Note: xxxFN (JEDEC SOP) is not available in Japan.

The TC74LVX174F/ FN/ FT is a high-speed CMOS hex D-flip flop fabricated with silicon gate CMOS technology. Designed for use in 3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.

Information signals applied to D inputs are transfered to the Q output on the positivegoing edge of the clock pulse. When the $\overline{CLR}$ input is held low, the Q output are in the low logic level independent of the other inputs.

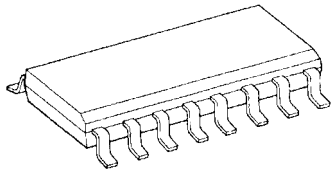
An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

TC74LCX174F



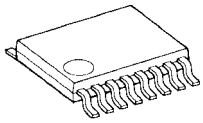
SOP16-P-300-1.27

TC74LCX174FN



SOL16-P-150-1.27

TC74LCX174FT



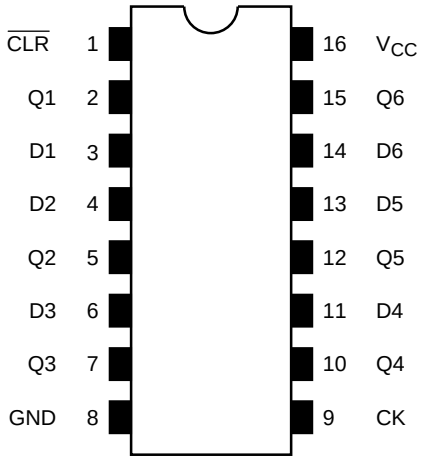
TSSOP16-P-0044-0.65

Weight
SOP16-P-300-1.27: 0.18 g (typ.)
SOL16-P-150-1.27: 0.12 g (typ.)
TSSOP16-P-0044-0.65: 0.06 g (typ.)

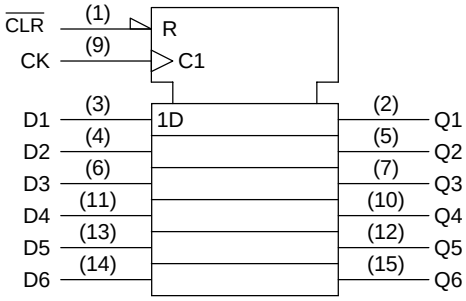
Features

- High-speed: f_{max} = 180 MHz (typ.) (V_{CC} = 3 V)
- Low power dissipation: I_{CC} = 4 μA (max) (Ta = 25°C)
- Input voltage level: V_{IL} = 0.8 V (max) (V_{CC} = 3 V)
  V_{IH} = 2.0 V (min) (V_{CC} = 3 V)
- Power-down protection provided on all inputs
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Low niose: V_{OLP} = 0.5 V (max)
- Pin and function compatible with 74HC174

Pin Assignment (top view)



IEC Logic Symbol

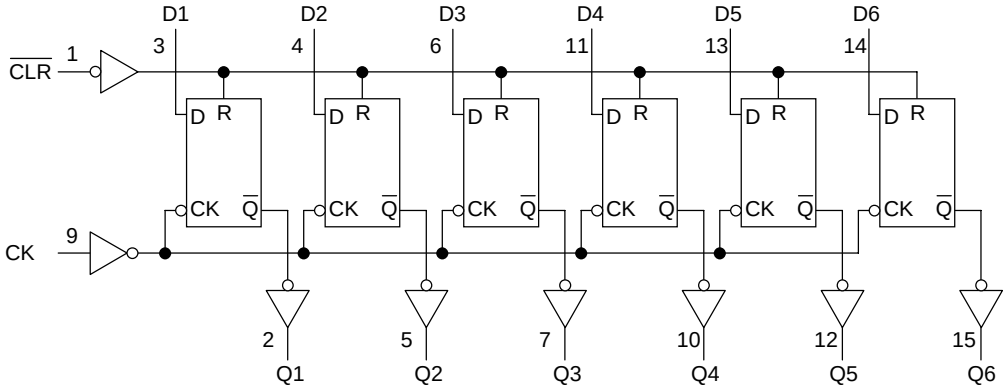


Truth Table

Inputs			Outputs	Function
$\overline{CLR}$	D	CK	Q	
L	X	X	L	Clear
H	L	↑	L	—
H	H	↑	H	—
H	X	↓	Qn	No change

X: Don't care

System Diagram



Maximum Ratings

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7.0	V
DC input voltage	V_{IN}	−0.5 to 7.0	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	−20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±50	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	−65 to 150	°C

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 3.6	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 100	ns/V

Electrical Characteristics

DC Characteristics

Characteristics		Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
				V_{CC} (V)	Min	Typ.	Max	Min	Max	
Input voltage	H-level	V_{IH}	—	2.0	1.5	—	—	1.5	—	V
				3.0	2.0	—	—	2.0	—	
				3.6	2.4	—	—	2.4	—	
	L-level	V_{IL}	—	2.0	—	—	0.5	—	0.5	
				3.0	—	—	0.8	—	0.8	
				3.6	—	—	0.8	—	0.8	
Output voltage	H-level	V_{OH}	V_{IN} = V_{IH} or V_{IL} / I_{OH} = −50 μA	2.0	1.9	2.0	—	1.9	—	V
			I_{OH} = −50 μA	3.0	2.9	3.0	—	2.9	—	
			I_{OH} = −4 mA	3.0	2.58	—	—	2.48	—	
	L-level	V_{OL}	V_{IN} = V_{IH} or V_{IL} / I_{OL} = 50 μA	2.0	—	0.0	0.1	—	0.1	
			I_{OL} = 50 μA	3.0	—	0.0	0.1	—	0.1	
			I_{OL} = 4 mA	3.0	—	—	0.36	—	0.44	
Input leakage current		I_{IN}	V_{IN} = 5.5 V or GND	3.6	—	—	±0.1	—	±1.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND	3.6	—	—	4.0	—	40.0	μA

Timing Requirements (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C	Ta = −40 to 85°C	Unit
			V_{CC} (V)	Limit	Limit	
Minimum pulse width (CK)	$t_{W(L)}$ / $t_{W(H)}$	—	2.7	6.5	7.5	ns
			3.3 ± 0.3	5.0	5.0	
Minimum pulse width ($\overline{CLR}$)	$t_{W(L)}$	—	2.7	6.5	7.5	ns
			3.3 ± 0.3	5.0	5.0	
Minimum set-up time	t_s	—	2.7	7.5	8.5	ns
			3.3 ± 0.3	5.0	6.0	
Minimum hold time	t_h	—	2.7	0	0	ns
			3.3 ± 0.3	0	0	
Minimum removal time ($\overline{CLR}$)	t_{rem}	—	2.7	4.5	4.5	ns
			3.3 ± 0.3	3.0	3.0	

AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q)	t_{pLH} / t_{pHL}	—	2.7	15	—	7.6	14.5	1.0	17.5	ns
				50	—	10.1	18.0	1.0	21.0	
			3.3 ± 0.3	15	—	5.9	9.3	1.0	11.0	
				50	—	8.4	12.8	1.0	14.5	
Propagation delay time ($\overline{CLR}$ -Q)	t_{pHL}	—	2.7	15	—	7.9	15.0	1.0	18.5	ns
				50	—	10.4	18.5	1.0	22.0	
			3.3 ± 0.3	15	—	6.2	9.7	1.0	11.5	
				50	—	8.7	13.2	1.0	15.0	
Maximum clock frequency	f_{max}	—	2.7	15	65	130	—	55	—	MHz
				50	45	60	—	40	—	
			3.3 ± 0.3	15	115	180	—	95	—	
				50	65	95	—	55	—	
Output to output skew	t_{osLH} / t_{osHL}	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
			3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input capacitance	C_{IN}			(Note 2)	—	4	10	—	10	pF
Power dissipation capacitance	C_{PD}			(Note 3)	—	29	—	—	—	pF

Note 1: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

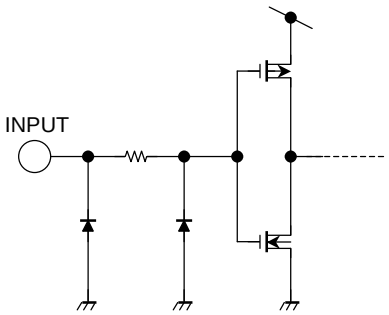
Note 2: Parameter guaranteed by design.

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.
Average operating current can be obtained by the equation:
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per F/F)
And the total C_{PD} when n pcs. of F/F operate can be gained by the following equation:
C_{PD} (total) = 19 + 10·n

Noise Characteristics (Ta = 25°C, input: $t_r = t_f = 3$ ns, $C_L = 50$ pF)

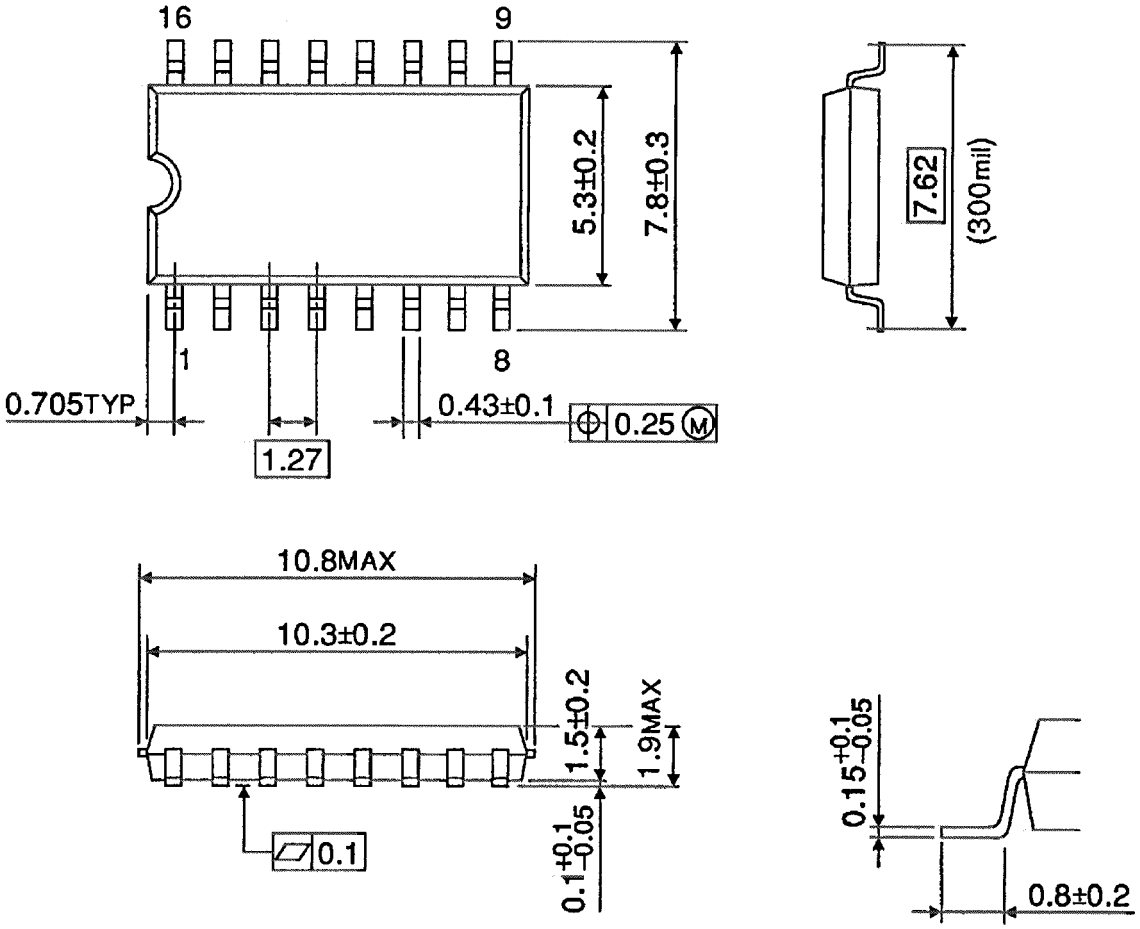
Characteristics		Symbol	Test Condition	Typ.	Limit	Unit
			V_{CC} (V)			
Quiet output maximum dynamic	V_{OL}	V_{OLP}	—	3.3	0.3	0.5	V
Quiet output minimum dynamic	V_{OL}	V_{OLV}	—	3.3	−0.3	−0.5	V
Minimum high level dynamic input voltage	V_{IH}	V_{IHD}	—	3.3	—	2.0	V
Maximum low level dynamic input voltage	V_{IL}	V_{ILD}	—	3.3	—	0.8	V

Input Equivalent Circuit



Package Dimensions

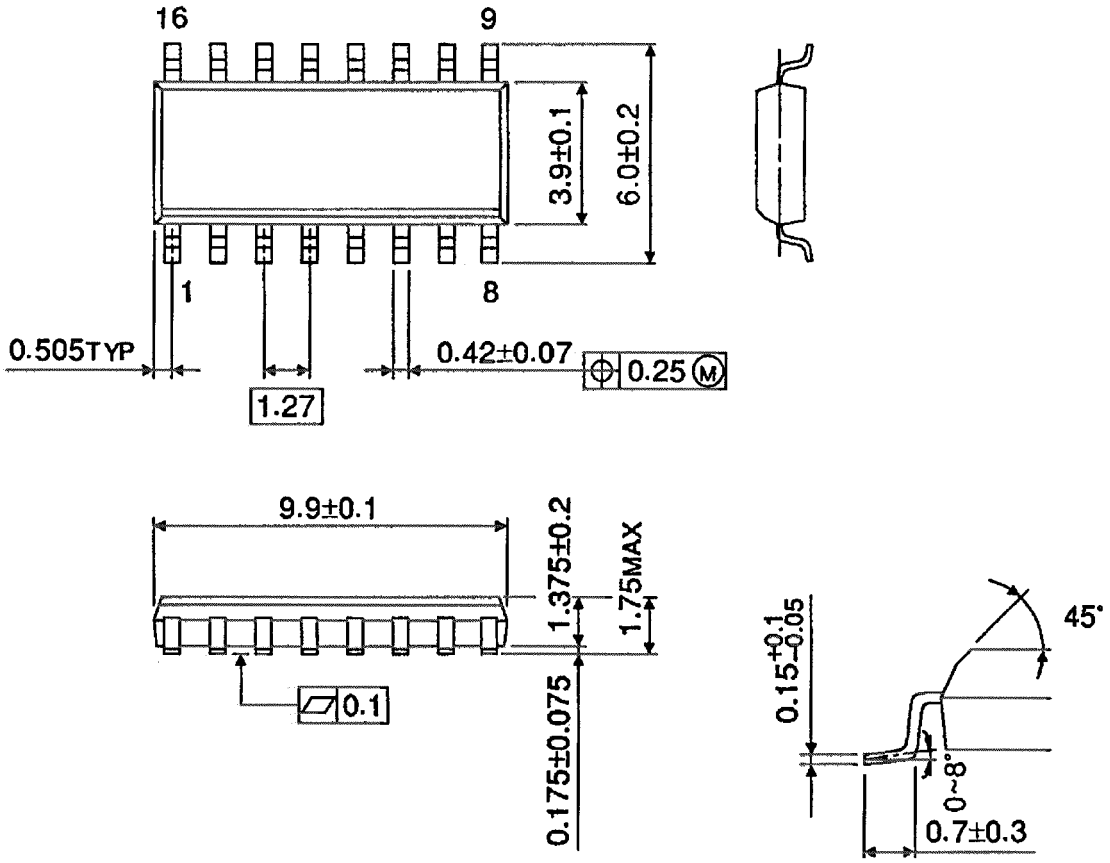
SOP16-P-300-1.27 Unit : mm



Weight: 0.18 g (typ.)

Package Dimensions

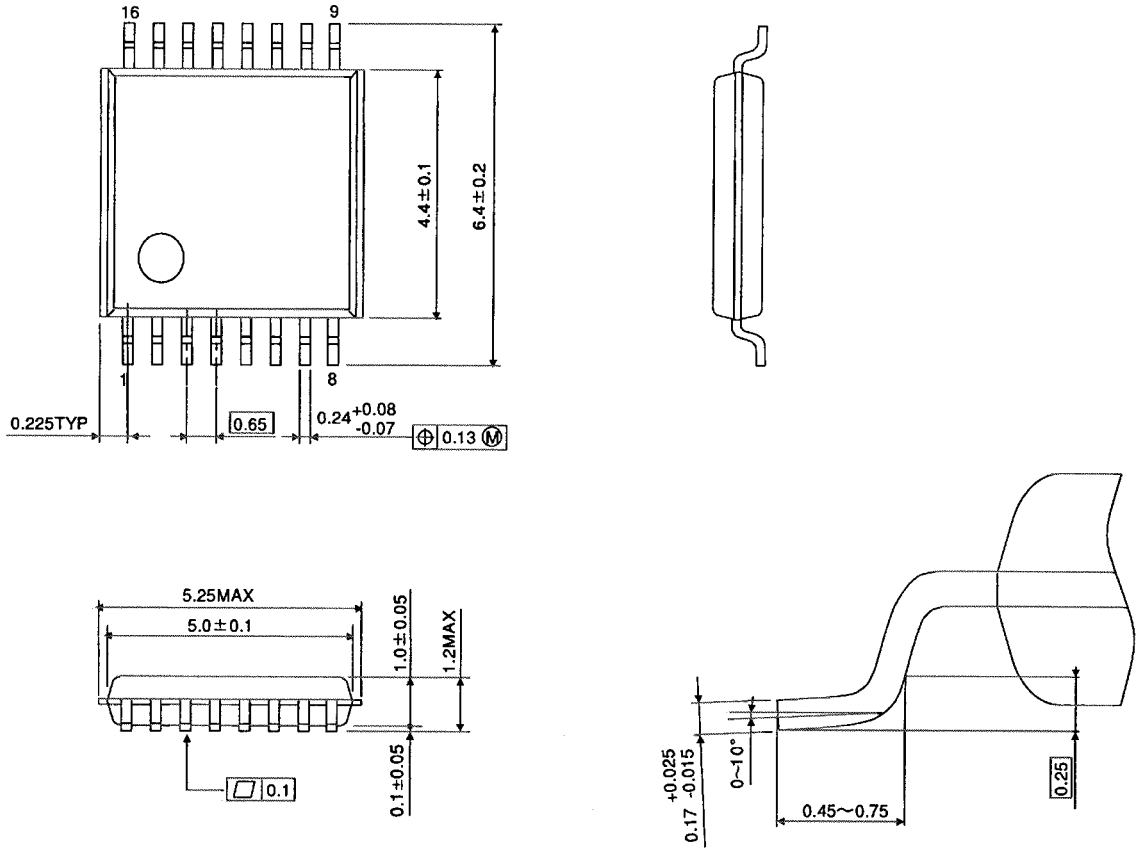
SOL16-P-150-1.27 Unit : mm



Weight: 0.12 g (typ.)

Package Dimensions

TSSOP16-P-0044-0.65 Unit : mm



Weight: 0.06 g (typ.)

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