

TC74VHC164F, TC74VHC164FN, TC74VHC164FT

8 - BIT SHIFT REGISTER (S - IN, P - OUT)

The TC74VHC164 is an advanced high speed CMOS 8 - BIT SERIAL - IN PARALLEL - OUT SHIFT REGISTER fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. It consists of a serial - in, parallel - out 8 - bit shift register with a CLOCK input and an overriding CLEAR input. Two serial data inputs (A, B) are provided so that one may be used as a data enable.

An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES :

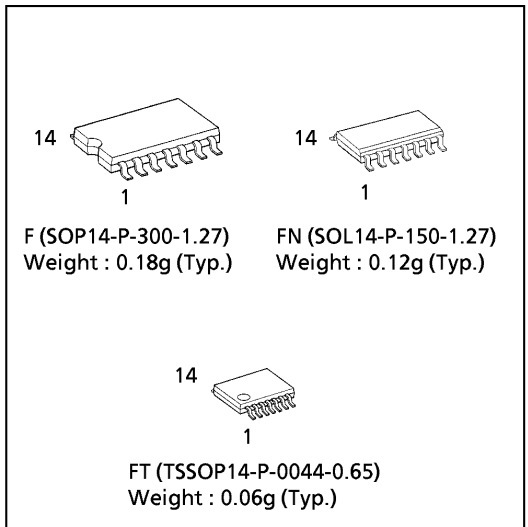
- High Speed..... $f_{MAX} = 175\text{MHz}(\text{typ.})$
at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (\text{Min.})$
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range.... $V_{CC} (\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Low Noise $V_{OLP} = 0.8\text{V} (\text{Max.})$
- Pin and Function Compatible with 74ALS164

TRUTH TABLE

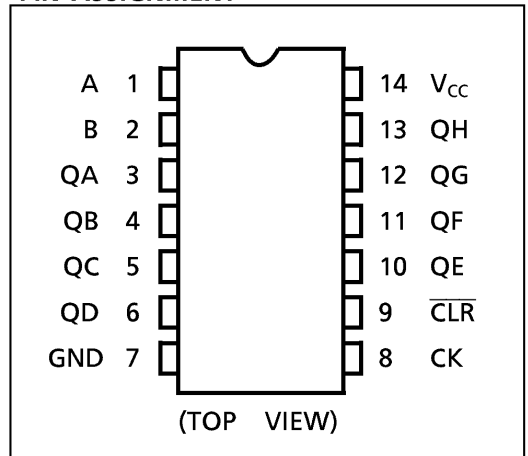
INPUTS				OUTPUTS			
CLR	CK	SERIAL IN		QA	QB	...	QH
		A	B				
L	X	X	X	L	L	...	L
H		X	X	NO CHANGE			
H		L	X	L	QA _n	...	QG _n
H		X	L	L	QA _n	...	QG _n
H		H	H	H	QA _n	...	QG _n

X : Don't Care
 QA_n ~ QG_n: The level of QA ~ QG, respectively, before the most recent positive edge of the clock.

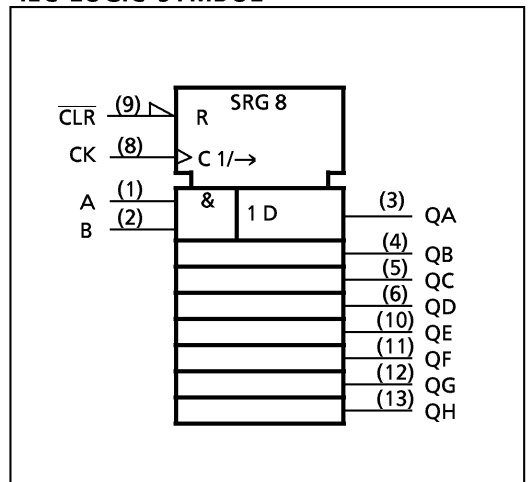
(Note) The JEDEC SOP (FN) is not available in Japan.



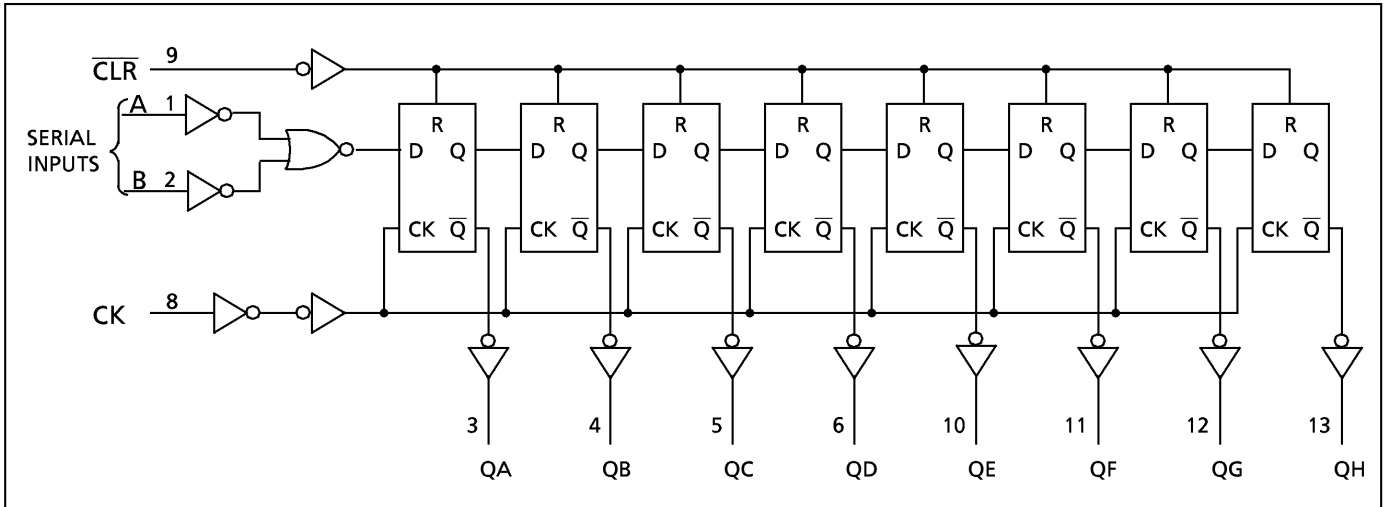
PIN ASSIGNMENT



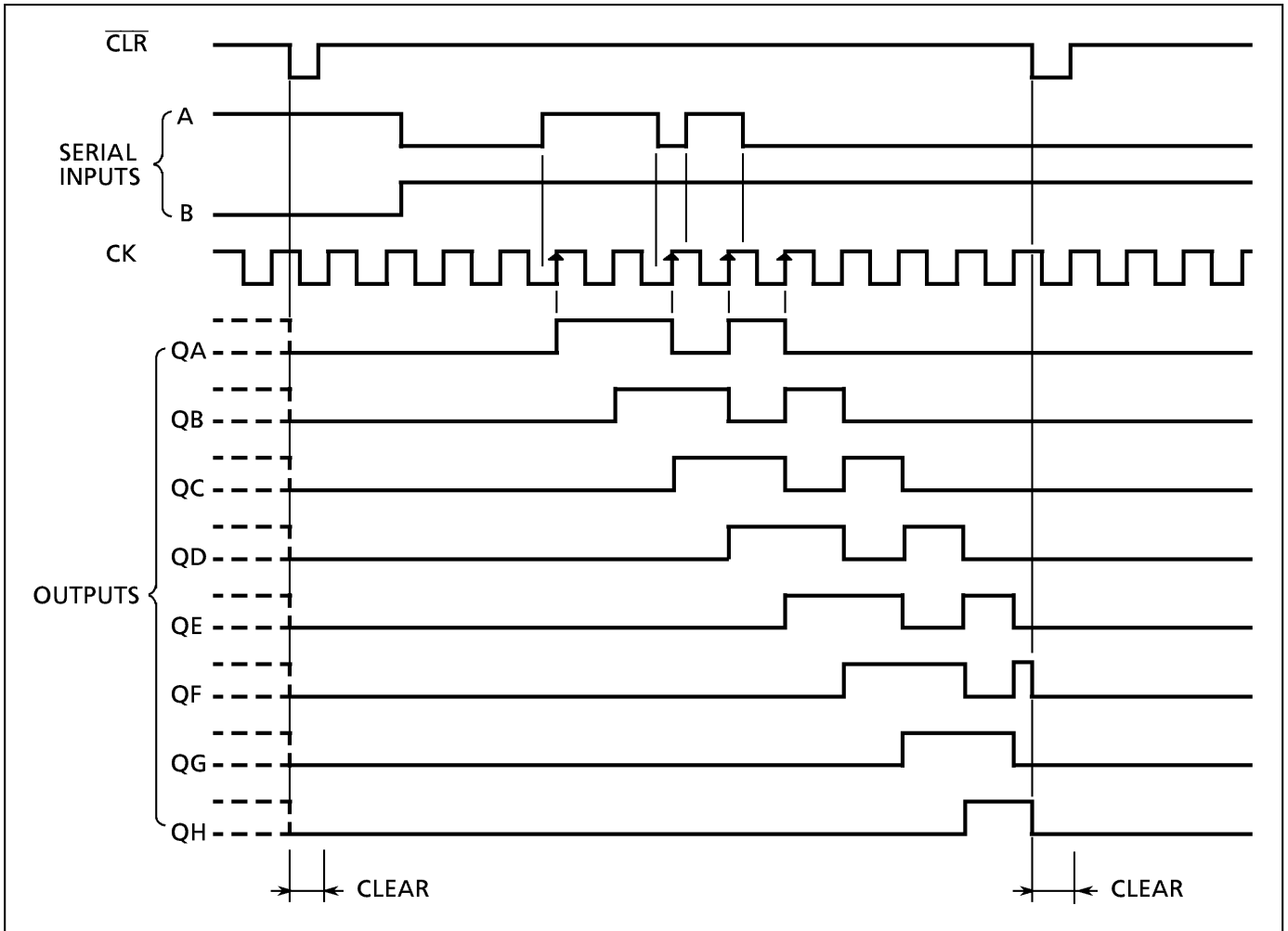
IEC LOGIC SYMBOL



SYSTEM DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V _{CC}	-0.5~7.0	V
DC Input Voltage	V _{IN}	-0.5~7.0	V
DC Output Voltage	V _{OUT}	-0.5~V _{CC} +0.5	V
Input Diode Current	I _{IK}	-20	mA
Output Diode Current	I _{OK}	±20	mA
DC Output Current	I _{OUT}	±25	mA
DC V _{CC} /Ground Current	I _{CC}	±75	mA
Power Dissipation	P _D	180	mW
Storage Temperature	T _{stg}	-65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V _{CC}	2.0~5.5	V
Input Voltage	V _{IN}	0~5.5	V
Output Voltage	V _{OUT}	0~V _{CC}	V
Operating Temperature	T _{opr}	-40~85	°C
Input Rise and Fall Time	dt / dv	0~100 (V _{CC} = 3.3 ± 0.3V) 0~20 (V _{CC} = 5 ± 0.5V)	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V _{IH}		2.0	1.50	—	—	1.50	—	V
			3.0~5.5	V _{CC} × 0.7			V _{CC} × 0.7		
Low - Level Input Voltage	V _{IL}		2.0	—	—	0.50	—	0.50	V
			3.0~5.5	V _{CC} × 0.3			V _{CC} × 0.3		
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	2.0	1.9	2.0	—	1.9	V
				3.0	2.9	3.0	—	2.9	
				4.5	4.4	4.5	—	4.4	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -4mA	3.0	2.58	—	—	2.48	V
			I _{OH} = -8mA	4.5	3.94	—	—	3.80	
			I _{OL} = 50μA	2.0	—	0.0	0.1	—	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}		3.0	—	0.0	0.1	—	V
				4.5	—	0.0	0.1	—	
			I _{OL} = 4mA	3.0	—	—	0.36	—	
		I _{OL} = 8mA	4.5	—	—	0.36	—	0.44	
Input Leakage Current	I _{IN}	V _{IN} = 5.5V or GND	0~5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C	UNIT
			V _{CC} (V)	TYP .	LIMIT	LIMIT	
Minimum Pulse Width (CK)	t _{w(L)}		3.3 ± 0.3	—	5.0	5.0	ns
	t _{w(H)}		5.0 ± 0.5	—	5.0	5.0	
Minimum Pulse Width (CLR)	t _{w(L)}		3.3 ± 0.3 5.0 ± 0.5	— —	5.0 5.0	5.0 5.0	
Minimum Set-up Time	t _s		3.3 ± 0.3	—	5.0	6.0	
			5.0 ± 0.5	—	4.5	4.5	
Minimum Hold Time	t _h		3.3 ± 0.3	—	0.0	0.0	
			5.0 ± 0.5	—	1.0	1.0	
Minimum Removal Time (CLR)	t _{rem}		3.3 ± 0.3	—	2.5	2.5	
			5.0 ± 0.5	—	2.5	2.5	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = -40~85°C		UNIT
		V _{CC} (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK-Q)	t _{pLH} t _{pHL}	3.3 ± 0.3	15	—	8.4	12.8	1.0	15.0	ns
			50	—	10.9	16.3	1.0	18.5	
		5.0 ± 0.5	15	—	5.8	9.0	1.0	10.5	
			50	—	7.3	11.0	1.0	12.5	
Propagation Delay Time (CLR-Q)	t _{pHL}	3.3 ± 0.3	15	—	8.3	12.8	1.0	15.0	
			50	—	10.8	16.3	1.0	18.5	
		5.0 ± 0.5	15	—	5.2	8.6	1.0	10.0	
			50	—	6.7	10.6	1.0	12.0	
Maximum Clock Frequency	f _{MAX}	3.3 ± 0.3	15	80	125	—	65	—	MHz
			50	50	75	—	45	—	
		5.0 ± 0.5	15	125	175	—	105	—	
			50	85	115	—	75	—	
Input Capacitance	C _{IN}			—	4	10	—	10	pF
Power Dissipation Capacitance	C _{PD}	(Note 1)		—	76	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

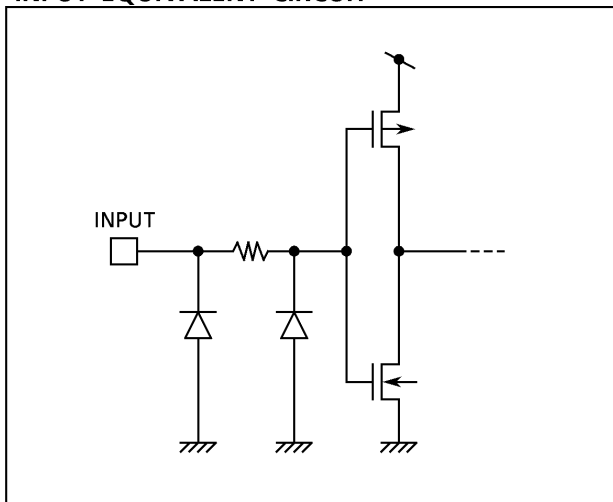
Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$)

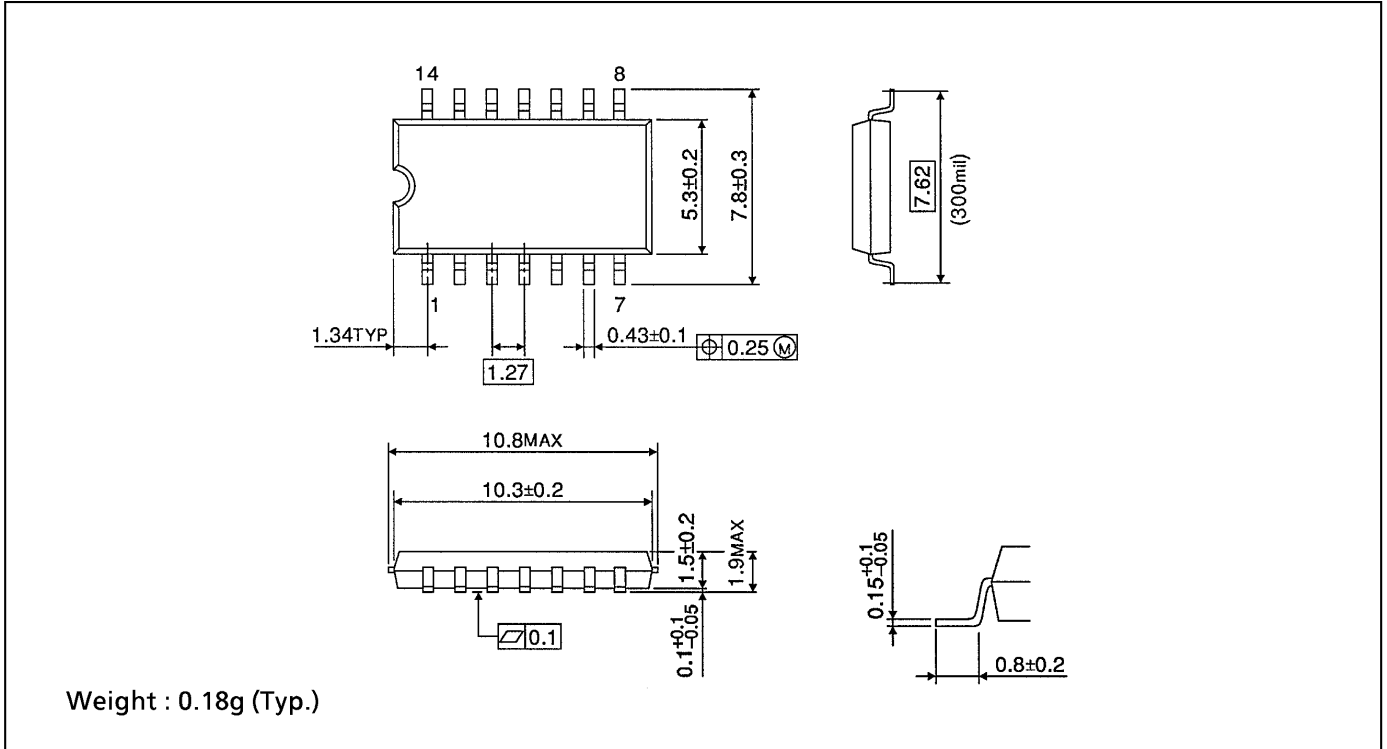
PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT
			V _{CC} (V)	TYP. / MAX.	
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	C _L = 50pF	5.0	0.5 / 0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	C _L = 50pF	5.0	-0.5 / -0.8	V
Minimum High Level Dynamic Input Voltage	V _{IHD}	C _L = 50pF	5.0	- / 3.5	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}	C _L = 50pF	5.0	- / 1.5	V

INPUT EQUIVALENT CIRCUIT



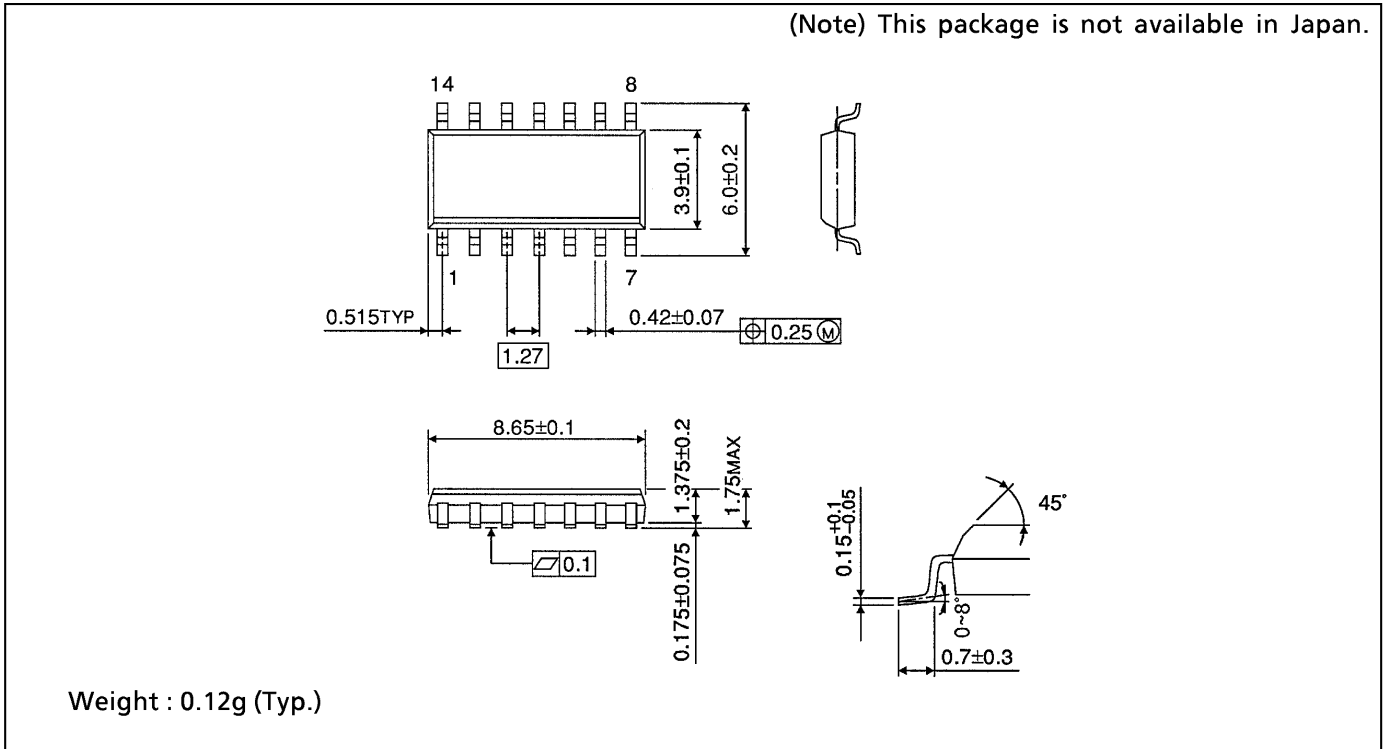
SOP 14PIN (200mil BODY) PACKAGE DIMENSIONS (SOP14-P-300-1.27)

Unit in mm



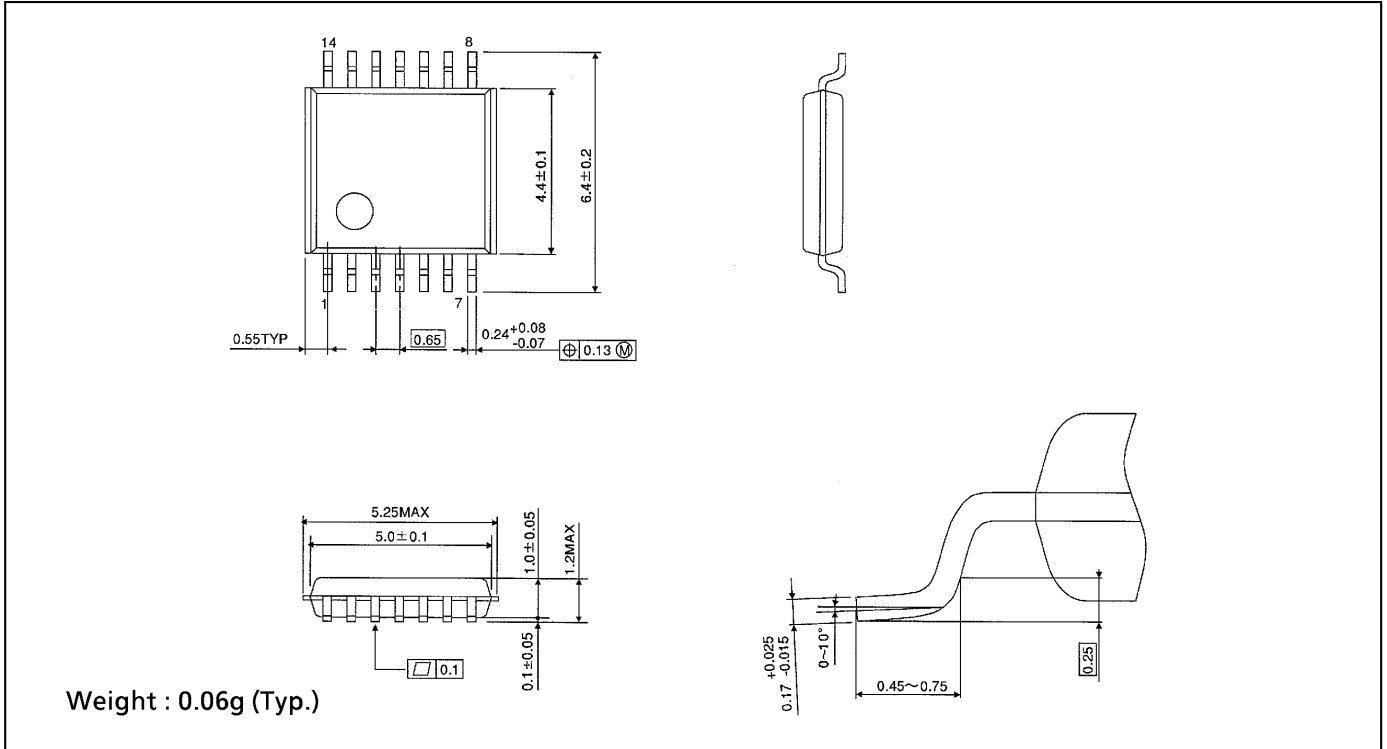
SOP 14PIN (150mil BODY) PACKAGE DIMENSIONS (SOP14-P-150-1.27)

Unit in mm



TSSOP 14PIN PACKAGE DIMENSIONS (TSSOP14-P-0044-0.65)

Unit in mm



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