TelCom Semiconductor, Inc.

TC911A
TC911B

AUTO-ZEROED MONOLITHIC OPERATIONAL AMPLIFIERS

FEATURES

- **First Monolithic Chopper-Stabilized Amplifier With On-Chip Nulling Capacitors**
- **Offset Voltage 5μV**
- **Offset Voltage Drift ..... 0.05μV/°C**
- **Low Supply Current 350μA**
- **High Common-Mode Rejection 116dB**
- **Single Supply Operation ..... 4.5V to 16V**
- **High Slew Rate 2.5V/μsec**
- **Wide Bandwidth 1.5MHz**
- **High Open-Loop Voltage Gain (R_L = 10kΩ) 120dB**
- **Low Input Voltage Noise (0.1Hz to 1Hz) ..... 0.65μV_{P-P}**
- **Pin Compatible With ICL7650**
- **Lower System Parts Count**

ORDERING INFORMATION

Part No.	Package	Temperature Range	Maximum Offset Voltage
TC911ACOA	8-Pin SOIC	0°C to +70°C	15μV
TC911ACPA	8-Pin Plastic DIP	0°C to +70°C	15μV
TC911BCOA	8-Pin SOIC	0°C to +70°C	30μV
TC911BCPA	8-Pin Plastic DIP	0°C to +70°C	30μV

GENERAL DESCRIPTION

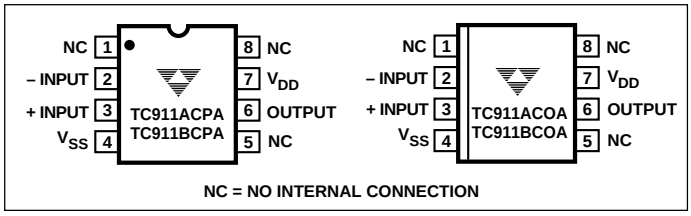
The TC911 CMOS auto-zeroed operational amplifier is the first complete monolithic chopper-stabilized amplifier. Chopper operational amplifiers like the ICL7650/7652 and LTC1052 require user-supplied, external offset compensation storage capacitors. **External capacitors are not required with the TC911.** Just as easy to use as the conventional OP07 type amplifier, the TC911 significantly reduces offset voltage errors. Pinout matches the OP07/741/7650 8-pin mini-DIP configuration.

Several system benefits arise by eliminating the external chopper capacitors: lower system parts count, reduced assembly time and cost, greater system reliability, reduced PC board layout effort and greater board area utilization. Space savings can be significant in multiple-amplifier designs.

Electrical specifications include 15μV maximum offset voltage, 0.15μV/°C maximum offset voltage temperature coefficient. Offset voltage error is five times lower than the premium OP07E bipolar device. The TC911 improves offset drift performance by eight times.

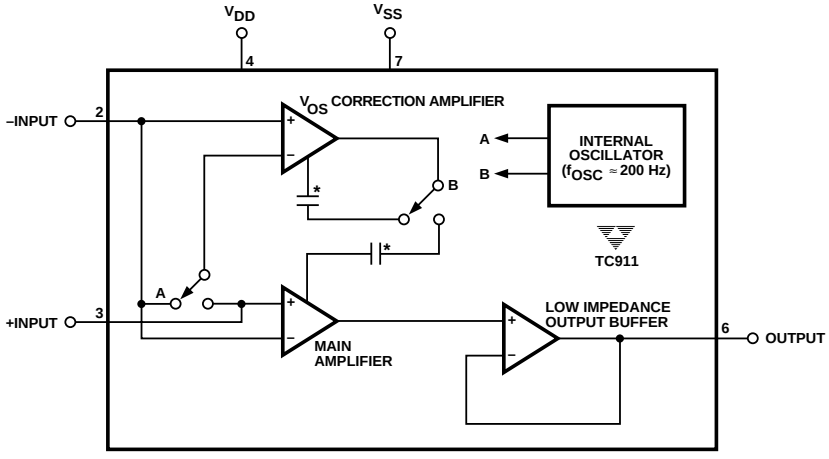
The TC911 operates from dual or single power supplies. Supply current is typically 350μA. Single 4.5V to 16V supply operation is possible, making single 9V battery operation possible. The TC911 is available in 2 package types: 8-pin plastic DIP and SOIC.

PIN CONFIGURATION (SOIC and DIP)



NC = NO INTERNAL CONNECTION

FUNCTIONAL BLOCK DIAGRAM



***NOTE:** Internal capacitors. No external capacitors required.

TC911A
TC911/B

ABSOLUTE MAXIMUM RATINGS*

Total Supply Voltage (V_{DD} to V_{SS}) ..... +18V
Input Voltage ..... (V_{DD} +0.3V) to (V_{SS} –0.3V)
Current into Any Pin 10mA
While Operating 100µA
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Operating Temperature Range
C Device ..... 0°C to +70°C

Package Power Dissipation ($T_A \leq 70°C$)
Plastic DIP 730mW
Plastic SOIC 470mW

*Static-sensitive device. Unused devices should be stored in conductive material. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.

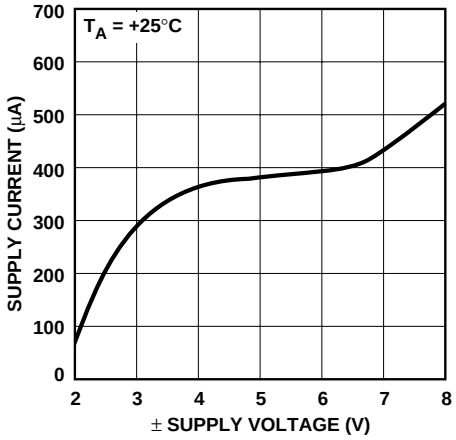
ELECTRICAL CHARACTERISTICS: V_S = ±5V, T_A = +25°C, unless otherwise indicated.

Symbol	Parameter	Test Conditions	TC911A			TC911B			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	T_A = +25°C	—	5	15	—	15	30	µV
TCV_{OS}	Average Temperature Coefficient of Input Offset Voltage (Note 1)	0°C ≤ T_A ≤ +70°C	—	0.05	0.15	—	0.1	0.25	µV/°C
		–25°C ≤ T_A ≤ +85°C	—	0.05	0.15	—	0.1	0.25	µV/°C
I_B	Average Input Bias Current	T_A = +25°C	—	—	70	—	—	120	pA
		0°C ≤ T_A ≤ +70°C	—	—	3	—	—	4	nA
		–25°C ≤ T_A ≤ +85°C	—	—	4	—	—	6	nA
I_{OS}	Average Input Offset Current	T_A = +25°C	—	5	20	—	10	40	pA
		T_A = +85°C	—	—	1	—	—	1	nA
e_N	Input Voltage Noise	0.1 to 1 Hz, $R_S \leq 100\Omega$	—	0.65	—	—	0.65	—	μV_{P-P}
		0.1 to 10 Hz, $R_S \leq 100\Omega$	—	11	—	—	11	—	μV_{P-P}
CMRR	Common-Mode Rejection Ratio	$V_{SS} \leq V_{CM} \leq V_{DD} - 2.2$	110	116	—	105	110	—	dB
CMVR	Common-Mode Voltage Range		V_{SS}	—	$V_{DD} - 2$	V_{SS}	—	$V_{DD} - 2$	V
A_{OL}	Open-Loop Voltage Gain	R_L = 10 kΩ, V_{OUT} = ±4V	115	120	—	110	120	—	dB
V_{OUT}	Output Voltage Swing	R_L = 10 kΩ	V_{SS} + 0.3	—	$V_{DD} - 0.9$	V_{SS} + 0.3	—	$V_{DD} - 0.9$	V
BW	Closed Loop Bandwidth	Closed Loop Gain = +1	—	1.5	—	—	1.5	—	MHz
SR	Slew Rate	R_L = 10 kΩ, C_L = 50pF	—	2.5	—	—	2.5	—	V/µsec
PSRR	Power Supply Rejection Ratio	±3.3V to ±5.5V	112	—	—	105	—	—	dB
V_S	Operating Supply Voltage Range	Split Supply	±3.3	—	±8	±3.3	—	±8	V
		Single Supply	6.5	—	16	6.5	—	16	V
I_S	Quiescent Supply Current	V_S = ±5V	—	350	600	—	—	800	µA

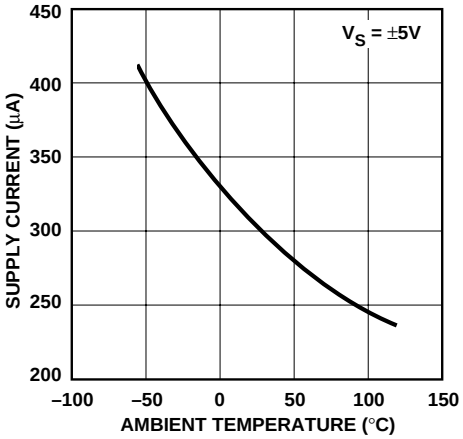
NOTES: 1. Characterized; not 100% tested.

TYPICAL CHARACTERISTICS

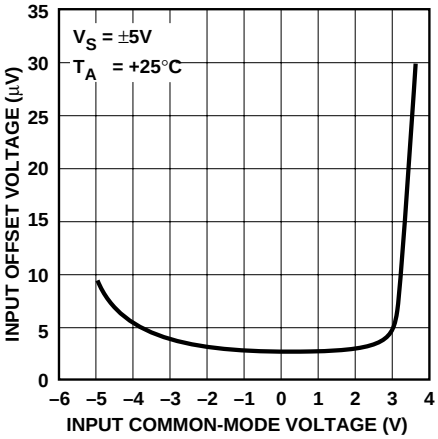
Supply Current vs. ± Supply Voltage



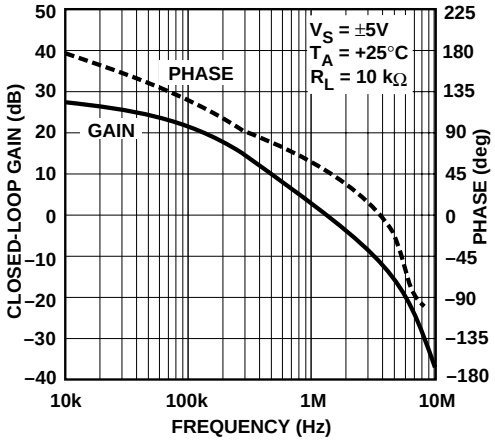
Supply Current vs. Temperature



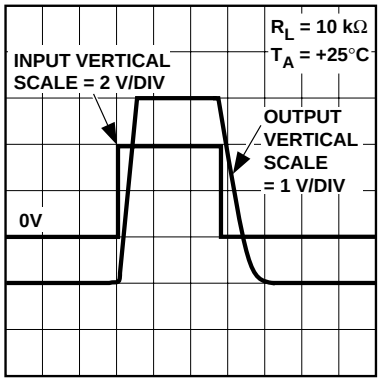
Input Offset Voltage vs. Common-Mode Voltage



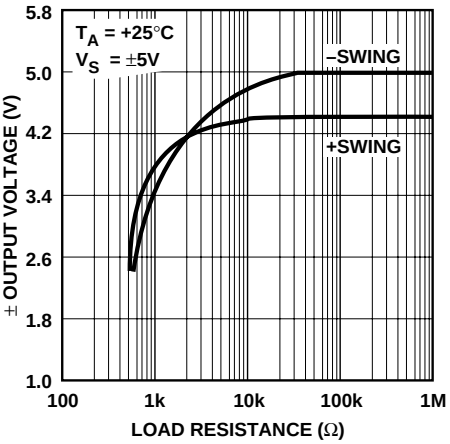
Gain and Phase vs. Frequency



Large Signal Output Switching Waveform



Output Voltage Swing vs. Load Resistance



Pin Compatibility

The CMOS TC911 is pin compatible with the industry standard ICL7650 chopper-stabilized amplifier. The ICL7650 must use external 0.1µF capacitors connected at pins 1 and 8. **With the TC911, external offset voltage error canceling capacitors are not required.** On the TC911 pins 1, 8 and 5 are not connected internally. The ICL7650 uses pin 5 as an optional output clamp connection. External chopper capacitors and clamp connections are not necessary with the TC911. External circuits connected to pins 1, 8 and 5 will have no effect. The TC911 can be quickly evaluated in existing ICL7650 designs. Since external capacitors are not required, system part count, assembly time, and total system cost are reduced. Reliability is increased and PC board layout eased by having the error storage capacitors integrated on the TC911 chip.

The TC911 pinout matches many existing op-amps: 741, LM101, LM108, OP05–OP08, OP-20, OP-21, ICL7650 and ICL7652. In many applications operating from +5V supplies the TC911 offers superior electrical performance and can be a functional pin-compatible replacement. Offset voltage correction potentiometers, compensation capacitors, and chopper-stabilization capacitors can be removed when retrofitting existing equipment designs.

Thermocouple Errors

Heating one joint of a loop made from two different metallic wires causes current flow. This is known as the Seebeck effect. By breaking the loop, an open circuit voltage

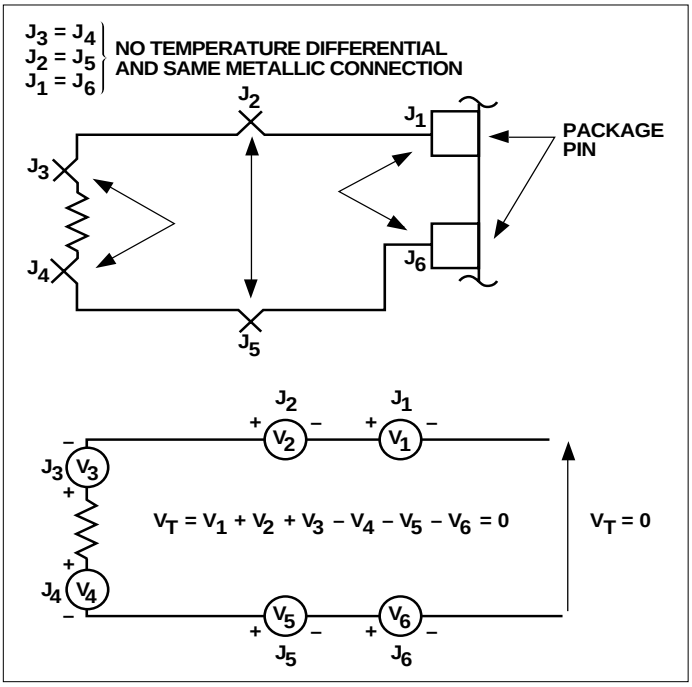


Figure 1. Unwanted Thermocouple Errors Eliminated by Reducing Thermal Gradients and Balancing Junctions

(Seebeck voltage) can be measured. Junction temperature and metal type determine the magnitude. Typical values are 0.1µV/°C to 10µV/°C. Thermal-induced voltages can be many times larger than the TC911 offset voltage drift. Unless unwanted thermocouple potentials can be controlled, system performance will be less than optimum.

Unwanted thermocouple junctions are created when leads are soldered or sockets/connectors are used. Low thermo-electric coefficient solder can reduce errors. A 60% Sn/36% Pb solder has 1/10 the thermal voltage of common 64% Sn/36% Pb solder at a copper junction.

The number and type of dissimilar metallic junctions in the input circuit loop should be balanced. If the junctions are kept at the same temperature, their summation will add to zero-canceling errors (Figure 1).

Shielding precision analog circuits from air currents — especially those caused by power dissipating components and fans — will minimize temperature gradients and thermocouple-induced errors.

Avoiding Latch-Up

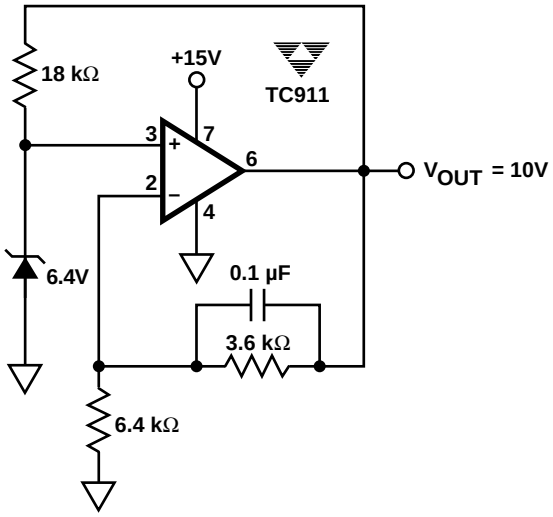
Junction-isolated CMOS circuits inherently contain a parasitic p-n-p-n transistor circuit. Voltages exceeding the supplies by 0.3V should not be applied to the device pins. Larger voltages can turn the p-n-p-n device on, causing excessive device power supply current and excessive power dissipation. TC911 power supplies should be established at the same time or before input signals are applied. If this is not possible input current should be limited to 0.1mA to avoid triggering the p-n-p-n structure.

Overload Recovery

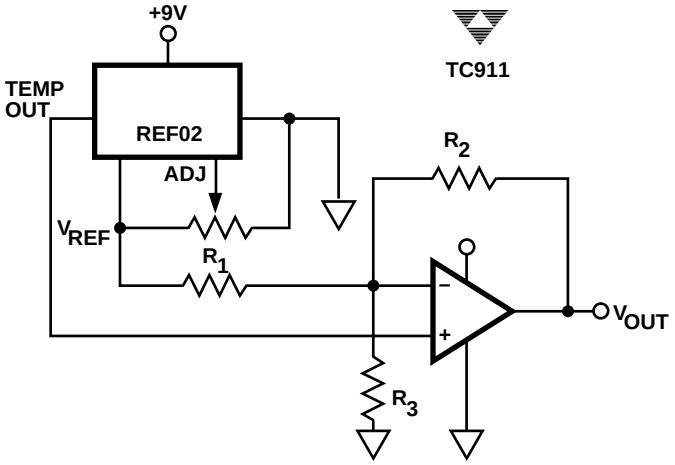
The TC911 recovers quickly from the output saturation. Typical recovery time from positive output saturation is 20msec. Negative output saturation recovery time is typically 5msec.

TYPICAL APPLICATIONS

10-Volt Precision Reference



Thermometer Circuit

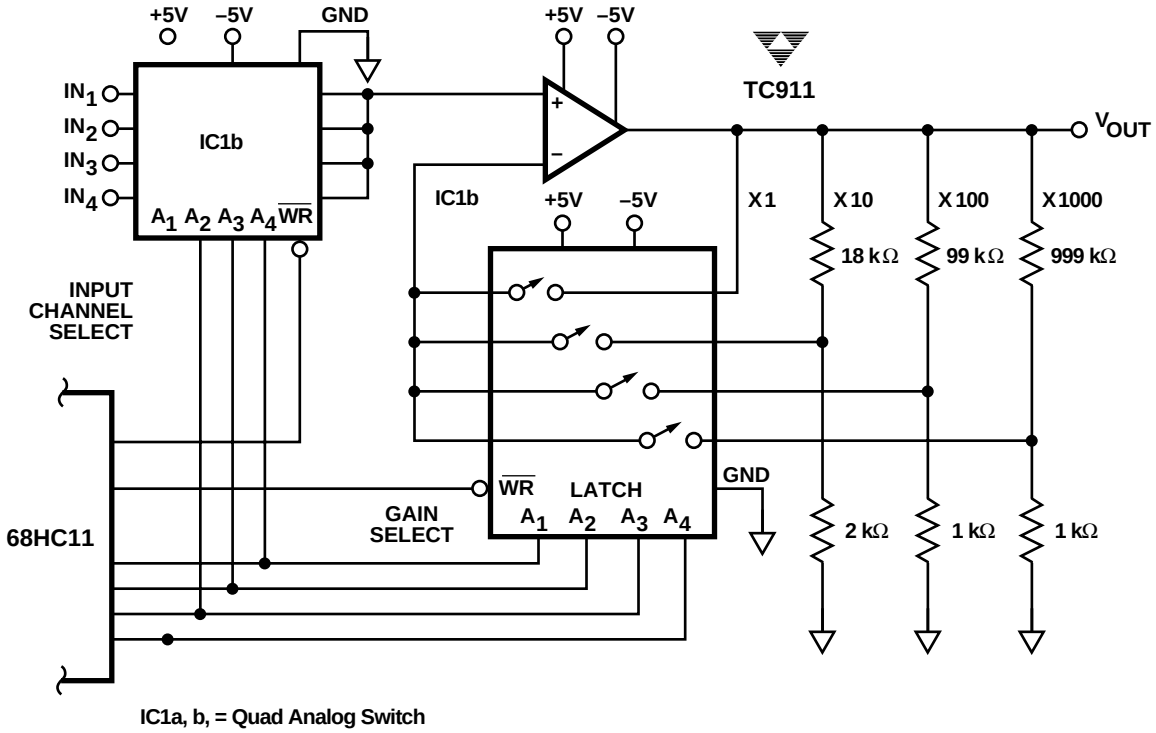


$$V_{OUT} = V_{TEMP}\left[1 + R_2\left(\frac{R_3 + R_1}{R_3 X\ R_1}\right)\right] - \left[V_{REF}\ \frac{R_2}{R_1}\right]$$

$$\frac{d\ V_{OUT}}{dT} = \left[1 + R_2\left(\frac{R_3 + R_1}{R_3 X\ R_1}\right)\right]\frac{d\ (V_{TEMP})}{dT} \approx K\ (2.1\ mV/°C)$$

$$K = 1 + \frac{R_2}{R_3 X\ R_1}$$

Programmable Gain Amplifier With Input Multiplexer

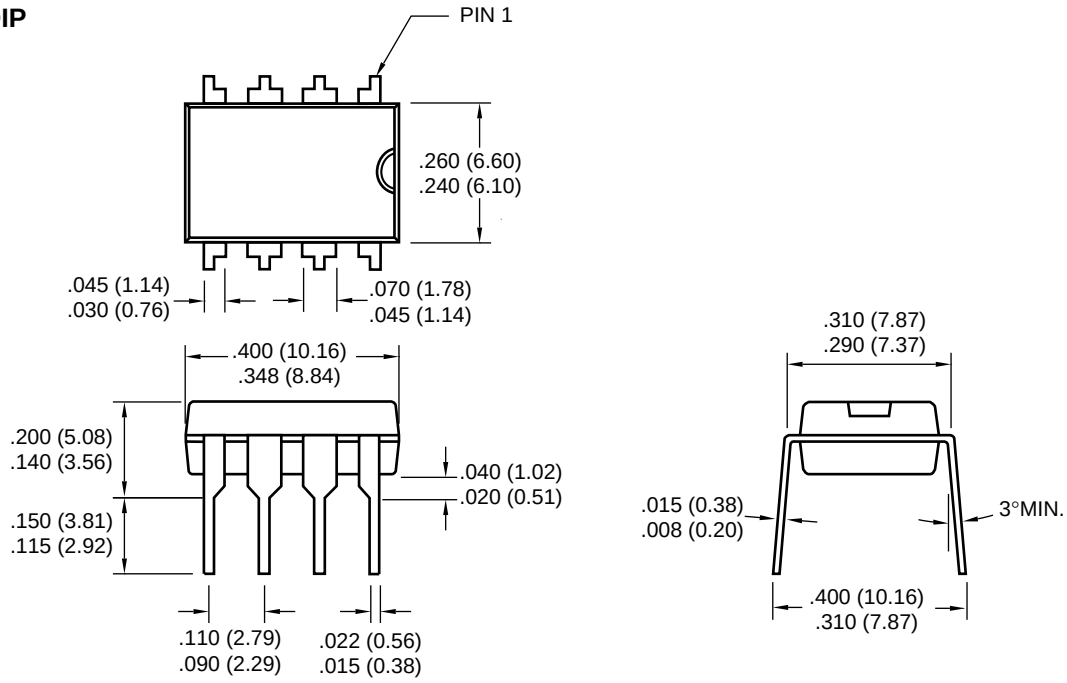


IC1a, b, = Quad Analog Switch

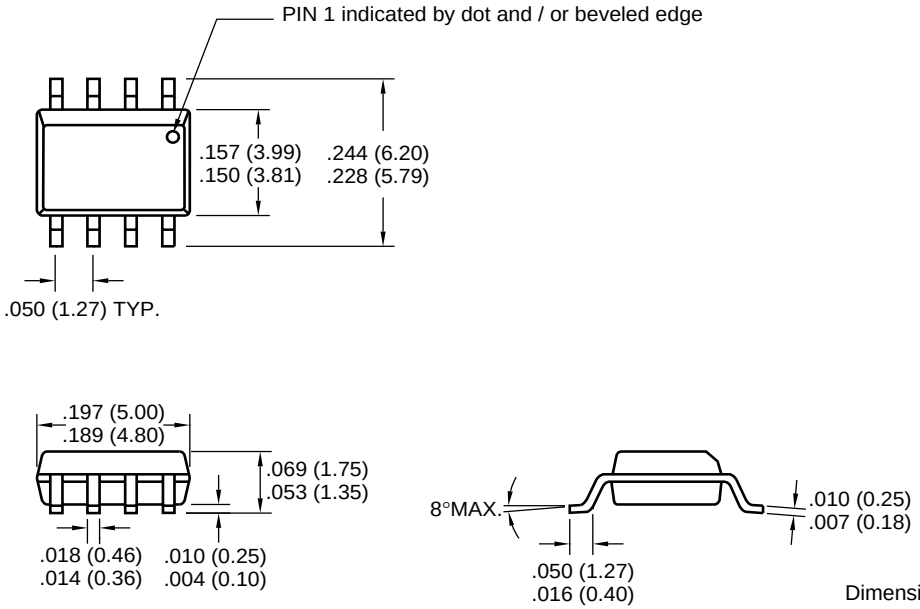
TC911A
TC911/B

PACKAGE DIMENSIONS

8-Pin Plastic DIP



8-Pin SOIC



Dimensions: inches (mm)

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