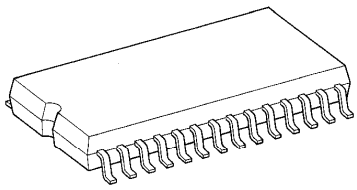
TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9270F, TC9270N

Σ-Δ MODULATION SYSTEM DA CONVERTER WITH A BUILT-IN DIGITAL ATTENUATOR DIGITAL FILTER

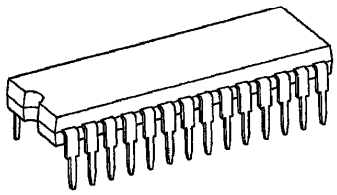
TC9270F, TC9270N are a 2'nd order Σ-Δ modulation system 1-bit DA converter with a built-in 8 times over sampling FIR type digital filter developed for digital audio equipment.
As the de-empahsis filter has been incorporation, it is possible to construct small the digital filter ~ the analog output unit at a low price.

TC9270F



SOP28-P-450-1.27

TC9270N



SDIP28-P-400-1.78

Weight
SOP28-P-450-1.27 : 0.8g (Typ.)
SDIP28-P-400-1.78 : 2.2g (Typ.)

FEATURES

- Built-in 8 times over-sampling FIR type digital filter.
- Over sampling ratio (OSR) of Σ-Δ modulation circuit is 384fs or 256fs.
- Built-in digital de-emphasis filter.
- Permits microcontrollers to attenuate output levels (128 steps) during serial mode.
- Simultaneous outputs L-ch and R-ch.
- Compatible with double speed operation.
- Built-in Digital 0 Detection.
- Pin of OSCE can be stopped system clock.
- Characteristics of the digital filter and DA converter are as follows.

DIGITAL FILTER

	DIGITAL FILTER	PASS-BAND RIPPLE	TRANSIENT BAND WIDTH	STOP-BAND SUPPRESSION
Standard Operation	8fs	±0.003dB	20k~24.1kHz	−68dB
Double Speed Operation	4fs	±0.05dB	20k~24.1kHz	−40dB

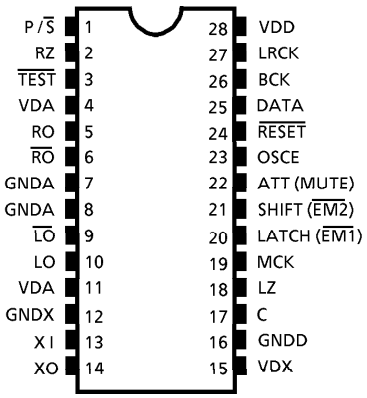
DA CONVERTER

	OSR	NOISE DISTORATION	S/N RATIO
Standard Operation	384fs	−90dB (TYP)	100dB (TYP)
Double Speed Operation	192fs	−87dB (TYP)	98dB (TYP)

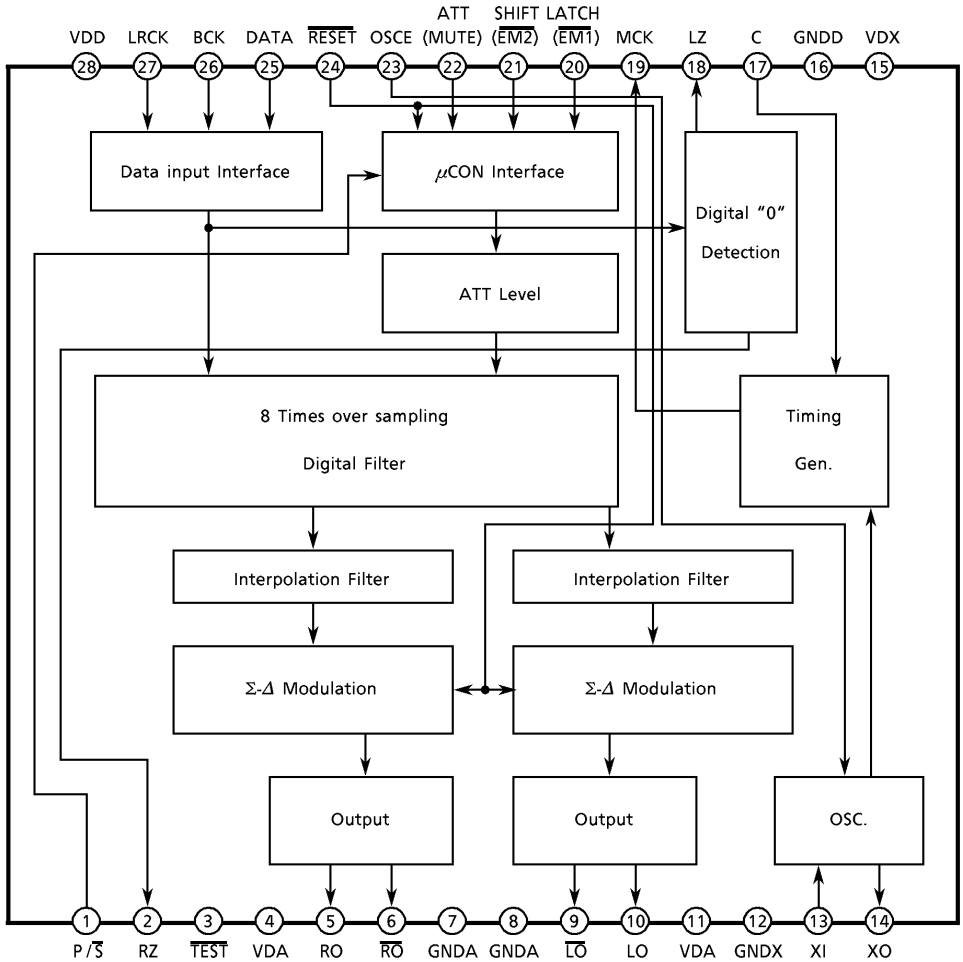
- 2 kinds of package, Pin 28 flat package and Pin 28 DIP shrunk package.

980910EBA1

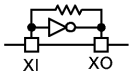
PIN CONNECION



BLOCK DIAGRAM



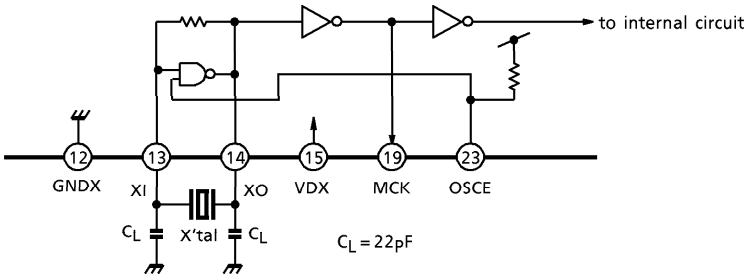
DESCRIPTION OF PIN FUNCTIONS

No.	SYMBOL	I / O	FUNCTION & OPERATION	REMARKS
1	P / $\overline{S}$	I	Parallel control, serial control, switching pin.	Pull-up resistance
2	RZ	O	R-ch digital "0" detection output pin.	
3	$\overline{TEST}$	I	Test pin. Normally, use at "H".	Pull-up resistance
4	VDA	—	Analog power supply pin.	
5	RO	O	R-ch data forward output pin.	
6	$\overline{RO}$	O	R-ch data reverse output pin.	
7	GNDA	—	Analog ground pin.	
8	GNDA	—	Analog ground pin.	
9	$\overline{LO}$	O	L-ch data reverse output pin.	
10	LO	O	L-ch data forward output pin.	
11	VDA	—	Analog power supply pin.	
12	GNDX	—	Crystal oscillator ground Pin.	
13	XI	I	Crystal oscillator connection pin. Connect to a crystal oscillator, generates needed frequency for the system.	
14	XO	O		
15	VDX	—	Crystal oscillator power supply pin.	
16	GNDD	—	Digtal ground pin.	
17	C	I	Clock Select pin. "L" ; 256fs, "H" ; 384fs.	Pull-up resistance
18	LZ	O	L-ch digital "0" detection output pin.	
19	MCK	O	System clock output pin.	
20	LATCH ($\overline{EM1}$)	I	Serial mode : Data latch signal input pin. Parallel mode : De-emphasis filter mode select pin.	Pull-up resistance
21	SHIFT ($\overline{EM2}$)	I	Serial mode : Shift clock input pin. Parallel mode : De-emphasis filter mode select pin.	Pull-up resistance
22	ATT (MUTE)	I	Serial mode : Data input pin. Parallel mode : Soft mute cantrol pin. ("H" Soft mute ON)	Pull-up resistance
23	OSCE	I	System clock control pin. "L" : System clock stop	Pull-up resistance
24	$\overline{RESET}$	I	Reset pin. "L" : Reset Σ-Δ circuit and ATT data 00 (HEX)	Pull-up resistance
25	DATA	I	Audio data input pin.	
26	BCK	I	Bit clock input pin.	
27	LRCK	I	LR clock input pin.	
28	VDD	—	Digital power supply pin.	

OPERATION DESCRIPTION FOR EACH BLOCK

1. CRYSTAL OSCILLATION CIRCUIT AND TIMING GENERATOR

Clock required for internal operation can be generated when crystal and capacitors are connected as shown in FIG.1 So external system clock signal may be applied to the X1 terminal at Pin 13. However are must be taken in using system clock since the S/N ratio and noise distortion performance can be greatly affected by Jitter, rise and fall characteristics··· etc. of system clock.



Use crystal with Low CI value and quick response.

FIG.1 Configuration of crystal oscillation circuit

The timing generator generates the timing signal for digital filter, digital attennator, de-emphasis filter Σ-Δ demodulator circuit.

C (Pin 17)	XI INPUT CLOCK
L	256fs
H	384fs

Internal system clock can be stopped by OSCE pin but output of DAC will become unstable.

OSCE (Pin 23)	SYSTEM CLOCK
L	Stop
H	Normal operation

2. DATA INPUT CIRCUIT

Data and LRCK are taken into the shift register at the leading edge of BCK.
As shown in the following timing example, it is necessary to input data and LRCK synchronized with the falling edge of BCK.
In parallel mode ($P/\overline{S}$ = "H"), input data length is fixed to 16 bits.
In serial mode ($P/\overline{S}$ = "L"), input data length can be selected to 16, 18, or 20bits.

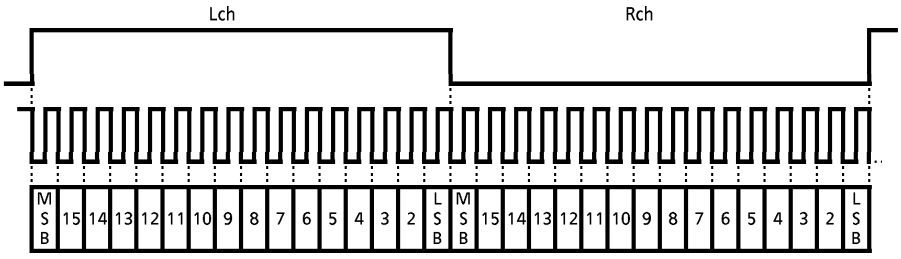


FIG.2a Example of input timing diagram (16 bit Input)

If BCK is 48fs or 64fs, please input DATA as follows.

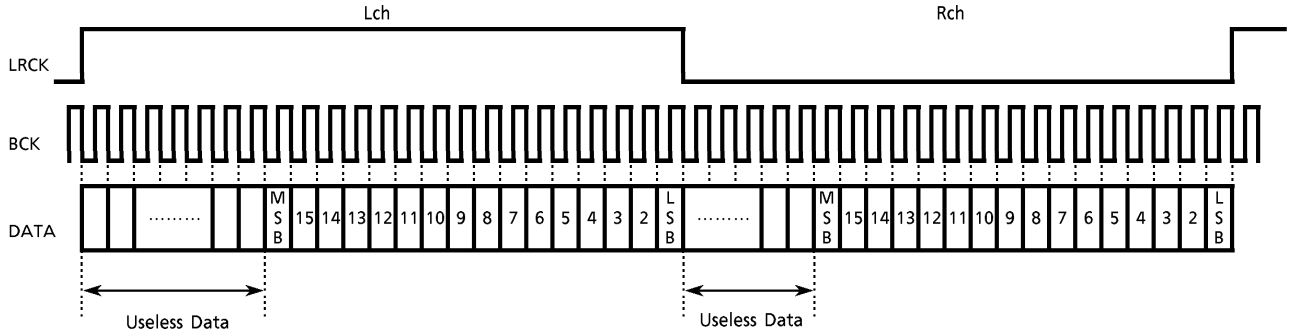


FIG.2b Example of input timing diagram (16 bit input)
When BCK = 48fs or 64fs.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	VDD	−0.3~6.0	V
	VDA	−0.3~6.0	V
	VDX	−0.3~6.0	V
Input Voltage	Vin	−0.3~VDD+0.3	V
Power Dissipation	PD	TC9270F : 600	mW
		TC9270N : 800	
Operating Temperature	T_{opr}	−35~85	°C
Storage Temperature	T_{stg}	−55~150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = −35~85°C VDD = VDX = VDA = 5V)

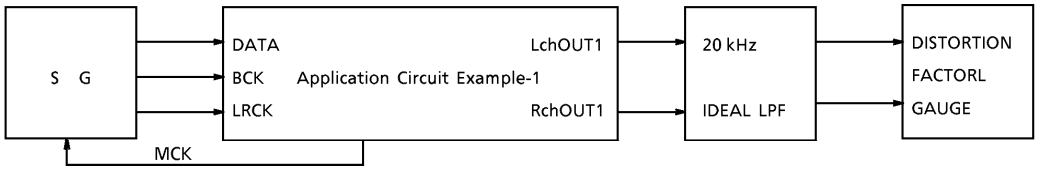
DC CHARACTERISTICS

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Power Supply Voltage		VDD	—	Ta = −35~85°C	4.5	5.0	5.5	V
		VDX			4.5	5.0	5.5	
		VDA			4.5	5.0	5.5	
Power Dissipation		IDD	—	XI = 16.9MHz	—	30	40	mA
Input Voltage	"H"Level	VIH	—		VDD×0.7	—	VDD	V
	"L"Level	VIL			0.0	—	VDD×0.3	
Input Current	"H"Level	IIH	—		−1.0	—	1.0	μA
	"L"Level	IIL						
Pull-up Resiso		RUP	—	1, 3, 17, 20, 21, 22, 23, Pin 24 Ta = 25°C, at 0V force measure current.	100	150	300	kΩ

AC CHARACTERISTICS (*) : Ta = 25°C

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Noise Distortion	(*)	THD+N	1	1kHz Sine wave, full-scale input	—	−90	−85	dB
S/N Ratio	(*)	S/N	1		95	100	—	dB
Dynamic Range	(*)	DR	1	1kHz Sine wave, −60 Input Conversion	90	95	—	dB
Cross-talk	(*)	CT	1	1kHz Sine wave, full-scale input	—	−95	−90	dB
Operating Frequency		f_{opr}	—		10	16.9344	19.2	MHz
Input Frequency		f_{LR}	—	LRCK duty cycle = 50%	30	44.1	100	kHz
		f_{BCK}		BCK duty cycle = 50%	0.96	1.4112	6.2	MHz
Rise Time		t_r	—	LRCK, BCK (10%~90%)	—	—	15	nS
Fall Time		t_f			—	—	15	nS
Delay Time		t_d	—	BCK Edge → LRCK, DATA	−50	—	50	nS

- **TEST CIRCUIT – 1** ; Application Circuit Example 1 is used.

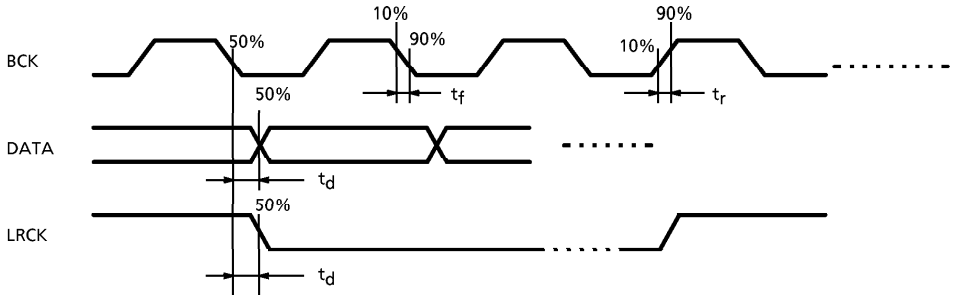


SG : ANRITSU MG-22A or equivalent
LPF : SHIBASOKU 725C Biult-In Filter
Distortion Factor Gauge : SHIBASOKU 725C or equivalent

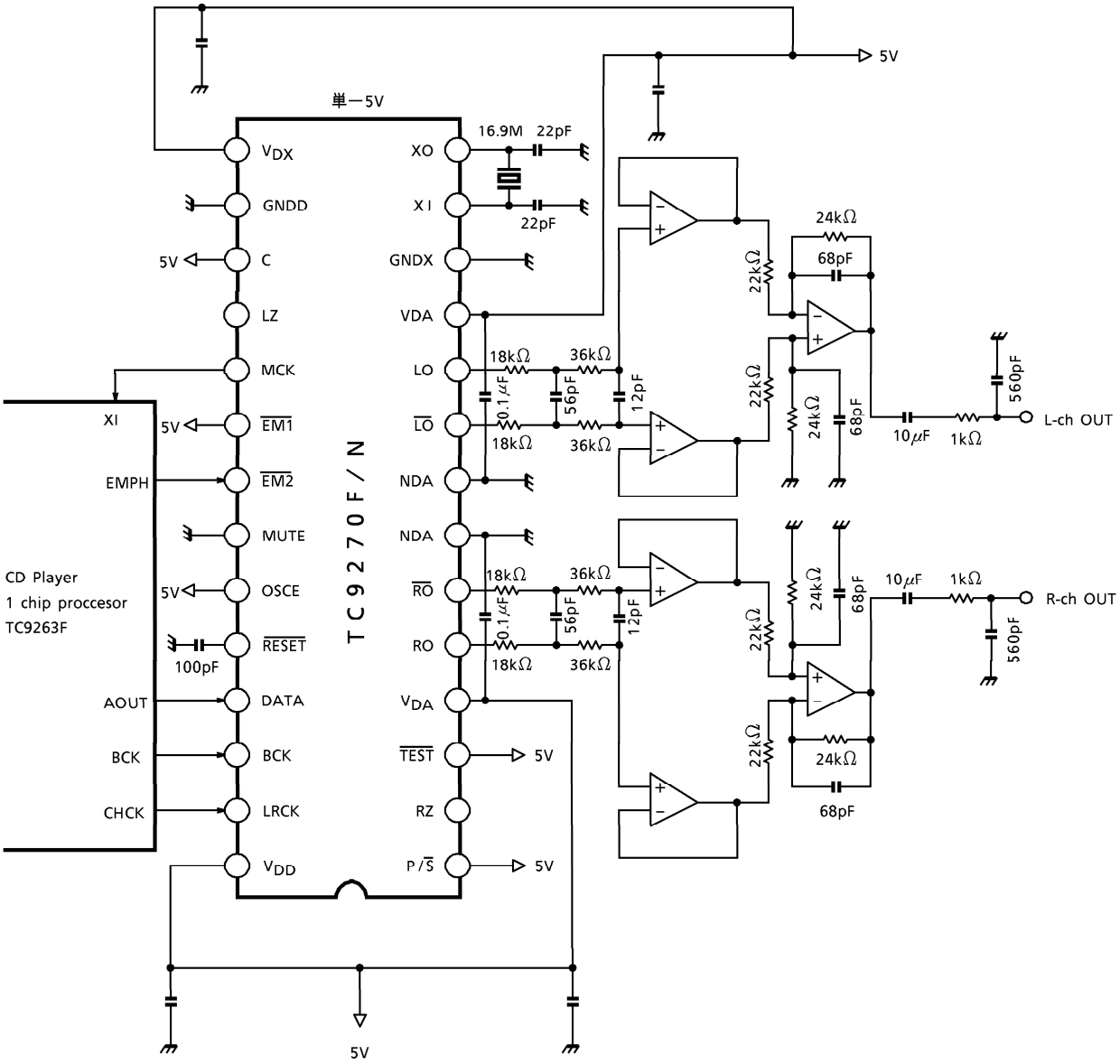
Measuring Item	Distortion factor gauge filter setting A weight
THD + N, CT	OFF
S / N, DR	ON

A weight : IEC - A or equivalent

- **AC CHARACTERISTIC POINT** ; (Input signal ; LRCK、BCK、DATA)

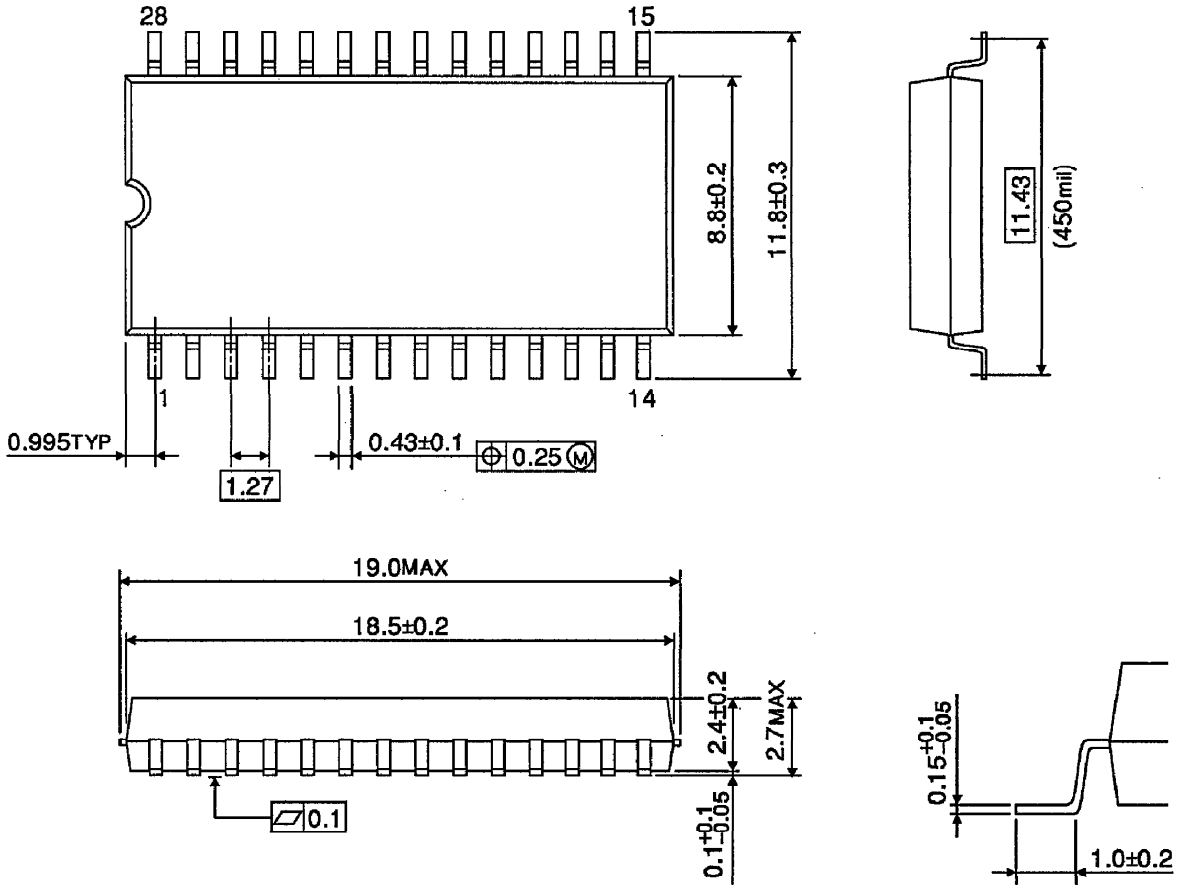


APPLICATION CIRCUIT



PACKAGE DIMENSIONS

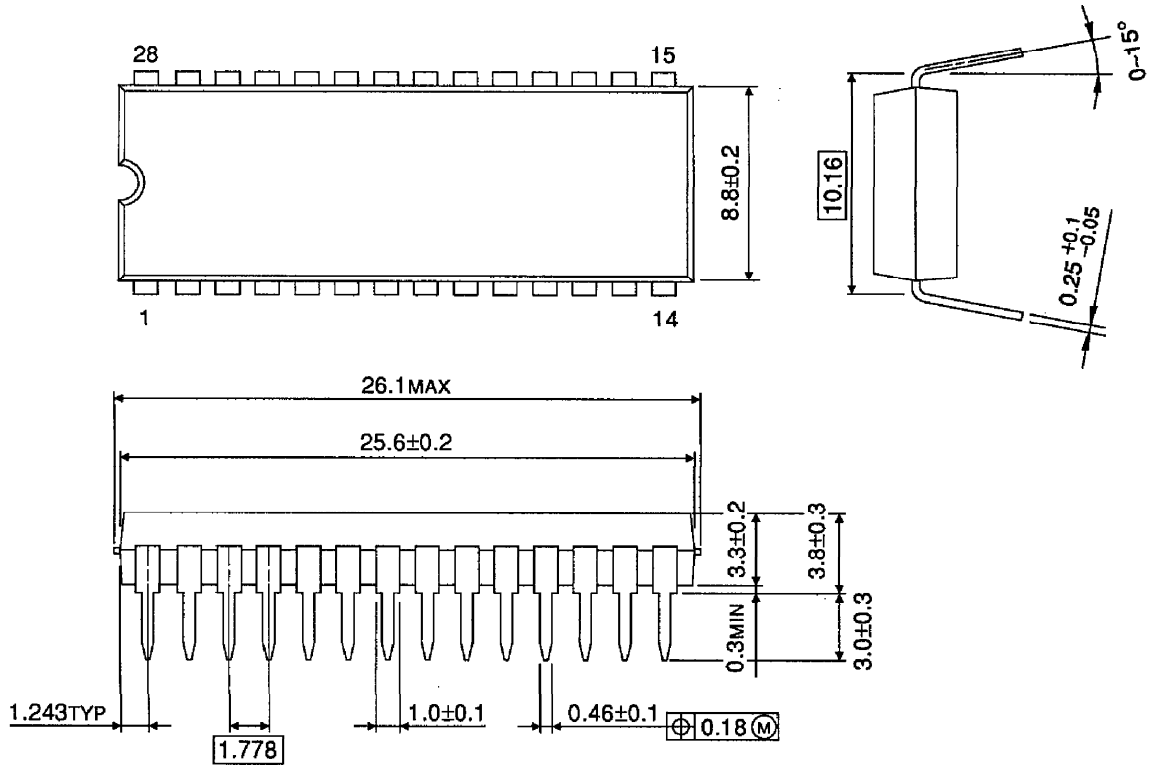
SOP28-P-450-1.27 Unit : mm



Weight : 0.8g (Typ.)

PACKAGE DIMENSIONS

SDIP28-P-400-1.78 Unit : mm



Weight : 2.2g (Typ.)