DATA SHEET

TDA3853T
TV IF amplifier and demodulator with TV-identification

Preliminary specification
File under Integrated Circuits, IC02

January 1992

Philips
Semiconductors

PHILIPS

TV IF amplifier and demodulator with TV-identification

TDA3853T

FEATURES

- Suitable for standards B/G (I, M, N, DK), see Table 1
- Gain controlled 3-stage IF amplifier with typically 80 MHz bandwidth
- High performance synchronous demodulator for negative and positive video modulation; passive regeneration of the reference signal
- Peak-sync-related AGC
- AGC output voltage take over point adjustable
- High sensitive TV identification based on vertical pulse duty cycle recognition; IDENT output
- Video off switch
- Sound trap buffer amplifier
- Tracking generator (AFT output) with Q-demodulator and internal 90 degree phase shifter for tracking the reference circuit
- Low supply voltage 5 V, low power consumption

GENERAL DESCRIPTION

Monolithic integrated circuit for vision IF signal processing in TV and VTR sets.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	4.75	5	6	V
I_P	supply current	–	46	–	mA
V_i	vision IF input signal sensitivity (RMS value, pins 1-20)	–	70	100	µV
	maximum vision IF input signal (RMS value, pins 1-20)	100	–	–	mV
G_v	IF gain control range	63	66	–	dB
$V_{o\ CVBS}$	buffered CVBS output signal on pin 12 (peak-to-peak value)	1.7	2	2.3	V
B	–3 dB video bandwidth (pin 12)	–	14	–	MHz
S/N	signal-to-noise ratio for video	55	60	–	dB
$\alpha_{1.1}$	intermodulation attenuation at yellow	53	56	–	dB
$\alpha_{3.3}$		60	–	–	dB
α_{spur}	suppression of spurious harmonics of video signal	22	26	–	dB
T_{amb}	operating ambient temperature	0	–	70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA3853T	20	mini-pack	plastic	SOT163A

Note

1. SOT163-1; 1997 January 8.

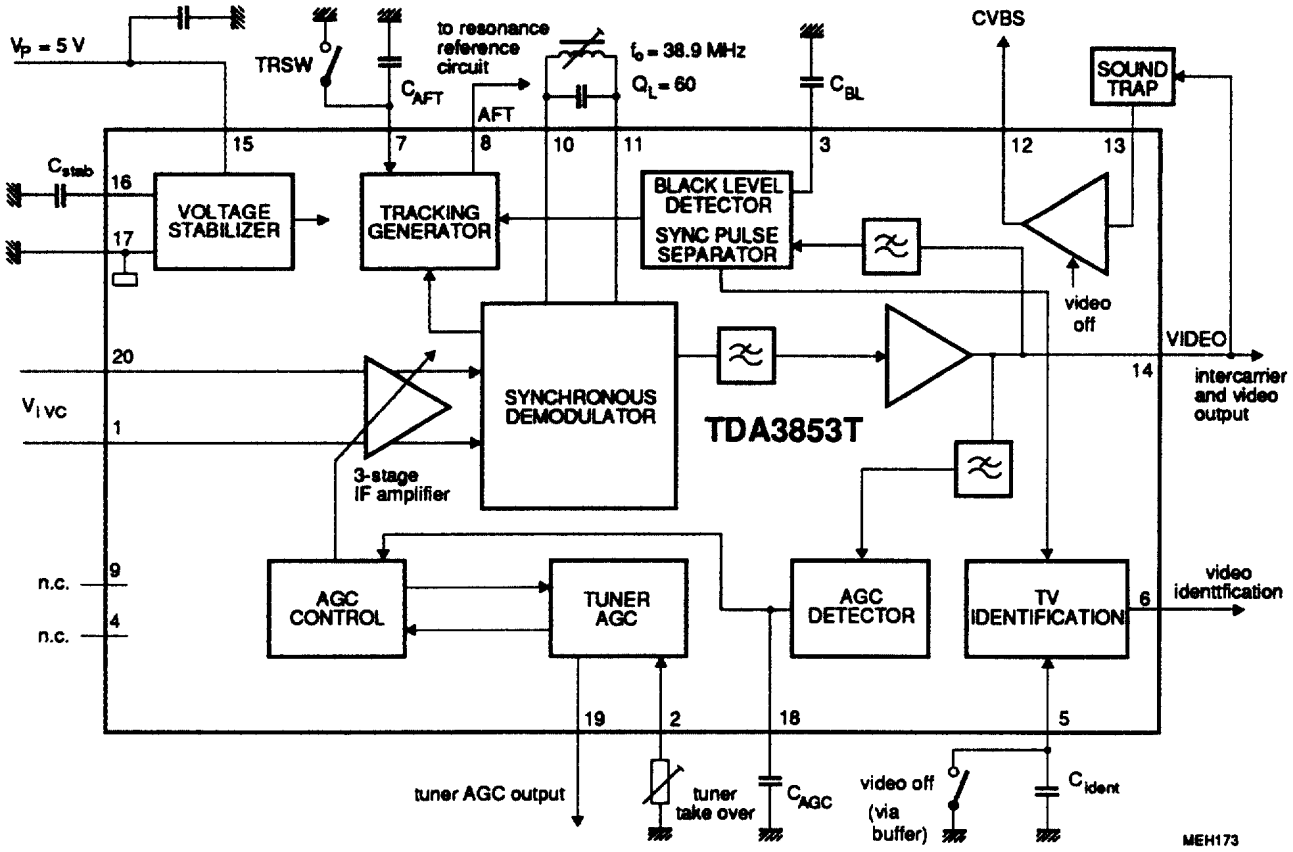


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\,a}$	1	balanced vision IF input a
TOP	2	tuner AGC take over adjustment point (TOP)
C_{BL}	3	capacitor for black level
n.c.	4	not connected
VIDOFF	5	video off input, identification capacitor
IDENT	6	TV identification output
TRSW	7	set input for tracking switch, tracking hold capacitor
AFT	8	automatic frequency tracking output
n.c.	9	not connected
RES1	10	resonance reference circuit for vision carrier
RES2	11	resonance reference circuit for vision carrier
CVBS	12	CVBS output (positive)
TRAP	13	video buffer amplifier input from sound trap
VIDEO	14	video and sound intercarrier output
V_P	15	+5 V supply voltage
C_{stab}	16	decoupling capacitor for voltage stabilizer
GND	17	ground (0 V)
C_{AGC}	18	capacitor for AGC
AGC	19	AGC output to tuner
$V_{i\,b}$	20	balanced vision IF input b

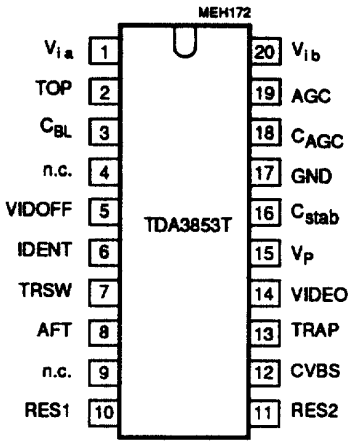


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA3853T is a TV IF amplifier/demodulator for negative modulation.

The IF input signal is amplified, gain-controlled and demodulated (Fig.1).

Vision IF amplifier and demodulator

The vision IF amplifier consists of three AC-coupled differential amplifiers. Gain control is achieved by current divider stages. Emitter feedback resistors in the differential amplifiers are optimized with respect to noise and signal capability.

Synchronous demodulator

The demodulator has a reference amplifier consisting of a differential amplifier with resistive load to provide passive vision carrier regeneration. This allows capacitive coupling of the resonance circuit to obtain a notch filter characteristic and tracking of the resonance circuit.
A cascaded limiter amplifier follows the reference amplifier to eliminate amplitude modulation. The limited IF reference signal is fed to the demodulator. The unlimited IF signal is fed via a phase correction network to the demodulator. The video amplifier is an operational amplifier with a wide bandwidth and internal feedback. The video and sound intercarrier signal is output on pin 14.

Video buffer amplifier

This operational amplifier has a wide bandwidth with internal feedback and frequency compensation. Gain and input impedance are adapted to operate with a ceramic sound trap. The switching functions are described in Table 1.

AGC detector and IF gain control

The video signal is fed through low-pass filters to attenuate the sound carriers and then is fed to the AGC detector.

Peak-sync AGC detection.
A special network provides current pulses to fast charge the AGC capacitor on pin 18 (gain reduction). This achieves a minimum of video distortion.
The AGC control converts the AGC capacitor voltage to three separate voltages to control the IF stages.

Sync pulse separator

The sync pulse separator separates the composite sync signal to gate the AFT. The vertical sync is used for identification. The input is band-limited to obtain a higher ident sensitivity.

Table 1 Switching functions of TDA3853T.

	VIDOFF PIN 5	TRSW PIN 7	VIDEO SIGNAL	IDENT PIN 6
pin	L	L(1)	video OFF	0.5 mA sink
setting	2.2 µF	L(1)	video ON	H or 0.5 mA sink

Note

1. capacitor on pin 7 means tracking active; LOW means tracking inactive

Tuner AGC

The tuner AGC output current is fed to the open-collector output on pin 19. The take-over point is adjusted externally at pin 2 to adapt the tuner and SAW filter to an optimum IF input level. The IF gain variation over the full tuner gain range (slip) is minimized to ensure a constant tuner output signal.

Identification

An analog integrating network followed by a window comparator identifies the video signal by detection of the duty cycle of the vertical sync pulses. The pulses charge the identification capacitor on pin 5.

Tracking generator (AFT)

A limited 90 degree phase-shifted vision carrier signal is fed to the AFT quadrature demodulator, internal RC networks provide active phase shifting. The linear IF signal is applied to the other AFT quadrature demodulator input. The AFT output signal is applied to a gating stage. Gating with the composite sync pulses activates the AFT demodulator. Therefore the AFT output is free from video modulation. The AFT capacitor (pin 7) is charged by the gated AFT current. The capacitor voltage is converted to an DC output current on pin 9 (open-collector sink/source currents).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	0	6.0	V
I_P	supply current on pin 15	–	55	mA
V_n	voltage on pins 6, 8 and 12	–0.3	V_P	V
$V_{5,7}$	voltage on pins 5 and 7	–0.3	5.5	V
V_{13}	voltage on pin 13	–0.3	5.0	V
V_{14}	voltage on pin 14	–0.3	4.2	V
V_{19}	voltage on pin 19	–0.3	13.2	V
$I_{2,16}$	current on pins 2 and 16	–	–200	µA
$I_{5,6}$	current on pins 5 and 6	–	–60	µA
I_7	current on pin 7	–	–100	µA
I_8	current on pin 8	–	–50	µA
I_{12}	current on pin 12	–	–10	mA
I_{14}	current on pin 14	–	–3	mA
T_{stg}	storage temperature range	–25	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
V_{ESD}	electrostatic handling[1] for all pins[2]	–	±300	V

Notes

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.
2. Pins 1, 10, 11 and 20 have special protection, the other pins have standard protection by diodes to V_P and GND (this excludes pins 15 (V_P) and 19 (tuner AGC output) which have standard protection to GND only).

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C, f_{VC} = 38.9 MHz; V_{iIF} = 10 mV rms; DSB video modulation; sync level for B/G.
Measurements taken in Fig.3 without notch components and video signal according to Fig.4 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 15)		4.75	5	6	V
I_P	supply current		–	46	55	mA
Standard set inputs (Table 1)						
V_{IL}	input voltage LOW, pins 5 and 7		0	–	0.8	V
Vision IF input (pins 1-20)						
V_i	input signal sensitivity (RMS value)	–1 dB video	–	70	100	μV
	maximum input signal (RMS value)	+1 dB video; note 1	100	–	–	mV
G_v	IF gain control range	Fig.6	63	66	–	dB
B	IF bandwidth	–3 dB	–	80	–	MHz
R_i	input resistance		–	2	–	kΩ
C_i	input capacitance		–	1.5	–	pF
V_I	DC voltage on pins 1 and 20		–	2.50	–	V
Synchronous demodulator (pins 10 and 11)						
$V_{o\ ref}$	picture carrier amplitude, pins 10-11 (peak-to-peak value)		–	1.6	–	V
$R_{10\text{-}11}$	integrated operating resistance		–	12	–	kΩ
$R_{L\ 10\text{-}11}$	load resistance		tbn	–	–	kΩ
Q_L	load Q-factor of resonance circuit; note 2	no notch components	55	60	–	
$V_{10,\ 11}$	DC voltage		–	2.8	–	V
Composite video output (pin 14)						
V_o	output signal (peak-to-peak value)		0.9	1.0	1.1	V
V_{14}	sync level		–	1.5	–	V
	ultra-white level		–	2.63	–	V
	upper video clipping level		–	4.3	–	V
	lower video clipping level		–	0.3	–	V
R_{14}	output resistance		–	–	10	Ω
I_{14}	output current	DC and AC	–	–	±1	mA
B	–1 dB video bandwidth	$C_{14} < 20$ pF	tbn	10	–	MHz
	–3 dB video bandwidth	$C_{14} < 20$ pF	tbn	14	–	MHz
RR	ripple rejection on pin 14	f_{ripple} = 70 Hz; note 3	tbn	30	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CVBS buffer amplifier (pins 12 and 13)						
R_{13}	input resistance		–	3.3	–	kΩ
C_{13}	input capacitance		–	2	–	pF
$V_{o\ CVBS}$	typical CVBS output signal on pin 14 (peak-to-peak value)	note 4	–	2	–	V
	CVBS output level	upper video clipping	–	4.25	–	V
		lower video clipping	–	0.3	–	V
		sync level	–	1.35	–	V
I_{12}	output current	DC and AC	–	–	±1	mA
R_{12}	output resistance		–	–	10	Ω
G_v	voltage gain	note 4	6.5	7	7.5	dB
B	–3 dB video bandwidth	$C_{14} < 20$ pF	tbn	14	–	MHz
RR	ripple rejection on pin 12	f_{ripple} = 70 Hz; note 3	tbn	35	–	dB
Measurements from IF input to CVBS output (pin 12)						
$V_{o\ CVBS}$	typical CVBS output signal on pin 12 (peak-to-peak value)	Fig.10	1.7	2	2.3	V
ΔV_o	deviation of CVBS output signal at B/G	50 dB gain control	–	–	0.5	dB
		30 dB gain control	–	0.1	–	dB
ΔG	differential gain	10 to 90% modulation	–	2	5	%
Δφ	differential phase	10 to 90% modulation	–	2	5	°
$tilt_H$	horizontal tilt		–	0.7	1.5	%
B	–2 dB video bandwidth	$C_L < 20$ pF	tbn	12	–	MHz
S/N	signal-to-noise ratio	note 5; Fig.5	–	58	–	dB
$\alpha_{1.1}$	intermodulation at “blue”, note 6	f = 1.1 MHz; Fig.8	56	58	–	dB
	intermodulation at “yellow”	f = 1.1 MHz	53	56	–	dB
$\alpha_{3.3}$	intermodulation at “blue”	f = 3.3 MHz	62	–	–	dB
	intermodulation at “yellow”	f = 3.3 MHz	60	–	–	dB
α_{1H}	residual vision carrier (RMS value)	fundamental wave	–	1	10	mV
α_{2H}		second harmonic	–	1	10	mV
α_{spur}	suppression of spurious video signal harmonics	transformer; Fig.4	22	26	–	dB
RR	ripple rejection on pin 12	f_{ripple} = 70 Hz; note 3	tbn	30	–	dB
AGC detector (pin 18)						
T_{resp}	response to an increasing amplitude step of 50 dB in input signal		–	1	10	ms
	response to a decreasing amplitude step of 50 dB in input signal		–	150	300	ms
V_{18}	gain control voltage on capacitor	full gain range	1.5	–	4	V
I_{18}	peak charging current (peak value)		–	–2	–	mA
	charging current		–	–0.5	–	mA
	discharging current		–	11	–	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Tuner AGC (pin 19)						
V_i	IF input signal for minimum starting point of tuner take over (RMS value)	input at pins 1-20	–	–	1	mV
	IF input signal for maximum starting point of tuner take over (RMS value)	input at pins 1-20	50	–	–	mV
ΔG_{IF}	IF gain variation	maximum ΔI_{AGC} = 1 mA	–	3	6	dB
V_{19}	permitted output voltage	from external	–	–	13.2	V
	saturation voltage	I_{19} = 1 mA	–	0.2	0.5	V
ΔV_{19}	variation of take over point by temperature	ΔT = 60 °C	–	2	3	dB
I_{19}	sink current	no tuner gain reduction; Fig.7	–	0	0.1	µA
		maximum tuner gain reduction	1.5	1.8	2.0	mA
RR	ripple rejecting on pin 19	f_{ripple} = 70 Hz; note 3	tbn	20	–	dB
TV identification and black level detector (pins 5, 6 and 3)						
V_i	IF input signal on pins 1-20 (RMS value)	TV identified	–	50	–	µV
C/N	carrier-to-noise ratio at IF input	TV identified; note 7	–	10	–	dB
V_{14}	minimum sync amplitude in relation to typical sync	identification on	–	30	–	%
V_6	output voltage for TV identified		4.5	4.95	V_P	V
	output voltage for TV not identified	I_7 = 500 µA	–	0.1	0.4	V
I_6	output current (sink)	no ident	–	500	–	µA
	allowed leakage current (source)	ident	–	–	–1	µA
V_5	voltage for “identification on”	2.2 µF capacitor on pin 5	–	2.6	–	V
I_{leak}	permitted leakage current (capacitor pin 5)		–	–	3	µA
$t_{p\,V}$	vertical pulse duty cycle for TV identified	$t_{sync}/t_{vertical}$	4	8	25	10^{-3}
Tracking generator, AFT (pins 7 and 8)		note 8				
V_8	maximum output voltage	note 9; Fig.9	4.3	–	4.7	V
	minimum output voltage		0.3	–	0.7	V
	permitted output voltage		–	–	V_P	V
I_8	sink output current		160	180	220	µA
	source output current		–160	–180	–220	µA
	offset output current		–	–	±20	µA
S	control steepness	$\Delta I_g/\Delta f$; note 9	–	2	–	µA/kHz
$\Delta\varphi$	phase offset spread for 38.9 MHz	note 10	–	–	±4	o
V_7	input voltage for TRSW	tracking off; Table 1	0	–	0.8	V
	(independent of other mode switches)	tracking on	open-circuit			V

Notes to the characteristics

1. Video signal is still gain controlled with 2 V (p-p) on output; but intermodulation figures are lowered.
2. AFT characteristic depends on Q-factor.
3. Ripple rejection for f = 50 to 100 Hz.
4. The 7 dB buffer gain accounts for 1 dB loss in the sound trap. Buffer output signal is typical 2 V (p-p). When no sound trap is applied, a 330 Ω resistor must be connected from output to input (from pin 14 to pin 13).
5. S/N is the ratio of the black-to-white amplitude (pin 12) and the RMS value of noise (black, pin 12). B = 5 MHz weighted in accordance with CCIR-567 at a source impedance of 50 Ω.
6. $\alpha_{1.1}$ = 20 log (V_o at 4.4 MHz / V_o at 1.1 MHz) + 3.6 dB; $\alpha_{1.1}$ value at 1.1 MHz related to black/white signal. $\alpha_{3.3}$ = 20 log (V_o at 4.4 MHz / V_o at 3.3 MHz); $\alpha_{3.3}$ value at 3.3 MHz related to colour carrier.
7. The carrier-to-noise ratio at IF input for “TV identified” is defined as the ratio of carrier (top sync, RMS value) and noise (RMS value). Conditions: 5 MHz bandwidth; V_{iIF} = 10 mV RMS (top sync) and a video signal of 2T + 20T + white bar.
8. A current source output is provided to match the AFT output signal to the different tuning systems. The internal 90 degrees phase shifter is matched for f_o = 38.9 MHz.
9. The AFT characteristic depends on Q_L of the resonance circuit (Q_L = 60, without notch components).
10. ±4° corresponds to ±23 kHz for Q_L as in Fig.1 (refer to note 9).

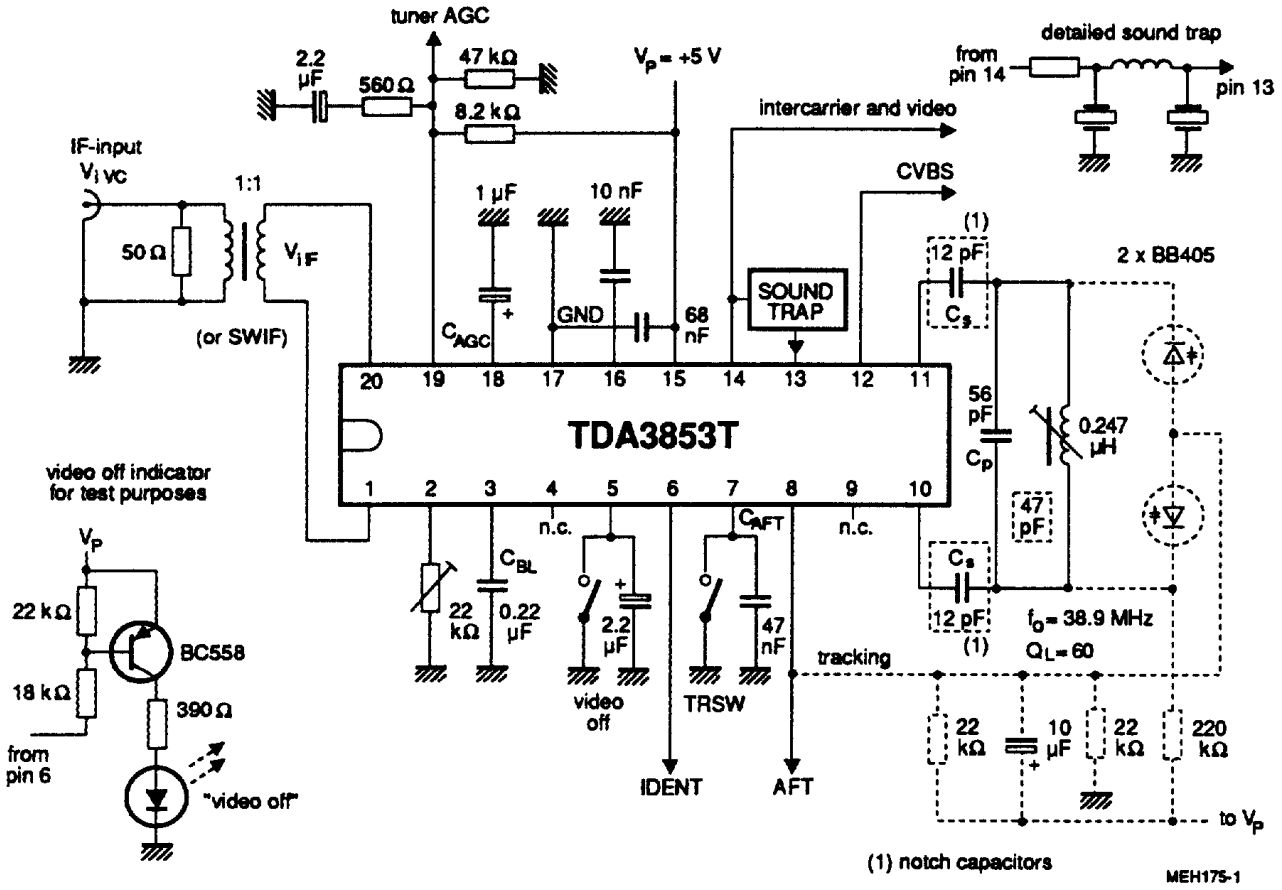


Fig.3 Test and application circuit. Test circuit without notch capacitors and with sound trap replaced by a 330 Ω resistor. Dashed components for tracking application only; application circuit with SWIF.

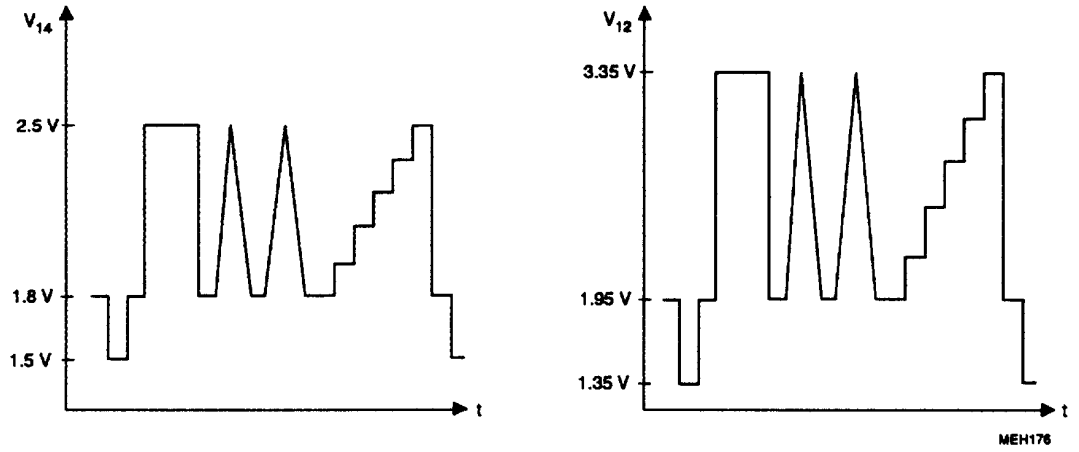


Fig.4 Video test signals.

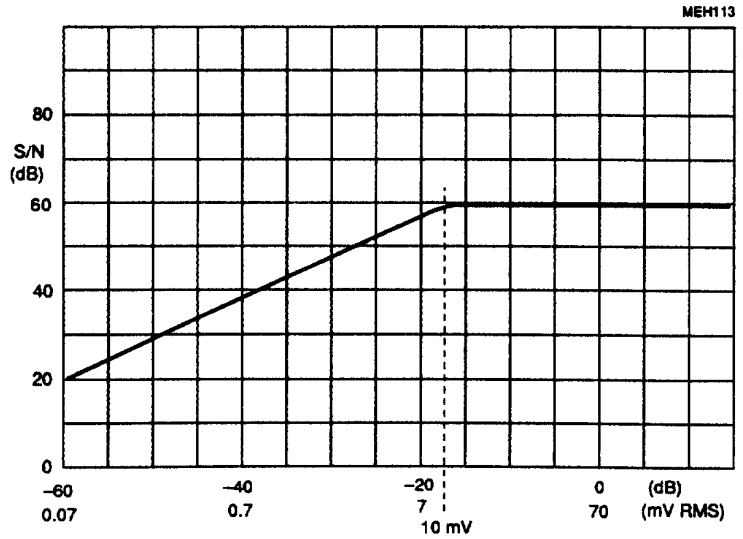


Fig.5 Signal-to-noise ratio (typical) as a function of IF input signal.

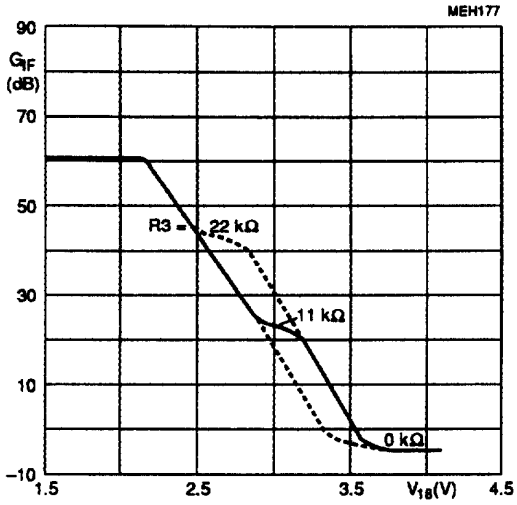


Fig.6 IF gain as a function of adjustment at pin 2.

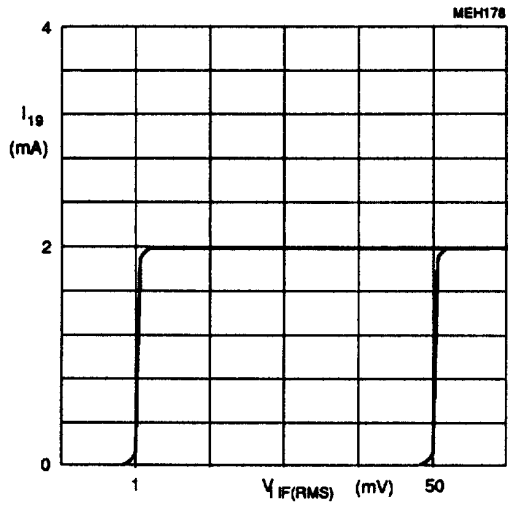


Fig.7 Tuner AGC characteristic.

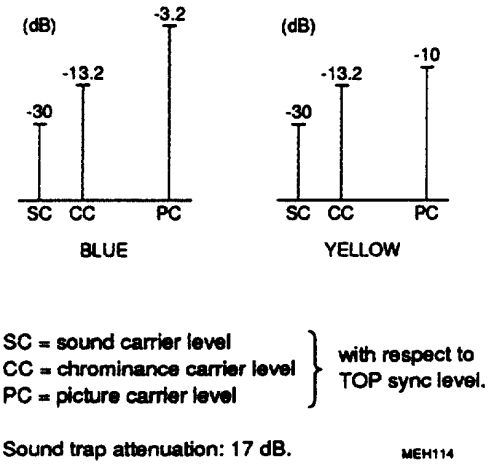


Fig.8 Input conditions for intermodulation measurements.

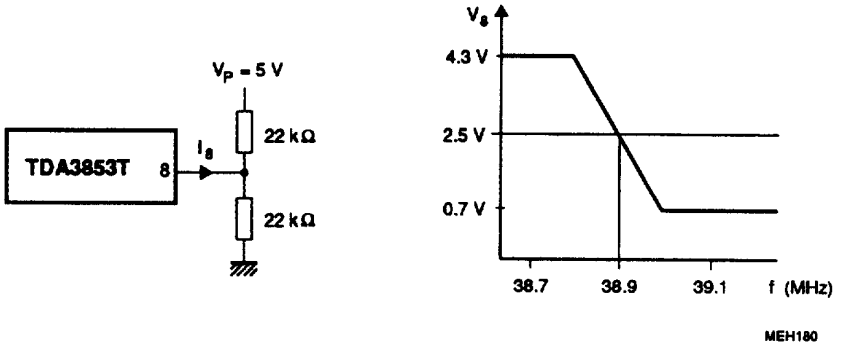


Fig.9 AFT characteristic.

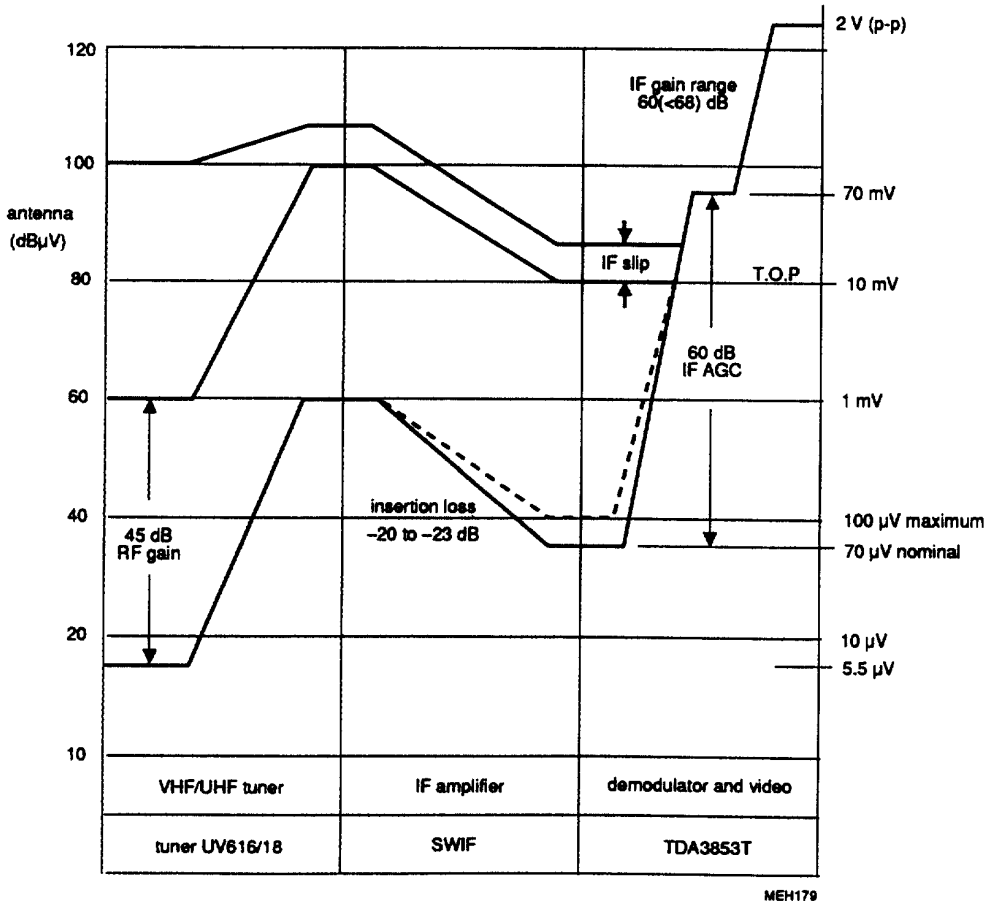


Fig.10 Front end level diagram.

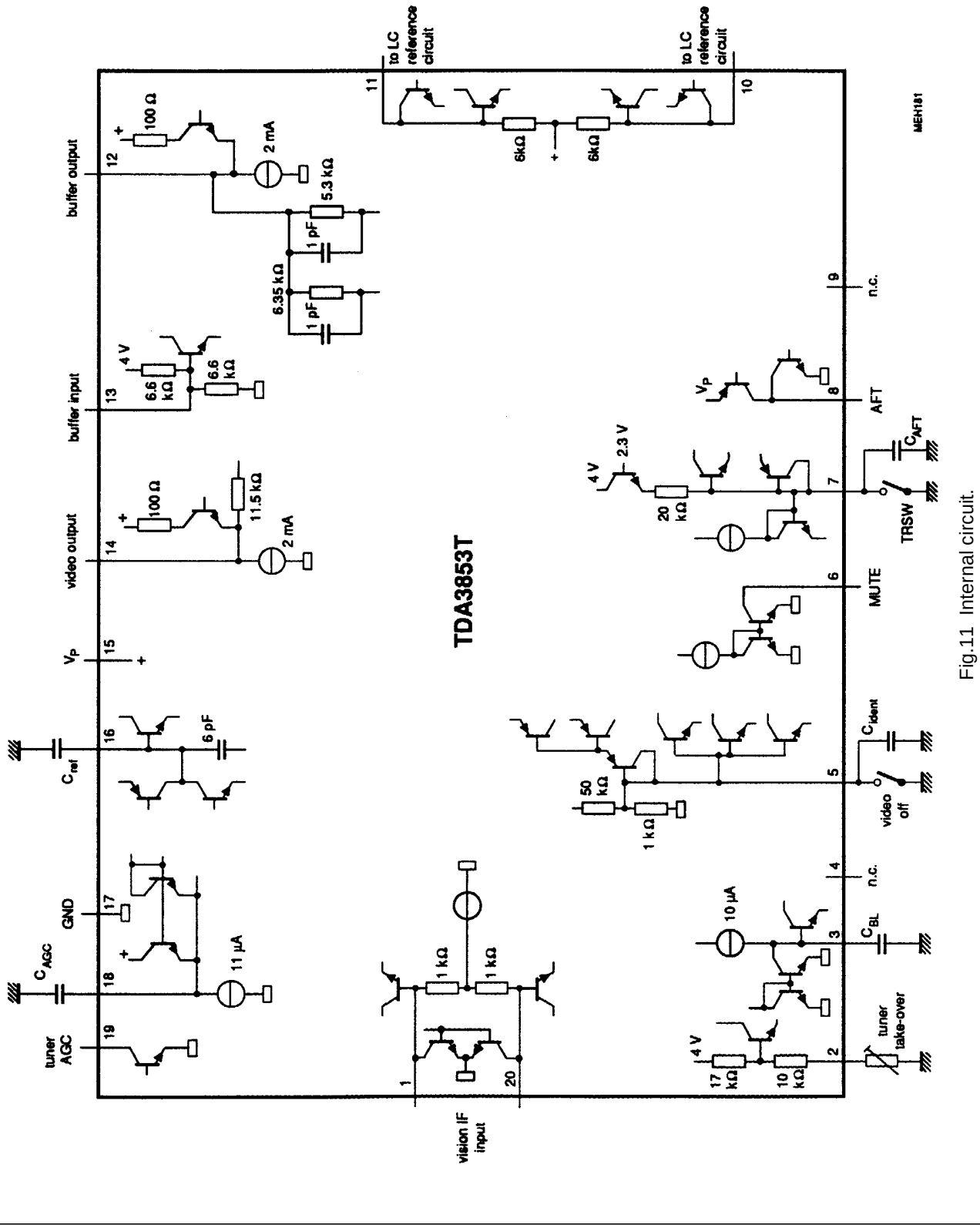
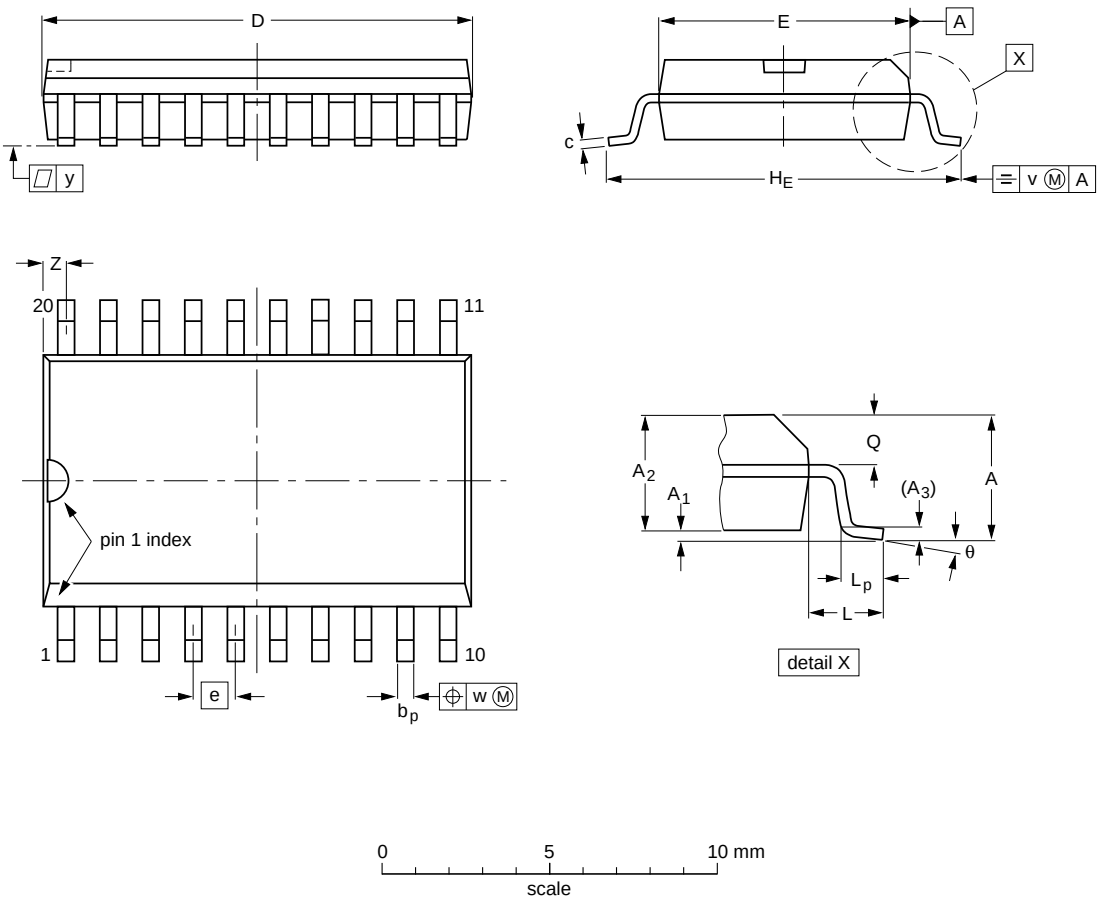


Fig.11 Internal circuit.

PACKAGE OUTLINE

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.