DATA SHEET

TDA5153

Pre-amplifier for Hard Disk Drive (HDD) with MR-read/inductive write heads

Preliminary specification
File under Integrated Circuits, IC11

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CONTENTS

Pre-amplifier for Hard Disk Drive (HDD) with MR-read/inductive write heads

TDA5153

1 FEATURES

- Designed for 4 (TDA5153BG) or 6 dual-stripe MR-read/inductive write heads
- Current bias-current sense architecture
- Single supply voltage (5.0 V ±10%); a separate write drivers supply pin can be biased from V_{CC} to 8 V +10%
- MR elements connected to ground (GND)
- Equal bias currents in the two MR stripes of each head
- On-chip AC couplings eliminate MR head DC offset
- 3-wire serial interface for programming
- Programmable high-frequency zero-pole gain boost
- Programmable write driver compensation capacitance
- Programmable MR bias currents and write currents
- 1-bit programmable read gain
- Sleep, standby, active and test modes available
- Measurement of head resistances in test mode
- In test mode, one MR bias current may be forced to a minimum current
- Short write current rise and fall times with near rail-to-rail voltage swing
- Head unsafe pin for signalling of abnormal conditions and behaviour
- Low supply voltage write-current inhibit (active or inactive)
- Supports servo writing
- Provides temperature monitor
- Thermal asperity detection with programmable threshold level
- Requires only one external resistor.

2 APPLICATIONS

- Hard Disk Drive (HDD).

3 GENERAL DESCRIPTION

The 5.0 V pre-amplifier for HDD described here is designed for five terminals, dual stripe Magneto-Resistive (MR)-read/inductive-write heads. The disks of the disk drive are connected to ground. To avoid voltage break-through between the heads and the disk, the MR elements of the heads are also connected to ground. The symmetry of the dual-stripe head-amplifier combination automatically distinguishes between the differential signals such as signals and the common-mode effects like interference. The latter are rejected by the amplifier.

The IC incorporates read amplifiers, write amplifiers, serial interface, digital-to-analog converters, reference and control circuits which operate on a single supply voltage of 5 V ±10%. The output drivers have a separate supply voltage pin which can be connected to a higher supply voltage of up to 8 V +10%. The complementary output stages of the write amplifier allow writing with near rail-to-rail peak voltages across the inductive write head.

The read amplifier has a low input impedance. The DC offset between the two stripes of the MR head is eliminated using on-chip AC coupling. Fast settling features are used to keep the transients short. As an option, the read amplifier may be left biased during writing so as to reduce the duration of these transients even more. Series inductance in the leads between the amplifier and MR heads influences the bandwidth which can be compensated by using a programmable high-frequency gain-boost (HF zero). HF noise and bandwidth can be attenuated using a programmable high-frequency gain-attenuator (HF pole).

On-chip digital-to-analog converters for MR bias currents and write currents are programmed via a 3-wire serial interface. Head selection, mode control, testing and servo writing can also be programmed using the serial interface. In sleep mode the CMOS serial interface is operational. Figure 1 shows the block diagram of the device.

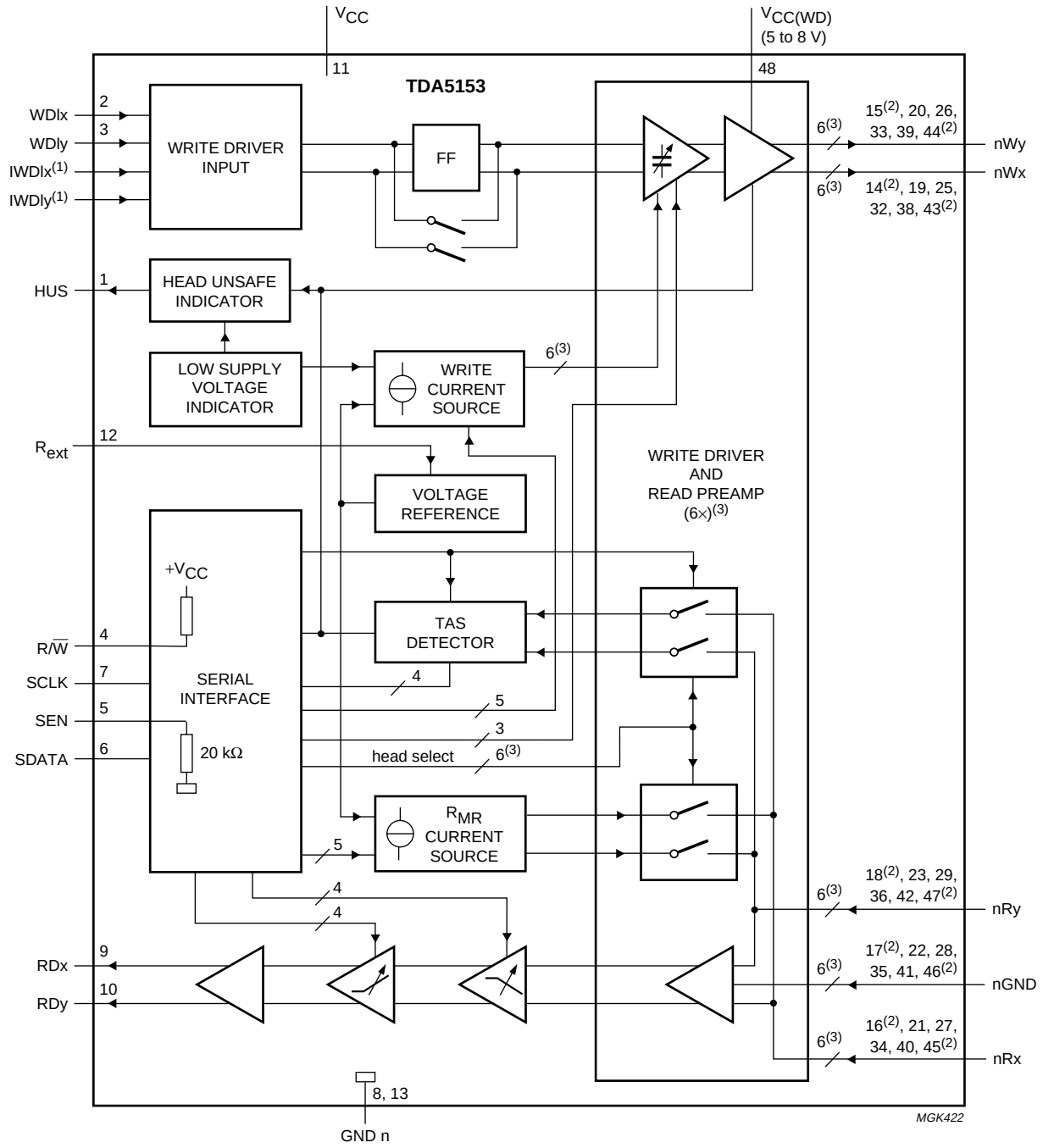
4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5153X	–	naked die	–
TDA5153AG; TDA5153BG	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

5 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.5	5.0	5.5	V
$V_{CC(WD)}$	write drivers supply voltage		V_{CC}	8.0	8.8	V
F	noise figure	R_{MR} = 28 Ω; I_{MR} = 10 mA; T_{amb} = 25 °C; f = 20 MHz	–	3.0	3.2	dB
V_{nir}	input referred noise voltage; see note 3 in Chapter 13	R_{MR} = 28 Ω; I_{MR} = 10 mA; T_{amb} = 25 °C; f = 20 MHz	–	0.9	1.0	nV/√Hz
$G_{v(dif)}$	differential voltage gain	from head inputs to RDx, RDy; R_{MR} = 28 Ω; I_{MR} = 10 mA				
		d4 = logic 0	–	160	–	
		d4 = logic 1	–	226	–	
$B_{-3\ db}$	−3 dB frequency bandwidth	upper bandwidth without gain boost (4 nH lead inductance)	–	220	–	MHz
CMRR	common mode rejection ratio; R_{MR} mismatch <5%	I_{MR} = 10 mA; f < 1 MHz	–	45	–	dB
		I_{MR} = 10 mA; f < 100 MHz	–	25	–	dB
PSRR	power supply rejection ratio (input referred); R_{MR} mismatch <5%	f < 1 MHz	–	80	–	dB
		f < 100 MHz	–	50	–	dB
t_r, t_f	rise/fall times (10% to 90%)	L_h = 150 nH; I_{WR} = 35 mA; f = 20 MHz				
		$V_{CC(WD)}$ = 8.0 V	–	–	1.8	ns
		$V_{CC(WD)}$ = 6.5 V	–	–	2.1	ns
$I_{MR(PR)}$	programming MR bias current	R_{ext} = 10 kΩ	5	–	20.5	mA
$I_{WR(PR)(b-p)}$	programming write current range (base-to-peak)	R_{ext} = 10 kΩ	20	–	51	mA
f_{SCLK}	serial interface clock rate		–	–	25	MHz

6 BLOCK DIAGRAM



Pin numbers correspond to TDA5153AG and TDA5153BG only. See Fig.3 and Chapter 7 for pinning of TDA5153X.

(1) Only available on naked die.

(2) Absent on TDA5153BG (4 channel version).

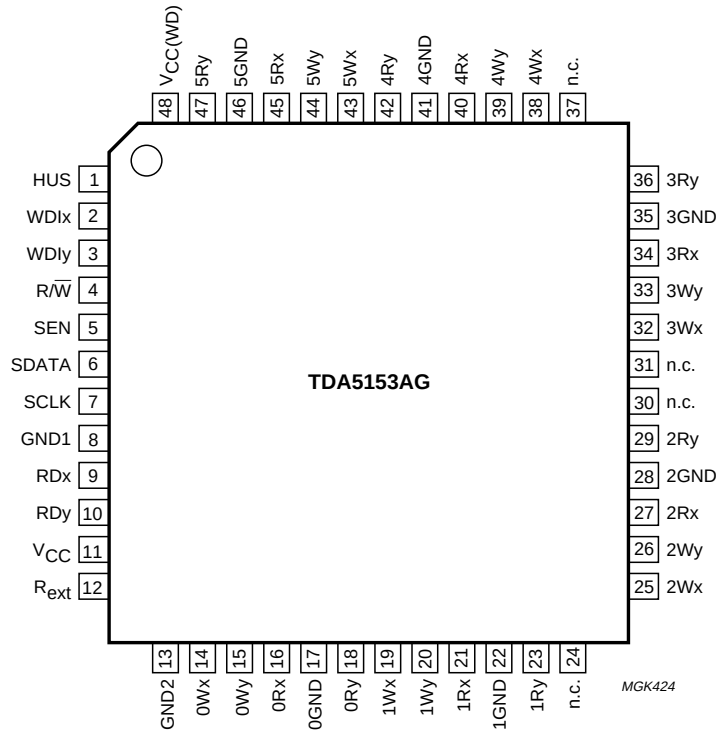
(3) 4 on TDA5153BG.

Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN		PAD	DESCRIPTION
	TDA5153AG	TDA5153BG	TDA5153X	
HUS	1	1	1	head unsafe output
WDIx	2	2	2	write data input (differential; voltage input)
WDIy	3	3	3	write data input (differential; voltage input)
IWDIx	–	–	4	write data input (differential; current input)
IWDIy	–	–	5	write data input (differential; current input)
R/$\overline{W}$	4	4	6	read/write (read = HIGH; write = LOW)
SEN	5	5	7	serial bus enable
SDATA	6	6	8	serial bus data
SCLK	7	7	9	serial bus clock
GND1	8	8	10	ground connection 1
RDx	9	9	11	read data output (differential x – y)
RDy	10	10	12	read data output (differential x – y)
GND3	–	–	13	ground connection 3
V_{CC}	11	11	14	supply voltage
R_{ext}	12	12	15	10 kΩ external resistor
GND2	13	13	16	ground connection 2
0Wx	14	–	17	inductive write head connection for head H0 (differential x – y)
0Wy	15	–	18	inductive write head connection for head H0 (differential x – y)
0Rx	16	–	19	MR-read head connection for head H0 (differential x – y)
0GND	17	–	20	ground connection for head H0
0Ry	18	–	21	MR-read head connection for head H0 (differential x – y)
n.c.	–	14	–	not connected
n.c.	–	15	–	not connected
n.c.	–	16	–	not connected
n.c.	–	17	–	not connected
n.c.	–	18	–	not connected
1Wx	19	19	22	inductive write head connection for head H1 (differential x – y)
1Wy	20	20	23	inductive write head connection for head H1 (differential x – y)
1Rx	21	21	24	MR-read head connection for head H1 (differential x – y)
1GND	22	22	25	ground connection for head H1
1Ry	23	23	26	MR-read head connection for head H1 (differential x – y)
n.c.	24	24	–	not connected
2Wx	25	25	27	inductive write head connection for head H2 (differential x – y)
2Wy	26	26	28	inductive write head connection for head H2 (differential x – y)
2Rx	27	27	29	MR-read head connection for head H2 (differential x – y)
2GND	28	28	30	ground connection for head H2
2Ry	29	29	31	MR-read head connection for head H2 (differential x – y)
n.c.	30	30	–	not connected

SYMBOL	PIN		PAD	DESCRIPTION
	TDA5153AG	TDA5153BG	TDA5153X	
n.c.	31	31	–	not connected
3Wx	32	32	32	inductive write head connection for head H3 (differential x – y)
3Wy	33	33	33	inductive write head connection for head H3 (differential x – y)
3Rx	34	34	34	MR-read head connection for head H3 (differential x – y)
3GND	35	35	35	ground connection for head H3
3Ry	36	36	36	MR-read head connection for head H3 (differential x – y)
n.c.	37	37	–	not connected
4Wx	38	38	37	inductive write head connection for head H4 (differential x – y)
4Wy	39	39	38	inductive write head connection for head H4 (differential x – y)
4Rx	40	40	39	MR-read head connection for head H4 (differential x – y)
4GND	41	41	40	ground connection for head H4
4Ry	42	42	41	MR-read head connection for head H4 (differential x – y)
5Wx	43	–	42	inductive write head connection for head H5 (differential x – y)
5Wy	44	–	43	inductive write head connection for head H5 (differential x – y)
5Rx	45	–	44	MR-read head connection for head H5 (differential x – y);
5GND	46	–	45	ground connection for head H5
5Ry	47	–	46	MR-read head connection for head H5 (differential x – y)
n.c.	–	43	–	not connected
n.c.	–	44	–	not connected
n.c.	–	45	–	not connected
n.c.	–	46	–	not connected
n.c.	–	47	–	not connected
$V_{CC(WD)}$	48	48	47	supply voltage for the write drivers
GND4	–	–	48	ground connection 4



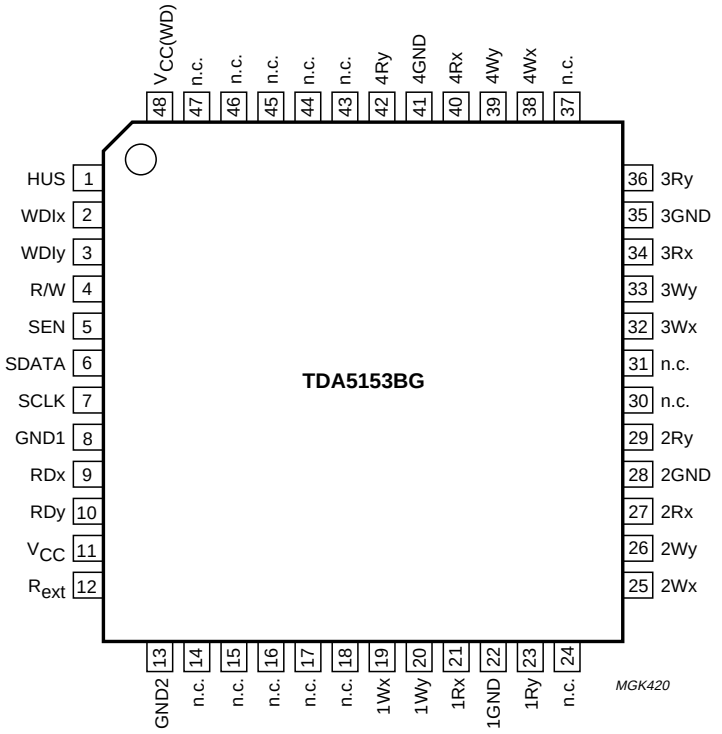


Fig.2 Pin configurations.

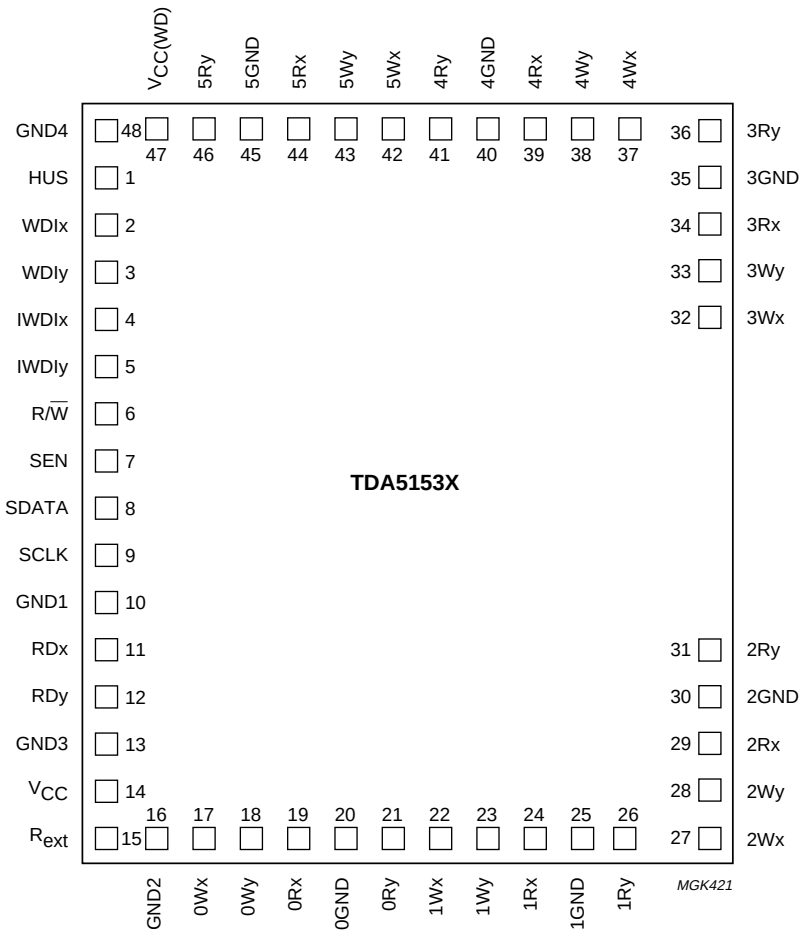


Fig.3 TDA5153X pad configuration.

8 FUNCTIONAL DESCRIPTION

8.1 Read mode

The read mode disables the write circuitry to save power while reading. The read circuitry is de-activated for write, sleep and standby modes. The read circuitry may also be biased during write mode to shorten transients.
The selected head is connected to a multiplexed low-noise read amplifier. The read amplifier has low-impedance inputs nRx and nRy (n is the number of the head) and low-impedance outputs RDx and RDy. The signal polarity is non-inverting from x and y inputs to x and y outputs.

Ambient magnetic fields at the MR elements result in a relative change in MR resistance

$$\frac{\Delta R_{MR}}{R_{MR}}$$

This change produces a current variation

$$\Delta I_{MR} = I_{MR} \times \frac{\Delta R_{MR}}{R_{MR}},$$

where I_{MR} is the bias current in the MR element.

The current variation is amplified to form the read data output signal voltage, which is available at RDx – RDy. AC coupling between MR elements and amplifier stages prevents the amplifier input stages from overload by DC voltages across the MR elements. A fast settling procedure shortens DC settling transients.

An on-chip generated stable temperature reference voltage (1.32 V), available at the R_{ext} pin, is dropped across an external resistor (10 kΩ) to form a global reference current for the write and the MR bias currents. The MR bias current DACs are programmed through the serial interface according to the following formula

$$I_{MR} = \frac{10\ k\Omega}{2 \cdot R_{ext}} (10 + 16 \cdot d4 + 8 \cdot d3 + 4 \cdot d2 + 2 \cdot d1 + d0)$$

(in mA), where d4 to d0 are bits (either logic 0 or logic 1). At power-up, all bits are set to logic 0, which results in a default MR current of 5 mA. The adjustable range of the MR currents is 5 mA to 20.5 mA. The MR bias currents are equal for the two stripes of each head. The gain amplifier is 1-bit programmable. The amplifier gain can be set to its nominal value or to the nominal value +3 dB.

8.2 Write mode

To minimize power dissipation, the read circuitry may be disabled in write mode. The write circuitry is disabled in read, sleep and standby modes. In write mode, a programmable current is forced through the selected two terminals inductive write head. The push-pull output drivers yield near rail-to-rail voltage swing for fast current polarity switching.

The differential write data input WDIx – WDIy is PECL (Positive Emitter Coupled Logic) compatible. The write data flip-flop can either be used or passed-by. In the case that the write data flip-flop is used, current polarity is toggled at the falling edges of the $V_{data} = V_{WDIx} - V_{WDIy}$. Switching to Write Mode initializes the data flip-flop so that the write current flows in the write head from x to y. In the case that the write data flip-flop is not used, the signal polarity is non-inverting from x and y inputs to x and y outputs.

The write current magnitude is controlled through on-chip DACs. The write current is defined as follows:

$$I_{WR} = \frac{10\ k\Omega}{R_{ext}} (20 + 16 \cdot d4 + 8 \cdot d3 + 4 \cdot d2 + 2 \cdot d1 + d0)$$

(in mA) where d4 to d0 are bits (either logic 0 or logic 1). The adjustable range of the write current is 20 mA to 51 mA. At power-up, the default values d4 = d3 = d2 = d1 = d0 = logic 0 are initialized, corresponding to I_{WR} = 20 mA. I_{WR} is the current provided by the write drivers: the current in the write coil and in the damping resistor together. The static current in the write coil is

$$\frac{I_{WR}}{1 + \frac{R_h}{R_d}},$$

where R_h is the resistance of the coil including leads and R_d is the damping resistor.

8.3 Sleep mode

In sleep mode, the device is accessible via the serial interface. All circuits are inactive, except the circuits of the CMOS serial interface and the circuit which forces the data registers to their default values at power-up and which fixes the DC level of RDx – RDy (required when operating with more than one amplifier). Typical static current consumption is –30 μA. Dynamic current consumption during operation of the serial interface in the sleep mode and owing to external activity at the inputs to the serial interface is not included. In all modes including the sleep mode, data registers can be programmed. Sleep is the default mode at power-up. Switching to other modes takes less than 0.1 ms.

8.4 Standby mode

The circuit can be put in standby mode using the serial interface. In standby mode, typical DC current consumption is 330 μA. Transients from standby mode to active mode are two orders of magnitude shorter than from sleep mode to active mode. This is important in the case of cylinder mode operation with multiple amplifiers.
All amplifiers can operate from standby mode and all head switch times can be kept just as short as in the case of operation with a single amplifier. Head switching times are summarized in the switching characteristics.

8.5 Active mode

Active mode is either read mode or write mode depending on the R/$\overline{W}$ pin.

8.6 Bi-directional serial interface

The serial interface is used for programming of the device and for reading of status information. 16 bits (8 bits for data and 8 for address) are used to program the device. The serial interface requires 3 pins: SDATA, SCLK and SEN. These pins (and R/$\overline{W}$) are CMOS inputs. The logic input R/$\overline{W}$ has an internal 20 kΩ pull-up resistor and the SEN logic input has an internal 20 kΩ pull-down resistor. Thus, in case the SEN line is opened, no data will be registered and in case the R/$\overline{W}$ line is opened, the device will never be in write mode.

SDATA: serial data; bi-directional data interface. In all circumstances, **the LSB is transmitted first**.

SCLK: serial clock; 25 MHz clock frequency.

SEN: serial enable; data transfer takes place when SEN is HIGH. When SEN is LOW, data and clock signals are prohibited from entering the circuit.

Three phases in the communication are distinguishable: addressing, programming and reading. Each communication sequence starts with an addressing phase, followed by either a programming phase or a reading phase.

8.7 Addressing

When SEN goes HIGH, bits are latched in at rising edges of SCLK. The first eight bits a7 to a0, starting with a0, are shifted serially into an address register. If SEN goes LOW before 16 bits have been received, the operation is ignored. When more than 16 bits (address and data) are latched in before SEN goes LOW, the first 8 bits are interpreted as an address and the last 8 bits as data. SEN should go HIGH at least 5 ns before the first rising edge of SCLK. Data should be valid at least 5 ns before and after a rising edge of SCLK. The bits a7 to a4 constitute the register address.To validate the communication with the preamplifier, bits a1, a2 and a3 have to be programmed as (1, 0, 0).

If bit a0 = logic 0, a programming sequence starts.
If bit a0 = logic 1, reading data from the pre-amplifier can start.

8.8 Programming data

If a0 = logic 0, the last eight bits d7 to d0 before SEN goes LOW are shifted into an input register. Bits d6 and d7 are don't care. When SEN goes LOW, the communication sequence is ended and the data in the input register is copied in parallel to the data register that corresponds to the decoded address a7 to a4. SEN should go LOW at least 5 ns after the last rising edge of SCLK.

8.9 Reading data

Immediately after the IC detects that a0 = logic 1, data from the data register (address a7 to a4) is copied in parallel to the input register. Two wait clock cycles must follow before the controller can start inputting data. At the first falling edge of SCLK after the 2 wait rising edges of SCLK, the LSB d0 is placed on SDATA line followed by d1 at the next falling edge of SCLK etc. If SEN goes LOW before 8 address bits (a7 to a0) have been detected, the communication is ignored.

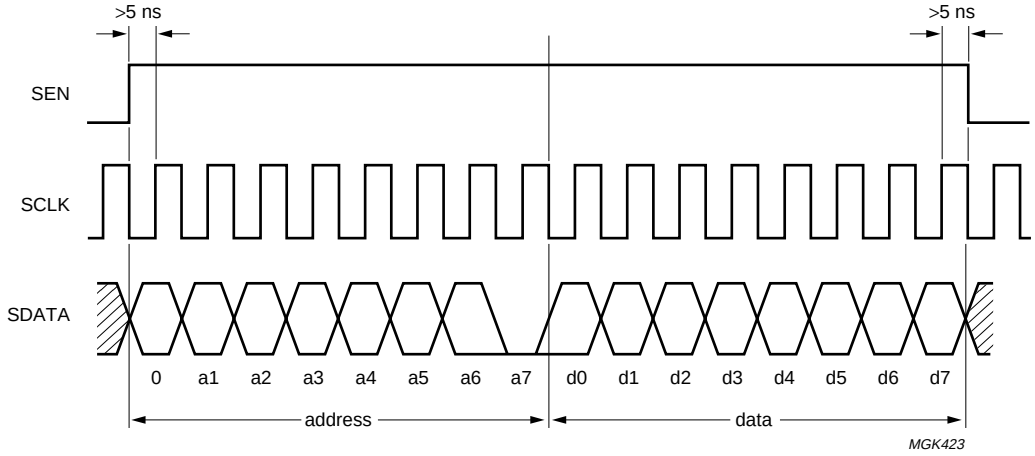


Fig.4 Timing diagram of the serial interface operation; writing sequence (a0 = 0).

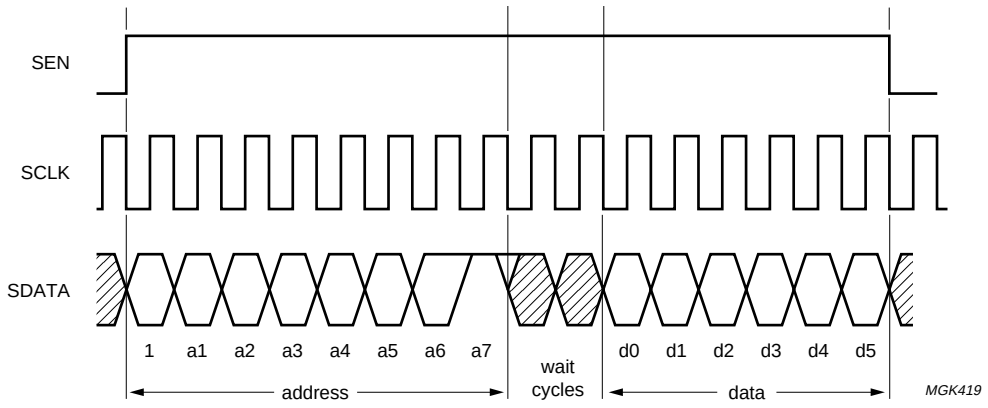


Fig.5 Timing diagram of the serial interface operation; reading sequence (a0 = 1).

8.10 Operation of the serial interface

8.10.1 CONFIGURATION

d0

By default (d0 = logic 0), write data passes from the write data input via the data flip-flop to the write driver. The write driver toggles the current in the head at the falling edges of

$$V_{data} = \frac{V_{WDIx} - V_{WDIy}}{2}$$

When d0 = logic 1, the flip-flop is not used. The signal polarity is non-inverting from WDIx and WDIy to Wx and Wy.

d1

By default (d1 = logic 0) the pre-amplifier senses PECL write signals at WDIx and WDIy. **d1 should remain logic 0**.

d2

By default, (d2 = logic 0) the write current is inhibited under low supply voltage conditions. The write current inhibit is made inactive by programming d2 to logic 1.

d3

By default (d3 = logic 0), in write mode low supply voltage, open head, and other conditions are monitored and flagged at HUS. If d3 = logic 1, HUS is LOW in write mode and HIGH in read mode.

d4

The amplifier read gain may be programmed in the configuration register. By default (d4 = logic 0), the read gain is typically 160 with R_{MR} = 28 Ω. If d4 = logic 1, the read amplifier typical gain is 3 dB higher (i.e. 226 if R_{MR} = 28 Ω).

d5

In order to minimize the write-to-read recovery times, the first stage of the read amplifier may be kept biased during write mode. By default, (d5 = logic 0) the read amplifier is powered-down during write mode, and the fast settling procedure is activated after write-to-read switching. If d5 = logic 1 the read amplifier is kept biased during write mode, and the fast settling procedure still occurs if the head is changed or the MR current is re-programmed.

8.10.2 POWER CONTROL

By default d0 = d1 = logic 0, the pre-amplifier powers-up in sleep mode. If d1 = logic 0, d0 = logic 1 or d1 = logic 1, d0 = logic 0 the circuit goes in standby mode.

If d1 = d0 = logic 1, the circuit goes in active mode, (read or write mode depending on the R/$\overline{W}$ input).

8.10.3 HEAD SELECT

d2, d1 and d0 are used to select head H0 to H5 for the 6 channel version and to select head H1 to H4 for the 4 channel version.

8.10.4 SERVO WRITE

The circuit is prepared for servo writing. However, the chip will not be guaranteed.

8.10.5 TEST

d2 = d1 = d0 = logic 0. The circuit is not in test mode. This is the default situation.

8.10.5.1 MR head test

d2 = logic 0, d1 = logic 0, d0 = logic 1. In read mode, the voltages at Rx and Ry (at the top of the MR elements) of the selected head are fed to RDx and RDy outputs. By measuring the output voltages single-ended at two different I_{MR} currents, the MR resistance can be accurately measured according to the following formula:

$$R_{MRx} = \frac{V_{RDx1} - V_{RDx2}}{I_{MRx1} - I_{MRx2}}$$ for the x side for instance.

Open head and head short-circuited to ground conditions can therefore be detected.

d2 = logic 0, d1 = logic 1, d0 = logic 0. Same as before, with the difference that I_{MR2} is fixed to a minimum constant value of 5 mA. Measuring in the same way as above with I_{MR1} > 5 mA, enables the detection of MR elements connected together.

8.10.5.2 Temperature monitor

d2 = logic 0, d1 = logic 1, d0 = logic 1. The temperature monitor voltages are connected to RDx and RDy. The output differential voltage depends on the temperature according to: $dV = -0.00364 \times T + 1.7$, $0 < T < 140$ °C The temperature may be measured with a typical precision of 5 °C.

8.10.5.3 Thermal asperity detector

d2 = logic 1, d1 = don't care, d0 = either logic or 1. Unlike the above tests, the thermal asperity detection does not use the RDx to RDy outputs. Thus, the reader is fully operational. In case a thermal asperity is detected, it is flagged at the HUS pin.

The threshold voltage for the thermal asperity detection is 2-bit programmable. These 2 bits consist of d0 (LSB) of the test mode register (address = 0XXX0110), as the MSB, and b2 of the compensation register (address = 0XXX0111).

$V_{th} = (210 + 560 \cdot d0 + 280 \cdot b2)\ \mu V$,

where d0 is d0 of test mode register and b2 is d2 of capacitor compensation register.

8.10.6 Write amplifier programmable capacitors

By default (d2 = d1 = d0 = logic 0) the programmable capacitors are zero. These capacitors are used to improve the performance of the write amplifier according to the write amplifier output load.

8.10.7 High frequency gain attenuator pole register

By default (d3 = d2 = d1 = d0 = logic 0), the high frequency gain attenuator is not active. The gain attenuator provides a pole which limits the bandwidth and reduces the high-frequency noise. The HF pole can be used in combination with the HF zero in order to boost the HF gain locally and yet limit the very high frequency noise enhancement.

8.10.8 High frequency gain boost register

By default (d3 = d2 = d1 = d0 = logic 0), the high frequency gain boost is not active. The gain boost provides a zero which allows to optimize the bandwidth of the read amplifier and to correct for attenuation caused by series inductances in the leads between the MR-heads and the read amplifier inputs.

8.10.9 Settle pulse

By default (d2 = d1 = d0 = logic 0) the settle pulse has a nominal duration of 3 µs. Its value can be programmed from 2.125 µs to 3 µs according to the following formula:

$$t_{st} = 2 + \frac{1}{(4 \cdot d2 + 2 \cdot d1 + 1 \cdot d0 + 1)}\ \mu s$$

8.10.10 Address registers; note 1

A7	A6	A5	A4	A3	A2	A1	A0	DESCRIPTION
0	0	0	0	0	0	1	0	configuration register: d0 = 0: use data flip-flop; d0 = 1: by-pass data flip-flop d1 = 0: the WDI inputs are PECL levels; d1 = 1: invalid d2 = 0: write current inhibit active; d2 = 1: write current inhibit inactive read mode: d3 = 0: HUS active; d3 = 1: HUS HIGH write mode: d3 = 0: HUS active; d3 = 1: HUS LOW d4 = 0: read gain nominal; d4 = 1: read gain nominal + 3 dB d5 = 0: read amplifier OFF during write mode; d5 = 1: read amplifier ON during write mode
0	0	0	1	0	0	1	0	power control register: (d1, d0) = (0, 0): sleep mode (d1, d0) = (1, 0) or (0, 1): standby mode (d1, d0) = (1, 1): active mode (write or read)
0	0	1	0	0	0	1	0	head select register: 6 channels: (d2,d1,d0) = (0,0,0) to (1,0,1): H0 to H5 4 channels: (d2,d1,d0) = (0, 0, 1) to (1, 0, 0): H1 to H4

A7	A6	A5	A4	A3	A2	A1	A0	DESCRIPTION
0	0	1	1	0	0	1	0	MR current DAC register: $I_{MR} = 0.5 \times \left(\frac{10\ k\Omega}{R_{ext}}\right) \times (10 + 16 \cdot d4 + 8 \cdot d3 + 4 \cdot d2 + 2 \cdot d1 + 1 \cdot d0)$ mA
0	1	0	0	0	0	1	0	write current DAC register: $I_{WR} = \left(\frac{10\ k\Omega}{R_{ext}}\right) \times (20 + 16 \cdot d4 + 8 \cdot d3 + 4 \cdot d2 + 2 \cdot d1 + 1 \cdot d0)$ mA
0	1	0	1	0	0	1	0	servo write register: (d0, d1) = (0, 0) = one head (d0, d1) = (1, 1) = all heads
0	1	1	0	0	0	1	0	test mode register: (d2,d1,d0) = (0,0,0) = not in test mode (d2,d1,d0) = (0,0,1) = read head test ($I_{MR1} = I_{MR2}$) (d2,d1,d0) = (0,1,0) = read head test (I_{MR2} = 5 mA fixed) (d2,d1,d0) = (0,1,1) = temperature monitor (d2,d1,d0) = (1, X, d0) = thermal asperity detection $V_{th} = (210 + 560 \cdot d0 + 280 \cdot b2)$ µV , see note 2
0	1	1	1	0	0	1	0	compensation capacitor register: equivalent differential capacitance: $(4 \cdot d2 + 2 \cdot d1 + 1 \cdot d0) \times 2$ pF
1	0	0	0	0	0	1	0	high frequency gain attenuator register: nominal pole frequency: $\frac{800\ MHz}{8 \cdot d3 + 4 \cdot d2 + 2 \cdot d1 + 1 \cdot d0}$
1	0	0	1	0	0	1	0	high-frequency gain boost register: nominal zero frequency: $\frac{800\ MHz}{8 \cdot d3 + 4 \cdot d2 + 2 \cdot d1 + 1 \cdot d0}$
1	0	1	0	0	0	1	0	settle time register: settle time: $t_{st} = 2 + \frac{1}{(4 \cdot d2 + 2 \cdot d1 + 1 \cdot d0 + 1)}$ µs
1	1	1	1	0	0	1	1	chip ID register: $ID = 8 \cdot d3 + 4 \cdot d2 + 2 \cdot d1 + 1 \cdot d0$, d3 to d0 are preset to (0, 0, 1, 1)
a7	a6	a5	a4	0	0	1	1	when a0 = 1, data from the register with address a7 to a4 is read out on SDATA

Notes

1. Not used bits in the registers (indicated by X) are don't care. Default data, initialized at power-up, is zero in all registers. For V_{CC} < 2.5 V, the register contents are not guaranteed.
2. V_{th} programming uses both test mode register and compensation capacitor register. d0 in the formula above is the LSB of the test mode register and b2 is the data bit d2 of the compensation register.

8.11 Head unsafe

The HUS pin is an open-collector output. Consequently, when the pin is not connected to an external pull-up resistor, HUS is LOW. HUS pins can be connected together in case of operation with more than one amplifier. It is used to detect abnormal/unexpected operation.

Sleep mode: HUS is HIGH, to permit working with more than one amplifier.

Standby mode: HUS is HIGH, to permit working with more than one amplifier.

Read mode:

- if in the configuration register d3 = 1, HUS is HIGH
- if in the configuration register d3 = 0, HUS goes LOW for:
  - R_{ext} pin open, short-circuited to ground or to V_{CC} (read current too low or too high)
  - Low V_{CC} and $V_{CC(WD)}$ conditions. A low supply voltage detector is placed close to the V_{CC} and $V_{CC(WD)}$ pins.

Detection of low V_{CC} (main general supply): a V_{CC} supply voltage below 4.0 V ±5% is flagged to the HUS pin. The voltage detection range is then 4.2 to 3.8 V with an hysteresis of 110 mV ±10%. Detection of low $V_{CC(WD)}$ (writer dedicated supply): a fault will be flagged at HUS pin if $V_{CC(WD)}$ drops 0.8 V ±10% below V_{CC}. One must be aware that such a detection is only aimed to warn for a catastrophic situation. Indeed, $V_{CC(WD)}$ should never be below V_{CC}.

Test mode: HUS is HIGH except when the TAS detector is ON. If a thermal asperity is detected, HUS goes LOW.

Servo write mode: HUS is LOW

Write mode:

- if in the configuration register d3 = 1, HUS is LOW
- if in the configuration register d3 = 0, HUS goes HIGH for: the write current may be inhibited if d1 = 0 in the configuration register.
  - R_{ext} pin open, short-circuited to ground or to V_{CC} (write current too low or too high)
  - Write data input frequency too low (WDIx – WDIy)
  - Write head Wx – Wy open, Wx or Wy short-circuited to ground (switching to write mode makes HUS LOW; after the transient the HUS detection circuitry is activated; the target for the head-open detect time is 15 ns)
  - Write-head still left biased while not selected
  - Low V_{CC} and $V_{CC(WD)}$ conditions (write current inhibit can be active or inactive).

The same detector is used for read and write mode. HUS goes LOW again between 0.5 and 1 μs after the last unsafe condition was detected.

8.12 HUS survey

HUS			DATA BIT D3	
MODE	**STATE**		**0**	**1**
Sleep mode	–	–	HIGH	HIGH
Standby mode	–	–	HIGH	HIGH
Active mode	Read	Read mode	ACTIVE	HIGH
		A-test mode[1]	HIGH	HIGH
		TAS mode	ACTIVE	ACTIVE
	Write	Write mode	ACTIVE	LOW
		A-test mode[1]	HIGH	HIGH
		Servo mode[2]	LOW	LOW

Notes

1. HUS survey: A-test mode = analog test mode.
2. In servo mode, the performance of the IC is not guaranteed.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.5	+6.0	V
$V_{CC(WD)}$	write driver supply voltage	–0.5	+9.5	V
V_{IL}	LOW level digital input voltage	–0.5	+5.5	V
V_{IH}	HIGH level digital input voltage	–0.5	+5.5	V
V_{n1}	voltage on all pins except V_{CC}, read inputs nRx, nRy and write outputs nWx, nWy (n = 0 to 9)	–0.5	+5.5	V
	but not higher than	–	V_{CC} + 0.5	V
V_{n2}	voltage on write driver outputs nWx, nWy	–0.5	+8.8	V
	but not higher than	–	$V_{CC(WD)}$ + 0.8	V
V_{n3}	voltage on read inputs nRx, nRy	–0.5	1	V
I_{nGND}	current through pins nGND	–	0.1	A
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	150	°C

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS device.

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient			
	TDA5153AG, TDA5153BG	in free air	70	K/W
	TDA5153X		see note 1	

Note

1. The TDA5153X is shipped in naked dies. The thermal resistance depends on the flex used.

12 RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP	MAX.	UNIT
V_{CC}	supply voltage range	note 1	4.5	–	5.5	V
$V_{CC(WD)}$	write driver supply voltage	note 2	V_{CC}	–	8.8	V
V_{IH}	HIGH level input voltage (CMOS)		3.5	–	V_{CC}	V
V_{IL}	LOW level input voltage (CMOS)		0	–	0.8	V
$V_{i(dif)(p-p)}$	differential input voltage (peak-to-peak value)	note 3	0.4	0.7	1.5	V
$V_{IH(PECL)}$	HIGH level PECL input voltage	note 3	1.5	2.85	V_{CC}	V
$V_{IL(PECL)}$	LOW level PECL input voltage	note 3	–	2.15	–	V
T_{amb}	ambient temperature		0	–	70	°C
T_j	junction temperature	reading	–	–	110	°C
		writing ($V_{CC(WD)}$ = 8 V)	–	–	130	°C
R_{MR}	MR element resistance		15	28	34	Ω
ΔR_{MR}	R_{MR} mismatch	note 4	–	–	4	Ω
$L_{l(tot)}$	total lead inductance to the head	in each lead; note 5	–	35	–	nH
$R_{l(tot)}$	total lead resistance to the head	in each lead; note 5	–	1.5	–	Ω
V_{MR}	voltage on top of MR elements	note 6	–	–	0.5	V
$V_{sig(dif)(p-p)}$	differential MR head input signal (peak-to-peak value)		0.4	1	2	mV
L_{wh}	write head inductance	including lead; note 5	–	0.15	–	µH
R_{wh}	write head resistance	including lead; note 5	–	10	–	Ω
C_{wh}	write head capacitance	including lead; note 5	–	5	–	pF
R_{ext}	external reference resistor	$I_{ref} = \frac{V_{ref}}{R_{ext}}$	–	10	–	k Ω

Notes

1. A supply by-pass capacitor from V_{CC} to ground or a low-pass filter may be used to optimize the PSRR.
2. The supply voltage $V_{CC(WD)}$ must never be below V_{CC} in normal mode, and two diode voltages above V_{CC} in servo mode.
3. The given values should be interpreted in such a way that the single-ended voltage could swing 0.2 to 0.75 V and that the common mode voltage should be such that for any of the two states, $V_{IH(max)} < V_{CC}$ and $V_{IL(min)} > 1.5$ V. PECL voltage swing: a wider peak-to-peak voltage swing can be used. In that case a current will flow through the WDI inputs. This current is approximately equal to $\frac{(WDIx - WDIy) - 1.4}{200}$
4. The mismatch refers to the resistance of the two stripes of the same head. This is defined as follows: $\Delta R_{MR} = |R_{MR1} - R_{MR2}|$
5. These parameters depend on the head model. The values given are those used for testing.
6. The combination of maximum head resistance, lead resistance and bias current is not permitted. To avoid voltage break-through between heads and disk, the voltage over the MR elements is limited by two diodes.

13 CHARACTERISTICS

V_{CC} = 5.0 V; $V_{CC(WD)}$ = 8 V; V_{GND} = 0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Read characteristics						
I_{MR}	MR current adjust range	R_{ext} = 10 kΩ; 0.5 mA steps	5	–	20.5	mA
ΔI_{MR}	tolerance (excluding R_{ext}) $\frac{I_{MR} - I_{MR(PR)}}{I_{MR(PR)}}$ with $I_{MR(PR)}$ = 10 mA		–	±4	–	%
$G_{v(dif)}$	differential voltage gain; note 1	from head inputs to RDx, RDy; R_{MR} = 28 Ω; I_{MR} = 10 mA; f = 20 MHz;				
		d4 = 0	–	160	–	
		d4 = 1	–	226	–	
$R_{i(dif)}$	differential input resistance	I_{MR} = 10 mA	–	13	–	Ω
$C_{i(dif)}$	differential input capacitance		–	16	–	pF
THD	total harmonic distortion		–	1	–	%
B_L	signal gain pass band edge; note 2	–3 dB	–	–	100	kHz
B_H	signal gain pass band edge without gain boost; note 2	–3 dB (4 nH lead inductance)	–	220	–	MHz
		–3 dB (50 nH lead inductance)	–	170	–	MHz
F	noise figure; note 3	R_{MR} = 28 Ω; I_{MR} = 10mA; T_{amb} = 25 °C; f = 20 MHz	–	3.0	3.2	dB
V_{nir}	input referred noise voltage; note 3	R_{MR} = 28 Ω; I_{MR} = 10mA; T_{amb} = 25 °C; f = 20 MHz	–	0.9	1.0	nV/√Hz
$f_{B(L)}$	+3 dB noise low corner frequency	R_{MR} = 28 Ω; I_{MR} = 10 mA; T_{amb} = 25 °C; no lead inductance	–		400	kHz
$f_{B(H)}$	+3 dB noise upper corner frequency	R_{MR} = 28 Ω; I_{MR} = 10 mA; T_{amb} = 25 °C; no lead inductance	–	220		MHz
α_{cs}	channel separation; note 4	unselected head	–	50		dB
PSRR	power supply rejection ratio; note 5	f < 1 MHz; I_{MR} = 10 mA	–	80		dB
		f < 100 MHz; I_{MR} = 10 mA	–	50		dB
CMRR	common mode rejection ratio; note 5	from nRx – nRy to RDx – RDy; R_{MR} mismatch < 5%; I_{MR} = 10 mA;				
		f < 1 MHz	–	45		dB
		f < 100 MHz	–	25		dB
DR	rejection of SCLK and SDATA; note 6	from SCLK, SDATA inputs to the RDx – RDy outputs; note 7	–	50		dB
$V_{O(R)(dif)}$	output DC offset voltage in read mode (differential after DC settling)	DC voltage between RDx – RDy (in read mode)	–	–	±0.2	V
$Z_{o(R)}$	output impedance in read mode	single ended	–	16	–	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{o(max)(dif)}$	maximum differential output current		–	4	–	mA
$V_{o(cm)}$	common mode output voltage in read mode	RDx, RDy	1.0	1.5	2.0	V
$\frac{\Delta V_{ocm}}{\Delta V_{CC}}$	common mode DC supply rejection in read mode		–	20	–	dB
$Z_{o(n)(dif)}$	differential output impedance in other modes (write, standby, sleep)		–	50	–	kΩ
Write characteristics						
I_{WR}	write current adjust range (in the write drivers)	R_{ext} = 10 kΩ; 1 mA steps	20	35	51	mA
ΔI_{WR}	tolerance (excluding R_{ext}); $\frac{I_{WR} - I_{RW(PR)}}{I_{RW(PR)}}$	$I_{WR(PR)}$ = 35 mA	–	±7	–	%
$V_{s(max)(p-p)}$	maximum voltage swing (peak-to-peak value)	$V_{CC(WD)}$ = 5 V	–	–	8	V
		$V_{CC(WD)}$ = 8 V (differential)	–	–	13	V
$R_{o(dif)}$	differential output resistance		–	200	–	Ω
t_r, t_f	write current rise/fall time without flip-flop (10% to 90%); note 8	$V_{CC(WD)}$ = 8 V; L_h = 150 nH, R_h = 10 Ω; I_{WR} = 35 mA; f = 20 MHz	–	–	1.8	ns
t_{as}	write current asymmetry; note 9	percentage of t_r/t_f (t_r, t_f and logic asymmetry)	–	–	5	%
t_{pd}	propagation delay 50% of (WDIx/WDIy) to 50% of (Wx, Wy)	write head short circuited; data flip-flop by passed	–	–	5	ns
α_{cs}	channel separation	unselected head	–	45	–	dB
Switching characteristics						
f_{SCLK}	serial interface clock rate		–	–	25	MHz
$\Delta V_{o(cm)}$	output common mode DC voltage change from Read to Write modes	I_{MR} = 10 mA; I_{WR} = 35 mA	–	200	–	mV
$t_{rec(W-R)}$	write to read recovery time (AC and DC settling); note 10	from 50% of the rising edge of R/$\overline{W}$ to steady state read-back signal: AC and DC settling at 90% (without load at RDx – RDy)				
		read amplifier OFF: d5 = 0	–	3	4.5	µs
		read amplifier ON: d5 = 1	–	100	150	µs
$t_{sw(R)}$	head switching (in read mode), standby to read active and MR current change recovery time; (AC and DC settling); note 11	from falling edge of SEN to steady state read-back signal; (without load at RDx – RDy)	–	3	4.5	µs
$t_{off(R)}$	read amplifier off time	from falling edge of R/$\overline{W}$ to read head inactive	–	–	50	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{st(W)}$	write settle times; note 12	from 50%of the falling edge of R/$\overline{W}$ to 90% of the steady state write current (in Write Mode)	–	–	70	ns
$t_{off(W)}$	write amplifier off time	from rising edge of R/$\overline{W}$ to I_{WR}-programmed /10 (I_{WR} = 35 mA)	–	–	50	ns
$t_{sw(W)}$	head switching (in write mode), and standby to write head active	from falling edge of SEN to write head active	–	50	70	ns
$t_{sw(S)}$	sleep to (and from) any other modes		–	–	100	µs
DC characteristics						
$I_{CC(R)}$	supply current; note 13	read mode; I_{MR} = 10 mA	–	72	80	mA
$I_{CC(W)}$	supply current; note 14	write mode; I_{WR} = 35 mA				
		from V_{CC} (5 V)	–	33	41	mA
		from $V_{CC(WD)}$ (5 to 8 V)	–	54	61	mA
$I_{DD(stb)}$	standby mode supply current		–	0.25	1	mA
$I_{DD(S)}$	sleep mode supply current	static	–	0.025	–	mA
V_{ref}	reference voltage for R_{ext}		–	1.32	–	V

Notes to the characteristics

1. The differential voltage gain depends on the MR resistance. It can be improved by programming the d4 bit in the configuration register using the serial interface.
2. The gain boost implements a pole-zero combination: The +3 dB gain boost corner frequency is

   $$\frac{800\ \text{MHz}}{(8 \cdot d3 + 4 \cdot d2 + 2 \cdot d1 + 1 \cdot d0)}$$

   The –3 dB gain attenuation corner frequency is

   $$\frac{800\ \text{MHz}}{(8 \cdot d3 + 4 \cdot d2 + 2 \cdot d1 + 1 \cdot d0)}$$

   where d3, d2, d1, d0 are bits (0, 1) to be programmed via the Serial Interface. In practical use, the bandwidth is limited by the inductance of the connection between the MR heads and the pre-amplifier.
3. **Noise calculation**

   a) **Definitions:** The amplifier has a low-ohmic input. No lead resistance is taken into account. The input referred noise voltage, excluding the noise of the MR resistors, is defined as follows:

   $$V_{nir}^{\ 2} = \left(\frac{V_{no}}{G_v}\right)^2 - 4kT \times (R_{MR1} + R_{MR2})\ \text{V}$$

   where G_v is the voltage gain and V_{no} is the noise voltage at the output of the amplifier, k is the Boltzmann constant and T is the temperature in K. The noise figure is defined as follows:

   $$F = 10 \times \left(\log \frac{\left(\frac{V_{no}}{G_v}\right)^2}{4kT \times (R_{MR1} + R_{MR2})} \right) \text{dB}$$

   in 1 Hz bandwidth. Note that R_{MR} includes all resistances between Rx or Ry to ground.

   b) **Noise figure versus I_{MR} and R_{MR}:** Table 1 shows the variation of the noise figure with I_{MR} (mA) and R_{MR} (Ω).

   c) **Input noise voltage consideration:** the input referred noise voltage calculation can significantly be different (from 1.0 to 0.44 nV/√Hz for instance) by taking into account an equivalent signal-to-noise ratio when using two MR stripes (28 Ω for each stripe) or one MR stripes (42 W). It assumes that the signal coming from the head is larger for a dual stripe head than for a single stripe head (50% extra signal for dual stripe head).
4. The channel separation is defined by the ratio of the gain response of the amplifier using the selected head H(n) to the gain response of the amplifier using the adjacent head H(n ±1), Head H(n) being selected.

5. The PSRR (in dB) is defined as input referred ratio:

   $$PSRR = 20 \times \log\left(\frac{G_v}{G_p}\right)$$

   Where G_v is the differential input to differential output gain, and G_p is the power supply to differential output gain. The CMRR (in dB) is defined as input referred ratio: $CMRR = 20 \times \log\left(\frac{G_v}{G_{cm}}\right)$

   where G_v is the differential input to differential output gain and G_{cm} is the common mode input to differential output gain. Flex and board lay-out may affect significantly these parameters.
6. This refers to the crosstalk from SCLK and SDATA inputs via the read inputs to RDx – RDy. Two cases can be distinguished:
   a) With SEN LOW, SCLK and SDATA are prohibited from entering the device and crosstalk is low.
   b) Programming via the serial interface is done with SEN HIGH. Then crosstalk can occur. A careful design of the board or flex-foil is required in order not to get crosstalk via this path.
7. A 200 mV peak-to-peak signal is applied to SCLK or SDATA inputs at 25 MHz, and measurement is performed at RDx – RDy.
8. The rise and fall times depend on the write amplifier-write head combination. L_h and R_h represent the components on the evaluation board. Parasitic capacitances also limit the performance.
9. The write current rise/fall time asymmetry is defined by $\frac{|t_r - t_f|}{2\,(t_r + t_f)}$
10. Write-to-read recovery time includes the write mode to read mode switching using the R/$\overline{W}$ pin on the same head (see Fig.6). The AC signal reaches its full amplitude few tenth of ns after appearing at the reader RDx and RDy outputs.
11. In read mode, the head switching, standby to read active switching and changing MR current include fast current settling (see Fig.7). Same note regarding the AC signals at the reader outputs as above.
12. Write settle time includes read mode to write mode switching using the R/$\overline{W}$ pin.
13. The typical supply current in read mode depends on the bias current for the MR element.
14. The typical supply current in write mode also depends on the write current.

Table 1 Noise figure

R_{MR} (Ω)	F (dB)		
	I_{MR} = 7 mA	I_{MR} = 10 mA	I_{MR} = 15 mA
20	2.7	2.9	3.1
25	2.8	3.0	3.3
30	2.9	3.1	3.5

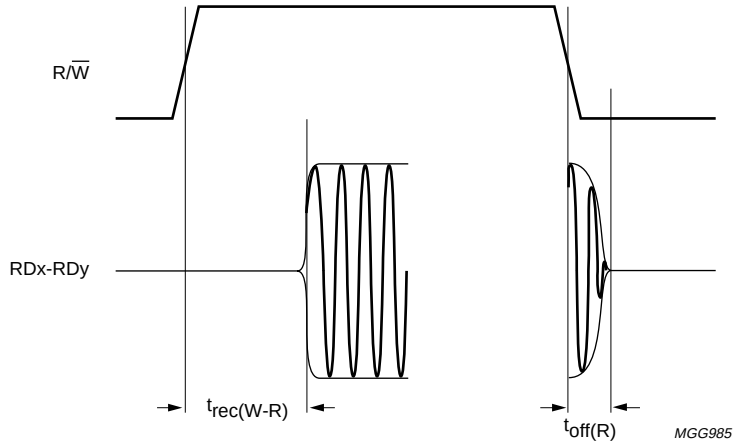


Fig.6 Timing diagram of the reader: write-to-read switching on the same logic head.

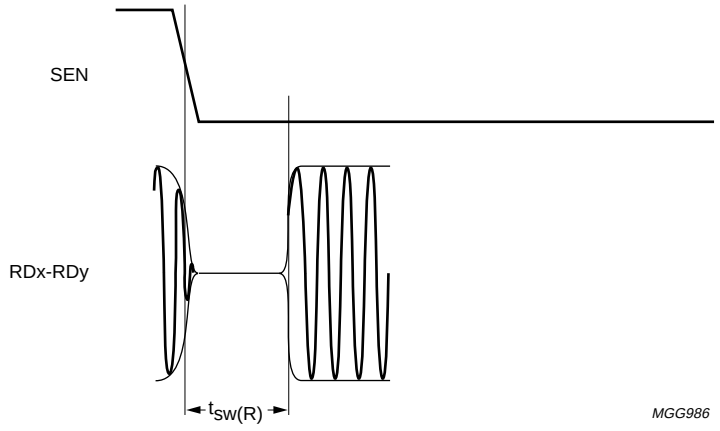
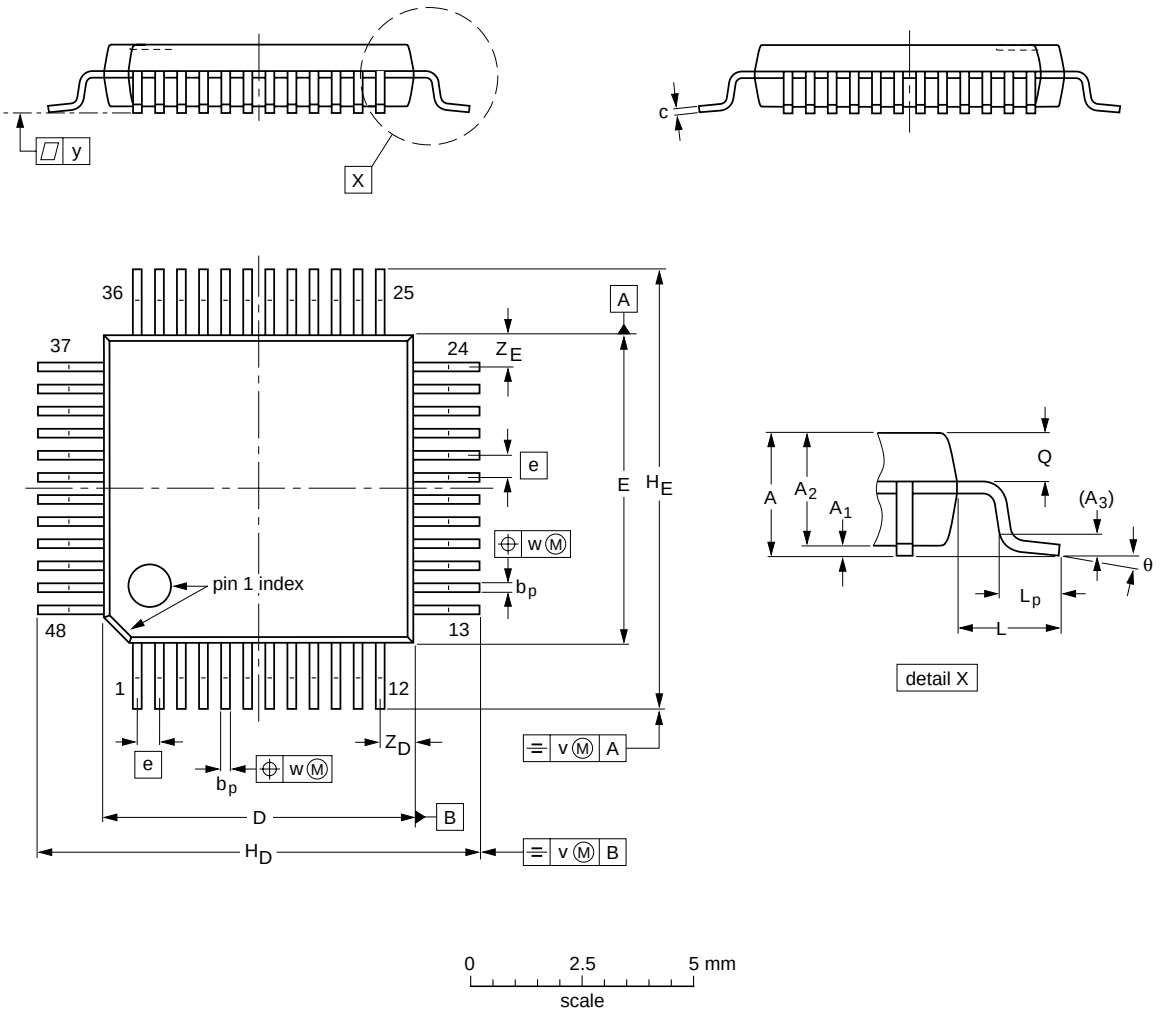


Fig.7 Timing diagram of the reader: typical head, current and standby-to-read characteristics.

14 PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~93-06-15~~ 94-12-19

15 SOLDERING

15.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

15.2 Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

15.3 Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

16 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

17 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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