DATA SHEET

TDA8718
8-bit high-speed analog-to-digital converter

Product specification
Supersedes data of April 1993
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

8-bit high-speed analog-to-digital converter TDA8718

FEATURES

- 8-bit resolution
- Sampling rate up to 600 MHz
- ECL (100K family) compatible for digital inputs and outputs
- Overflow/Underflow output
- 50 Ω load drive capability
- Low input capacitance (5 pF typ.).

GENERAL DESCRIPTION

The TDA8718 is an 8-bit analog-to-digital converter (ADC) designed for professional applications. The device converts the analog input signal into 8-bit binary coded digital words at a sampling rate of 600 MHz. It has an effective bandwidth capability up to 150 MHz full-scale sine wave. All digital outputs are ECL compatible.

APPLICATIONS

- High speed analog-to-digital conversion
- Industrial instrumentation
- Data communication
- RF communication.

QUICK REFERENCE DATA

Measured over full voltage and temperature ranges, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		–4.2	–4.5	–4.8	V
V_{EED}	digital supply voltage		–4.2	–4.5	–4.8	V
I_{ref}	resistive ladder current	R = 48 Ω	30	45	60	mA
I_{EEA}	analog supply current		30	42	54	mA
I_{EED}	digital supply current		100	120	150	mA
$I_{EEO(L)}$	LOW level output supply current	R_L = 50 Ω	40	70	90	mA
$I_{EEO(H)}$	HIGH level output supply current	R_L = 50 Ω	155	170	185	mA
ILE	DC integral linearity error		–	±0.7	±1.0	LSB
DLE	DC differential linearity error		–	±0.3	±0.5	LSB
EB	effective bits	f_i = 4.43 MHz; I_{ref} = 45 mA; f_{clk} = 100 MHz	–	7.5	–	bits
		f_i = 4.43 MHz; I_{ref} = 45 mA; f_{clk} = 100 MHz	–	6.5	–	bits
$f_{clk(max)}$	maximum clock frequency		600	–	–	MHz
P_{tot}	total power dissipation		–	990	1250	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8718K	28	PLCC28	plastic	SOT261-2

BLOCK DIAGRAM

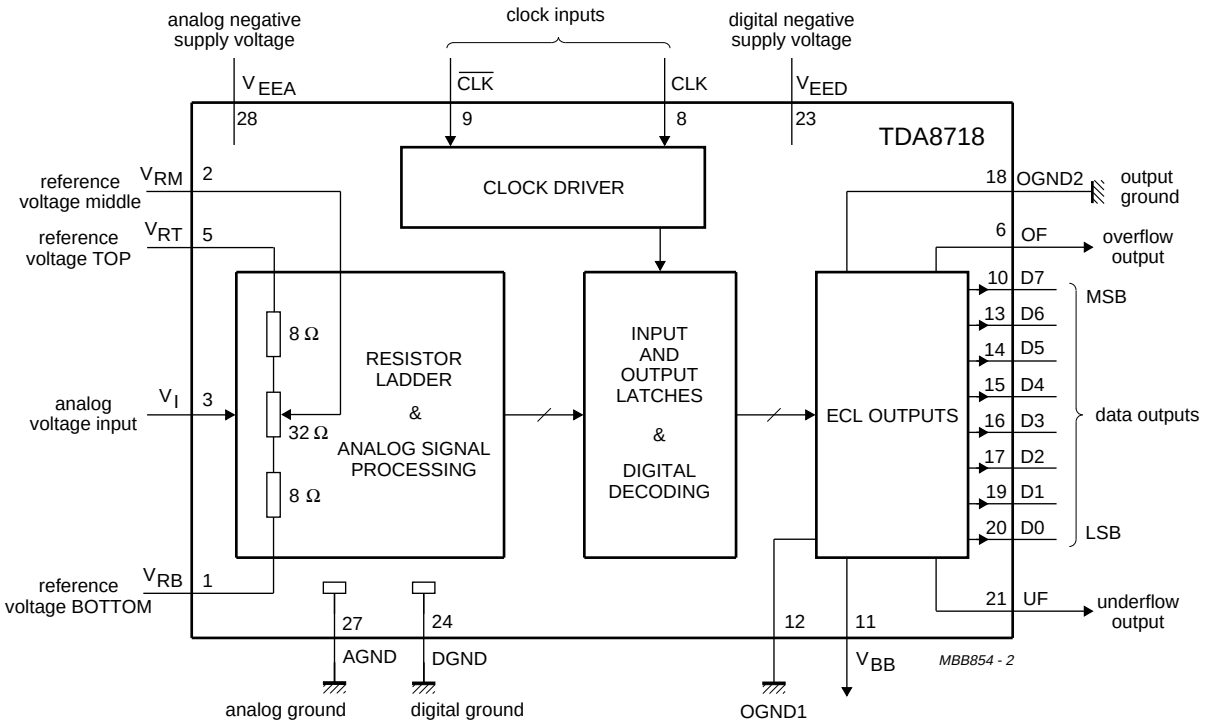


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{RB}	1	reference voltage BOTTOM
V_{RM}	2	reference voltage MIDDLE decoupling
V_I	3	analog input voltage
n.c.	4	not connected
V_{RT}	5	reference voltage TOP
OF	6	overflow digital output
n.c.	7	not connected
CLK	8	clock input
$\overline{CLK}$	9	complementary clock input
D7	10	digital output; bit 7 (MSB)
V_{BB}	11	ECL reference voltage
OGND1	12	output ground 1 (0 V)
D6	13	digital output; bit 6
D5	14	digital output; bit 5
D4	15	digital output; bit 4
D3	16	digital output; bit 3
D2	17	digital output; bit 2
OGND2	18	output ground 2 (0 V)
D1	19	digital output; bit 1
D0	20	digital output; bit 0 (LSB)
UF	21	underflow digital output
n.c.	22	not connected
V_{EED}	23	digital supply voltage (–4.5 V)
DGND	24	digital ground
n.c.	25	not connected
n.c.	26	not connected
AGND	27	analog ground
V_{EEA}	28	analog supply voltage (–4.5 V)

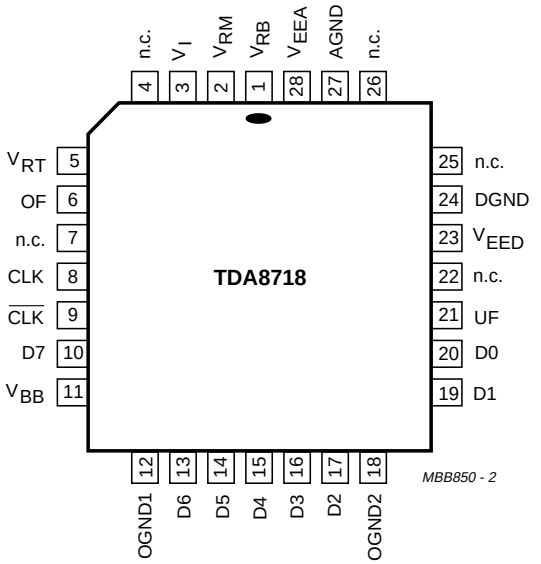


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

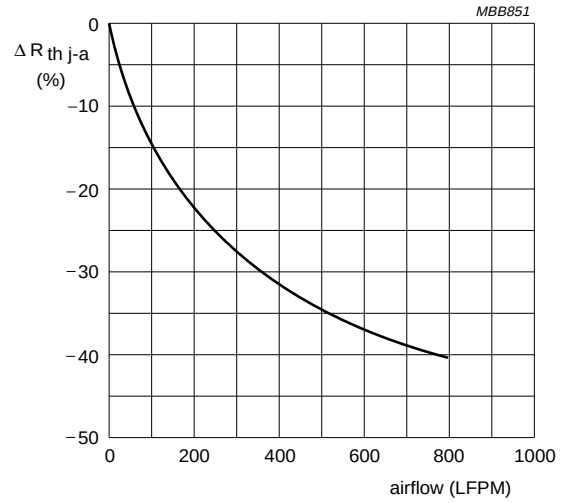
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EEA}	analog supply voltage (pin 28)		–7.0	+0.3	V
V_{EED}	digital supply voltage (pin 23)		–7.0	+0.3	V
ΔV_{EE}	supply voltage difference between V_{EEA} and V_{EED}		–1.00	+1.0	V
V_I	input voltage (pin 3)	referenced to AGND	V_{EEA}	0	V
$\Delta V_{clk(p-p)}$	clock input voltage difference between CLK and $\overline{CLK}$ pin 8 to pin 9 (peak-to-peak value)	referenced to V_{EED}; note 1	–	2.0	V
I_O	output current for each digital output		–	30	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		–	+150	°C

Note

1. The circuit has two clock inputs CLK and $\overline{CLK}$. Sampling takes place on the falling edge of the clock input signal; CLK and $\overline{CLK}$ are two complementary signals.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	55	K/W



Test conditions: PCB (2.24 × 2.24 × 0.062 inches).
LFPM = Linear Foot Per Minute.

Fig.3 Average effect of air flow on $R_{th\ j\text{-}a}$.

CHARACTERISTICS

V_{EEA} = –4.2 to –4.8 V; V_{EED} = –4.2 to –4.8 V; V_{EEA} to V_{EED} = –0.1 to +0.1 V; AGND and DGND shorted together; T_{amb} = 0 to +70 °C; typical values measured at V_{EEA} = –4.5 V, V_{EED} = –4.5 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{EEA}	analog supply voltage (pin 28)		–4.2	–4.5	–4.8	V
V_{EED}	digital supply voltage (pin 23)		–4.2	–4.5	–4.8	V
I_{EEA}	analog supply current (pin 28)		30	42	54	mA
I_{EED}	digital supply current (pin 23)		100	120	150	mA
$I_{EEO(L)}$	LOW level output supply current	R_L = 50 Ω	40	70	90	mA
$I_{EEO(H)}$	HIGH level output supply current	R_L = 50 Ω	155	170	185	mA
Reference voltages for the resistor ladder (see Table 1)						
I_{RT}	reference current (pin 5)	R = 48 Ω	30	45	60	mA
V_{RB}	reference voltage BOTTOM (pin 1)		–	48 Ω × I_{RT}	–	V
V_{RT}	reference voltage TOP (pin 5)		–	0	–	V
R_{LAD}	resistor ladder		–	48	–	Ω
TC_{RLAD}	temperature coefficient of the resistor ladder		–	175	–	MΩ/K
V_{osB}	voltage offset BOTTOM	note 1	–	8 Ω × I_{RT}	–	mV
V_{osT}	voltage offset TOP	note 1	–	8 Ω × I_{RT}	–	mV
Inputs						
CLK INPUT (PIN 8); $\overline{\text{CLK}}$ INPUT (PIN 9)						
V_{IL}	LOW level input voltage		–	–1.8	–	V
V_{IH}	HIGH level input voltage		–	–0.8	–	V
I_{IL}	LOW level input current	V_{clk} = –1.8 V	–	0	–	µA
I_{IH}	HIGH level input current	V_{clk} = –0.8 V	–	120	–	µA
R_I	input resistance	f_{clk} = 100 MHz	–	1.5	–	kΩ
C_I	input capacitance	f_{clk} = 100 MHz	–	3.5	–	pF
$\Delta V_{clk(p-p)}$	clock input voltage difference between CLK and $\overline{\text{CLK}}$ pin 8 to pin 9 (peak-to-peak value)		–	900	–	mV
ANALOG INPUT (PIN 3); NOTE 2						
I_{IL}	LOW level input current	data output = 00	20	40	80	µA
I_{IH}	HIGH level input current	data output = FF	100	200	400	µA
R_I	input resistance		–	10	–	kΩ
C_I	input capacitance		–	5	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs (R_L = 50 Ω)						
DIGITAL 100K ECL OUTPUTS (D0 TO D7; OF; UF)						
V_{OL}	LOW level output voltage	Tamb = 25 °C	–	–1770	–1650	mV
V_{OH}	HIGH level output voltage	Tamb = 25 °C	–1300	–1150	–	mV
V_{ECL}	ECL reference voltage		–1550	–1450	–1350	mV
I_{OL}	LOW level output current		4	6	8	mA
I_{OH}	HIGH level output current		10	20	25	mA
Switching characteristics						
$f_{clk(max)}$	maximum clock frequency (pins 8 and 9)		600	–	–	MHz
t_r; t_f	rise and fall times	f_i = 100 MHz	–	–	750	ps
Analog signal processing (f_{clk} = 500 MHz)						
HARMONICS (FULL SCALE)						
h_1	fundamental harmonics	f_i = 100 MHz	–	0	–	dB
h_2	second harmonics	f_i = 100 MHz	–	–54	–	dB
h_3	third harmonics	f_i = 100 MHz	–	–50	–	dB
Transfer function						
ILE	DC integral linearity error		–	±0.7	±1.0	LSB
DLE	DC differential linearity error		–	±0.3	±0.5	LSB
AILE	AC integral linearity error	note 3	–	±0.9	±1.5	LSB
EB	effective bits	f_i = 4.43 MHz, full scale; I_{ref} = 45 mA; note 4; f_{clk} = 100 MHz; Fig.5	–	7.5	–	bits
		f_i = 100 MHz, full scale; I_{ref} = 45 mA; note 4; f_{clk} = 500 MHz; Fig.6	–	6.5	–	bits
BER	bit error rate	f_{clk} = 500 MHz; f_i = 100 MHz; V_i = ±8 LSB at code 128; 50% clock duty cycle	–	10^{-11}	–	times/ samples
Timing (f_{clk} = 500 MHz; R_L = 50 Ω; C_L = 5 pF) note 5						
t_{ds}	sampling delay		–	–	300	ps
t_h	output hold time		400	700	–	ps
t_d	output delay time		–	1300	1500	ps

Notes to the "Characteristics"

1. Voltage offset BOTTOM (V_{osB}) is the difference between the analog input which produces data outputs equal to 00 and the reference voltage BOTTOM (V_{RB}) at T_{amb} = 25 °C. Voltage offset TOP (V_{osT}) is the difference between reference voltage TOP (V_{RT}) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C.
2. The analog input is not internally biased. It should be externally biased between V_{RT} and V_{RB} levels.
3. Full-scale sine wave; f_i = 4.43 MHz; f_{clk} = 100 MHz.
4. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 4K acquisition points per period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency).

   Conversion to signal-to-noise ratio: S/N = EB × 6.02 + 1.76 dB.
5. TDA8718 can only withstand one or two 100K ECL loads in order to work out timings at the maximum sampling frequency. It is recommended to minimize the printed circuit-board load by implementing the load device as close as possible to the TDA8718.

Table 1 Output coding and input voltage (typical values; referenced to AGND.

STEP	V_I	O/UF	BINARY OUTPUT BITS					
			D5	D4	D3	D2	D1	D0
Underflow	$< -40\ \Omega \times I_{RT}$	1	0	0	0	0	0	0
0	$-40\ \Omega \times I_{RT}$	0	0	0	0	0	0	0
1	.	0	0	0	0	0	0	1
.	.	.	.		.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	.	0	1	1	1	1	1	0
255	$-8\ \Omega \times I_{RT}$	0	1	1	1	1	1	1
Overflow	$> -8\ \Omega \times I_{RT}$	1	1	1	1	1	1	1

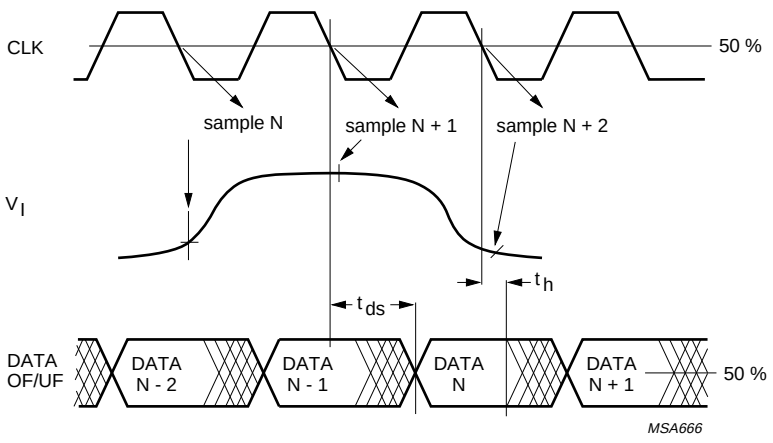
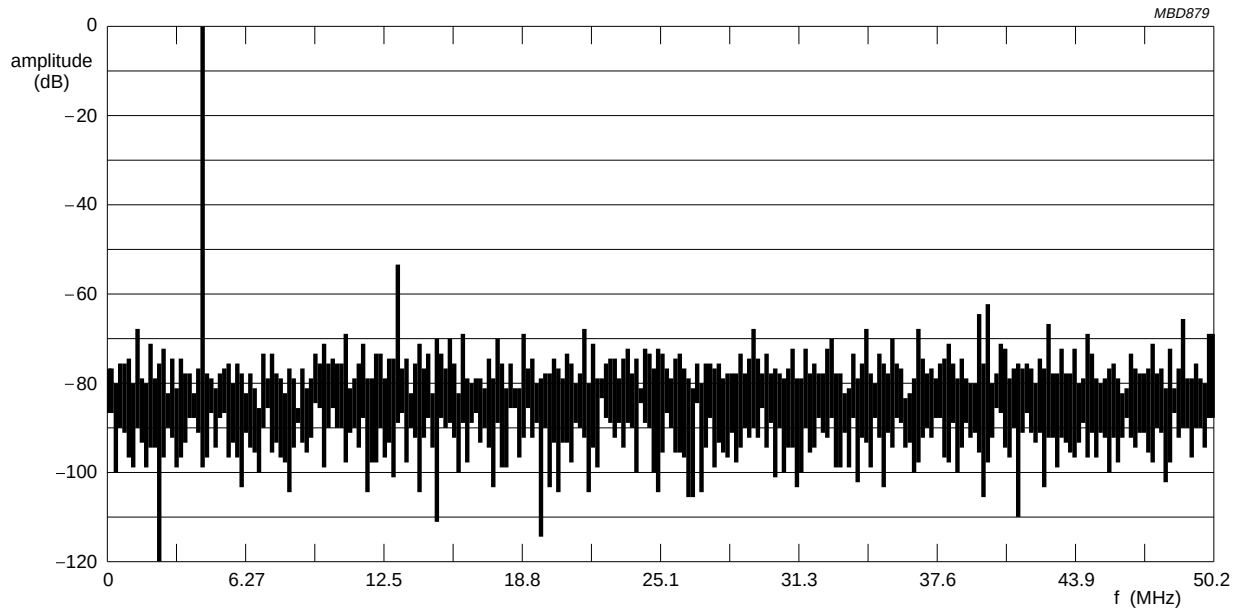


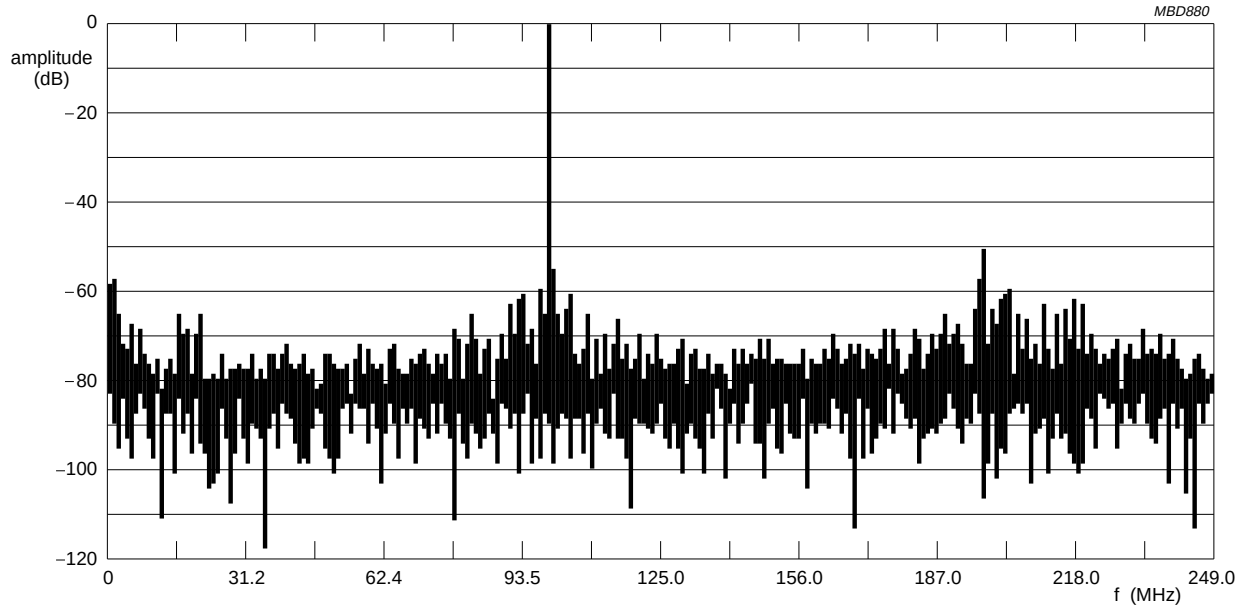
Fig.4 Timing diagram.



Effective bits: 7.53; THD = −54.56 dB.

Harmonic levels (dB): 2nd = −77.28; 3rd = −54.76; 4th = −71.43; 5th = −71.85; 6th = −105.50.

Fig.5 Fast Fourier Transform (f_{clk} = 100 MHz; f_i = 4.43 MHz).



Effective bits: 6.60; THD = −48.60 dB.

Harmonic levels (dB): 2nd = −64.81; 3rd = −51.10; 4th = −65.05; 5th = −58.33; 6th = −54.07.

Fig.6 Fast Fourier Transform (f_{clk} = 500 MHz; f_i = 100 MHz).

APPLICATION INFORMATION

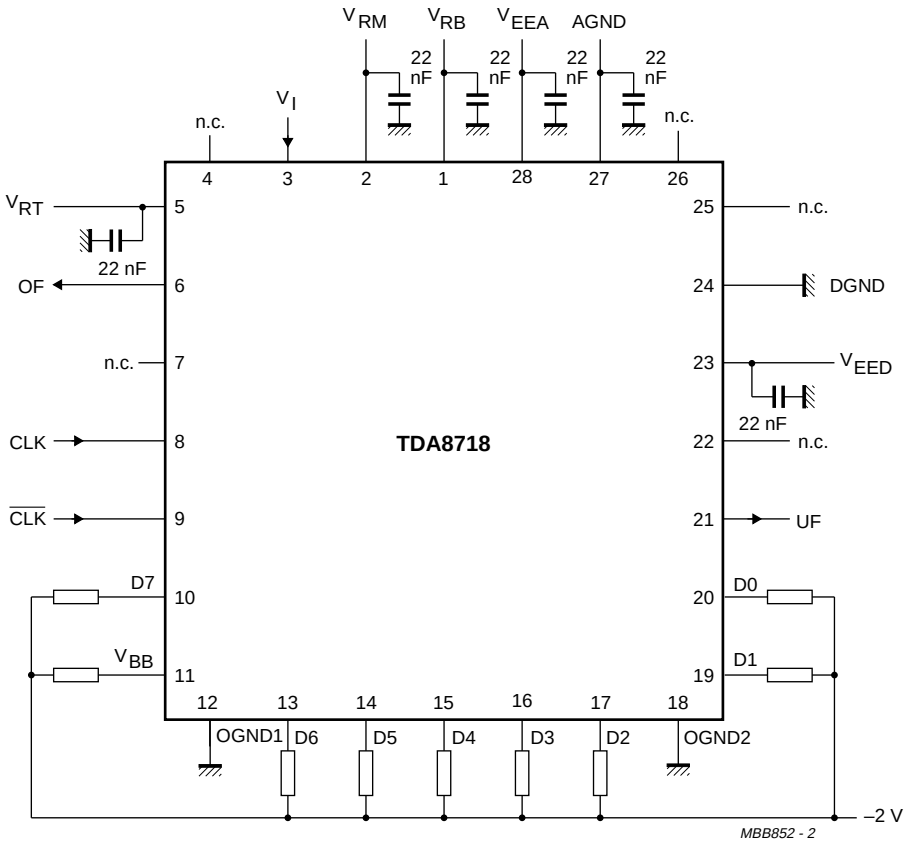
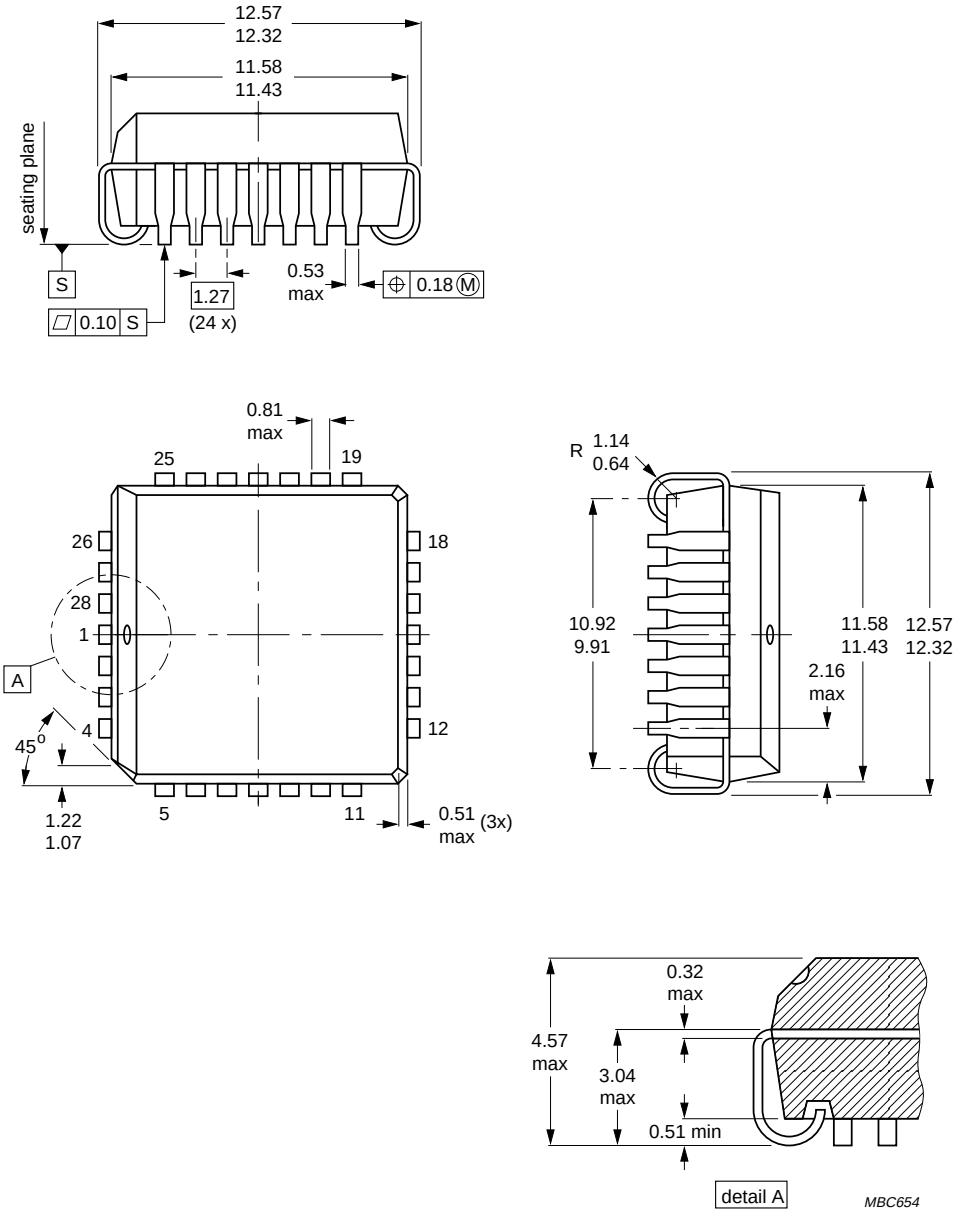


Fig.7 Application diagram.

PACKAGE OUTLINE



Dimensions in mm.

Fig.8 Plastic leaded chip carrier, 28-leads; SOT261-2.

SOLDERING

Plastic leaded chip carriers

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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