



## RAD-TOLERANT CLASS V, WIDEBAND, FULLY DIFFERENTIAL AMPLIFIER

### FEATURES

- Fully Differential Architecture
- Common-Mode Input Range Includes Negative Rail
- Minimum Gain of 2 V/V (6 dB)
- Bandwidth: 1.1 GHz (Gain = 6 dB)
- Slew Rate: 5100 V/ $\mu$ s
- 1% Settling Time: 5.5 ns
- HD<sub>2</sub>: -76 dBc at 70 MHz
- HD<sub>3</sub>: -88 dBc at 70 MHz
- OIP<sub>2</sub>: 84 dBm at 70 MHz
- OIP<sub>3</sub>: 42 dBm at 70 MHz
- Input Voltage Noise: 2 nV/ $\sqrt{\text{Hz}}$  (f > 10 MHz)
- Noise Figure: 21.8 dB (50  $\Omega$  System, G = 6 dB)
- Output Common-Mode Control
- 5 V Power Supply Current: 39.2 mA
- Power-Down Capability: 0.65 mA
- Rad-Tolerant: 150 kRad (Si) TID
- QML-V Qualified, SMD 5962-07222

### APPLICATIONS

- 5 V Data-Acquisition Systems
- High Linearity ADC Amplifier
- Wireless Communication
- Medical Imaging
- Test and Measurement

### RELATED PRODUCTS

DEVICE	MINIMUM GAIN	COMMON-MODE RANGE OF INPUT <sup>(1)</sup>
THS4511-SP	6 dB	-0.3 V to 2.3 V
THS4513-SP	6 dB	0.75 V to 4.25 V

(1) Assumes a 5 V single-ended power supply

### DESCRIPTION/ORDERING INFORMATION

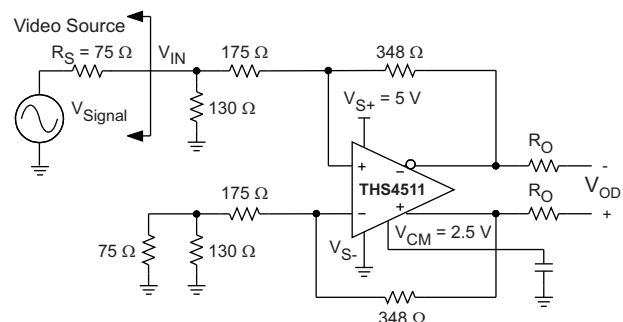
The THS4511 is a fully differential operational amplifier designed for single-supply 5 V data-acquisition systems. It has very low noise at 2 nV/ $\sqrt{\text{Hz}}$ , and extremely low harmonic distortion of -76 dBc HD<sub>2</sub> and -88 dBc HD<sub>3</sub> at 70 MHz with 2 V<sub>pp</sub>, G = 14 dB, and 100  $\Omega$  load. Slew rate is very high at 5100 V/ $\mu$ s and with settling time of 5.5 ns to 1% (2 V step) it is ideal for pulsed applications. It is designed for minimum gain of 6 dB.

To allow for dc coupling to ADCs, its unique output common-mode control circuit maintains the output common-mode voltage within 5 mV offset (typical) from the set voltage, when set within  $\pm 0.5$  V of mid-supply. The common-mode set point is set to mid-supply by internal circuitry, which may be over-driven from an external source.

The THS4511 is a high-performance amplifier that has been optimized for use in 5 V single-supply data acquisition systems. The output has been optimized for best performance with its common-mode voltages set to mid-supply, and the input has been optimized for performance over a wide range of common-mode input voltages. High performance at a low power-supply voltage enables single-supply 5 V data-acquisition systems while minimizing component count.

The THS4511 is offered in a 16-pin ceramic flatpack package (W), and is characterized for operation over the full military temperature range from -55°C to 125°C.

### Video Buffer, Single Ended to Differential



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### PACKAGING/ORDERING INFORMATION<sup>(1)</sup>

TEMPERATURE	PACKAGED DEVICES	
	CERAMIC FLATPACK W (16) <sup>(2)</sup>	SYMBOL
-55°C to 125°C	5962-0722201VFA	5962-0722201VFA

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).  
 (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		UNIT
$V_{S-}$ to $V_{S+}$	Supply voltage	6 V
$V_I$	Input voltage	$\pm V_S$
$V_{ID}$	Differential input voltage	4 V
$I_O$	Output current	200 mA
Continuous power dissipation		See Dissipation Rating Table
$T_J$	Maximum junction temperature <sup>(2)</sup>	150°C
$T_A$	Operating free-air temperature range	-55°C to 125°C
$T_{stg}$	Storage temperature range	-65°C to 150°C
ESD ratings	HBM	2000 V
	CDM	1500 V
	MM	100 V

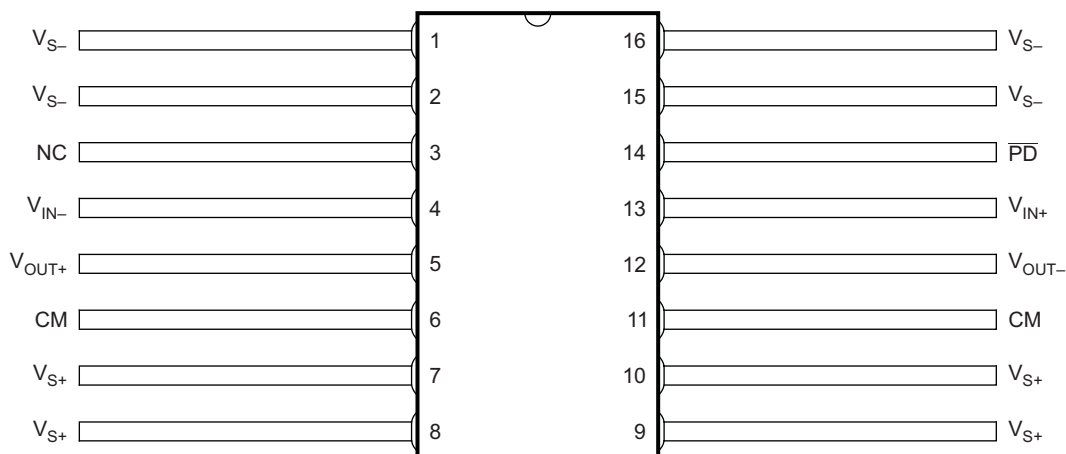
- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.  
 (2) The absolute maximum temperature under any condition is limited by the constraints of the silicon process.

### DISSIPATION RATINGS TABLE

PACKAGE	$\theta_{JC}$	$\theta_{JA}$	POWER RATING	
			$T_A \leq 25^\circ\text{C}$	$T_A = 125^\circ\text{C}$
W (16)	14.7°C/W	189°C/W	661 mW	132 mW

## DEVICE INFORMATION

**W PACKAGE  
TOP VIEW**



## TERMINAL FUNCTIONS

TERMINAL (W PACKAGE)		DESCRIPTION
NO.	NAME	
3	NC	No internal connection
4	V <sub>IN-</sub>	Inverting amplifier input
5	V <sub>OUT+</sub>	Non-inverting amplifier output
6, 11	CM	Common-mode voltage input
7, 8, 9, 10	V <sub>S+</sub>	Positive amplifier power supply input
12	V <sub>OUT-</sub>	Inverting amplifier output
13	V <sub>IN+</sub>	Non-inverting amplifier input
14	$\overline{\text{PD}}$	Powerdown, $\overline{\text{PD}}$ = logic low puts part into low power mode, $\overline{\text{PD}}$ = logic high or open for normal operation
1, 2, 15, 16	V <sub>S-</sub>	Negative amplifier power supply input

**ELECTRICAL CHARACTERISTICS;  $V_{S+} - V_{S-} = 5\text{ V}$  (Unchanged after 150 kRad):**

Test conditions unless otherwise noted:  $V_{S+} = 5\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $G = 14\text{ dB}$ ,  $CM = \text{open}$ ,  $V_{OD} = 2\text{ Vpp}$ ,  $R_F = 348\ \Omega$ ,  $R_L = 200\ \Omega$  Differential,  $T_A = 25^\circ\text{C}$ , Single-Ended Input, Differential Output, Input Referenced to Ground, and Output Referenced to Mid-Supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>AC PERFORMANCE</b>					
Small-Signal Bandwidth	$G = 6\text{ dB}$ , $V_O = 100\text{ mVpp}$		1.1		GHz
	$G = 10\text{ dB}$ , $V_O = 100\text{ mVpp}$		1.0		
	$G = 14\text{ dB}$ , $V_O = 100\text{ mVpp}$		720		MHz
Gain-Bandwidth Product	$G = 10\text{ dB}$		3		GHz
Bandwidth for 0.1 dB flatness	$G = 10\text{ dB}$ , $V_O = 2\text{ Vpp}$		65		MHz
	$G = 14\text{ dB}$ , $V_O = 2\text{ Vpp}$		115		
Large-Signal Bandwidth	$G = 6\text{ dB}$ , $V_O = 2\text{ Vpp}$		1.1		GHz
Slew Rate (Differential)			5100		V/ $\mu\text{s}$
Rise Time	$V_O = 2\text{ V Step}$		0.5		ns
Fall Time			0.5		ns
Settling Time to 1%			5.5		ns
2 <sup>nd</sup> Order Harmonic Distortion	$f = 10\text{ MHz}$ , $R_L = 100\ \Omega$		-106		dBc
	$f = 50\text{ MHz}$ , $R_L = 100\ \Omega$		-90		
	$f = 100\text{ MHz}$ , $R_L = 100\ \Omega$		-87		
3 <sup>rd</sup> Order Harmonic Distortion	$f = 10\text{ MHz}$ , $R_L = 100\ \Omega$		-108		
	$f = 50\text{ MHz}$ , $R_L = 100\ \Omega$		-106		
	$f = 100\text{ MHz}$ , $R_L = 100\ \Omega$		-83		
2 <sup>nd</sup> Order Intermodulation Distortion	200 kHz tone spacing, $R_L = 100\ \Omega$	$f_C = 50\text{ MHz}$	-83		dBc
		$f_C = 100\text{ MHz}$	-75		
3 <sup>rd</sup> Order Intermodulation Distortion		$f_C = 50\text{ MHz}$	-83		
		$f_C = 100\text{ MHz}$	-74		
2 <sup>nd</sup> Order Output Intercept Point	200 kHz tone spacing, $R_L = 100\ \Omega$	$f_C = 50\text{ MHz}$	84		dBm
		$f_C = 100\text{ MHz}$	77		
3 <sup>rd</sup> Order Output Intercept Point		$f_C = 50\text{ MHz}$	42		
		$f_C = 100\text{ MHz}$	38		
Noise Figure	50 $\Omega$ system, 10 MHz		21.8		dB
Input Voltage Noise	$f > 10\text{ MHz}$		2		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f > 10\text{ MHz}$		1.5		pA/ $\sqrt{\text{Hz}}$
<b>DC PERFORMANCE</b>					
Open-Loop Voltage Gain ( $A_{OL}$ )			63		dB
Input Offset Voltage	$T_A = 25^\circ\text{C}$		1	4	mV
	$T_A = -55^\circ\text{C to } 125^\circ\text{C}$			5.5	
Average Offset Voltage Drift			2.3		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$T_A = 25^\circ\text{C}$		8	15.5	$\mu\text{A}$
	$T_A = -55^\circ\text{C to } 125^\circ\text{C}$			20	
Average Bias Current Drift			20		nA/ $^\circ\text{C}$
Input Offset Current	$T_A = 25^\circ\text{C}$		0.5	3.6	$\mu\text{A}$
	$T_A = -55^\circ\text{C to } 125^\circ\text{C}$			7	
Average Offset Current Drift			7		nA/ $^\circ\text{C}$

**ELECTRICAL CHARACTERISTICS;  $V_{S+} - V_{S-} = 5\text{ V}$  (Unchanged after 150 kRad): (continued)**

Test conditions unless otherwise noted:  $V_{S+} = 5\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $G = 14\text{ dB}$ ,  $CM = \text{open}$ ,  $V_{OD} = 2\text{ V}_{pp}$ ,  $R_F = 348\ \Omega$ ,  $R_L = 200\ \Omega$  Differential,  $T_A = 25^\circ\text{C}$ , Single-Ended Input, Differential Output, Input Referenced to Ground, and Output Referenced to Mid-Supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
<b>INPUT</b>						
Common-Mode Input Range High			2.3		V	
Common-Mode Input Range Low			-0.3			
Common-Mode Rejection Ratio			80		dB	
Differential Input Impedance			18.2    0.5		M $\Omega$    pF	
Common-Mode Input Impedance			4.0    1.5			
<b>OUTPUT</b>						
Maximum Output Voltage High	Each output with 100 $\Omega$ to mid-supply	$T_A = 25^\circ\text{C}$	3.7	3.8	V	
		$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	3.5			
Minimum Output Voltage Low		$T_A = 25^\circ\text{C}$		1.2		1.3
		$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$				1.5
Differential Output Voltage Swing	$T_A = 25^\circ\text{C}$	4.8	5.2		V	
	$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	4.0				
Differential Output Current Drive	$R_L = 10\ \Omega$		96		mA	
Output Balance Error	$V_O = 100\text{ mV}$ , $f = 1\text{ MHz}$		-52		dB	
Closed-Loop Output Impedance	$f = 1\text{ MHz}$		0.3		$\Omega$	
<b>OUTPUT COMMON-MODE VOLTAGE CONTROL</b>						
Small-Signal Bandwidth			250		MHz	
Slew Rate			110		V/ $\mu\text{s}$	
Gain			1		V/V	
Output Common-Mode Offset from CM input	$1.5\text{ V} < CM < 3.5\text{ V}$		5		mV	
CM Input Bias Current	$1.5\text{ V} < CM < 3.5\text{ V}$		$\pm 40$		$\mu\text{A}$	
CM Input Voltage Range			1.25 to 3.75		V	
CM Input Impedance			32    2.8		k $\Omega$    pF	
CM Default Voltage	CM pins floating		2.5		V	
<b>POWER SUPPLY</b>						
Specified Operating Voltage		3.75 <sup>(1)</sup>	5	5.25	V	
Maximum Quiescent Current	$T_A = 25^\circ\text{C}$		39.2	42.5	mA	
	$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$			44		
Minimum Quiescent Current	$T_A = 25^\circ\text{C}$	35.9	39.2			
	$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	34				
Power Supply Rejection ( $\pm\text{PSRR}$ )	To differential output		90		dB	
<b>POWER DOWN</b>						
Enable Voltage Threshold	Device assured on above 2.1 V		> 2.1		V	
Disable Voltage Threshold	Device assured off below 0.7 V		< 0.7			
Powerdown Quiescent Current	$T_A = 25^\circ\text{C}$		0.65	0.9	mA	
	$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$			1.2		
Input Bias Current	$\overline{PD} = V_{S-}$		100		$\mu\text{A}$	
Input Impedance			50    2		k $\Omega$    pF	
Turn-On Time Delay	Measured to output on		55		ns	
Turn-Off Time Delay	Measured to output off		10		$\mu\text{s}$	

(1) See the *Application Information* section of this data sheet for device operation with full supply voltages less than 5 V.

**TYPICAL CHARACTERISTICS**

**TYPICAL AC PERFORMANCE:  $V_{S+} - V_{S-} = 5\text{ V}$**

Test conditions unless otherwise noted:  $V_{S+} = 5\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $G = 14\text{ dB}$ ,  $CM = \text{open}$ ,  $V_{OD} = 2\text{ V}_{PP}$ ,  $R_F = 348\ \Omega$ ,  $R_L = 200\ \Omega$   
Differential, Single-Ended Input, Input Referenced to Ground and Output Referenced to Mid-Rail

Small-Signal Frequency Response	G = 6 dB, $V_{OD} = 100\text{ mV}_{PP}$		<a href="#">Figure 1</a>
	G = 10 dB, $V_{OD} = 100\text{ mV}_{PP}$		<a href="#">Figure 2</a>
	G = 14 dB, $V_{OD} = 100\text{ mV}_{PP}$		<a href="#">Figure 3</a>
Large Signal Frequency Response	G = 6 dB, $V_{OD} = 2\text{ V}_{PP}$		<a href="#">Figure 4</a>
	G = 10 dB, $V_{OD} = 2\text{ V}_{PP}$		<a href="#">Figure 5</a>
	G = 14 dB, $V_{OD} = 2\text{ V}_{PP}$		<a href="#">Figure 6</a>
Harmonic Distortion	HD <sub>2</sub> , G = 14 dB, $V_{OD} = 2\text{ V}_{PP}$	vs Frequency	<a href="#">Figure 7</a>
	HD <sub>3</sub> , G = 14 dB, $V_{OD} = 2\text{ V}_{PP}$	vs Frequency	<a href="#">Figure 8</a>
	HD <sub>2</sub> , G = 14 dB	vs Output Voltage	<a href="#">Figure 9</a>
	HD <sub>3</sub> , G = 14 dB	vs Output Voltage	<a href="#">Figure 10</a>
Intermodulation Distortion	IMD <sub>2</sub> , G = 14 dB	vs Frequency	<a href="#">Figure 11</a>
	IMD <sub>3</sub> , G = 14 dB	vs Frequency	<a href="#">Figure 12</a>
Output Intercept Point	OIP <sub>2</sub>	vs Frequency	<a href="#">Figure 13</a>
	OIP <sub>3</sub>	vs Frequency	<a href="#">Figure 14</a>
Transition Rate	vs Output Voltage		<a href="#">Figure 15</a>
Transient Response			<a href="#">Figure 16</a>
Rejection Ratios	vs Frequency		<a href="#">Figure 17</a>
Overdrive Recovery			<a href="#">Figure 18</a>
Output Voltage Swing	vs Load Resistance		<a href="#">Figure 19</a>
Turn-Off Time			<a href="#">Figure 20</a>
Turn-On Time			<a href="#">Figure 21</a>
Input Offset Voltage	vs Input Common-Mode Voltage		<a href="#">Figure 22</a>
Input Referred Noise	vs Frequency		<a href="#">Figure 23</a>
Noise Figure	vs Frequency		<a href="#">Figure 24</a>
Quiescent Current	vs Supply Voltage		<a href="#">Figure 25</a>
Output Balance Error	vs Frequency		<a href="#">Figure 26</a>
CM Input Bias Current	vs CM Input Voltage		<a href="#">Figure 27</a>
Differential Output Offset Voltage	vs CM Input Voltage		<a href="#">Figure 28</a>
Output Common-Mode Offset	vs CM Input Voltage		<a href="#">Figure 29</a>

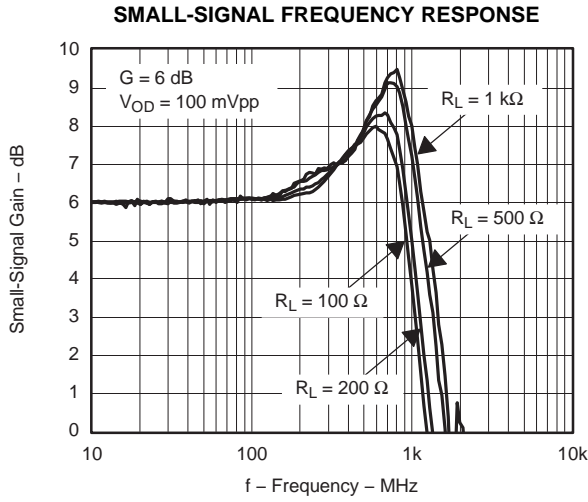


Figure 1.

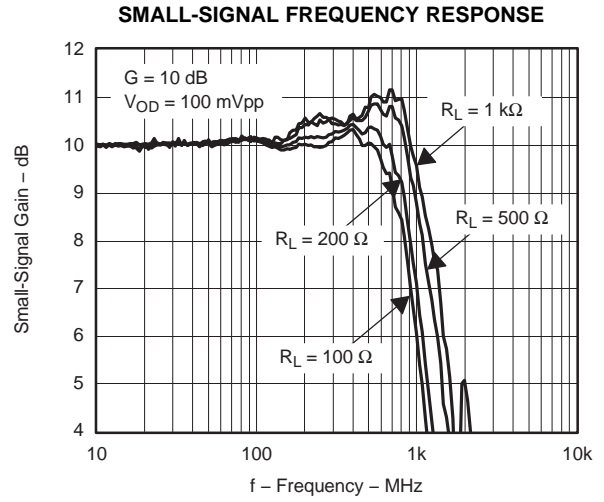


Figure 2.

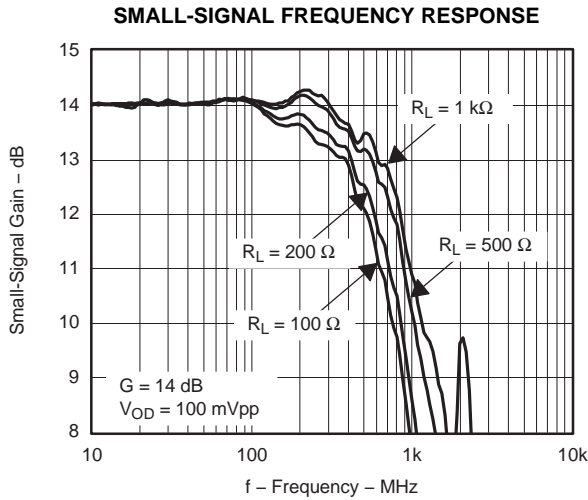


Figure 3.

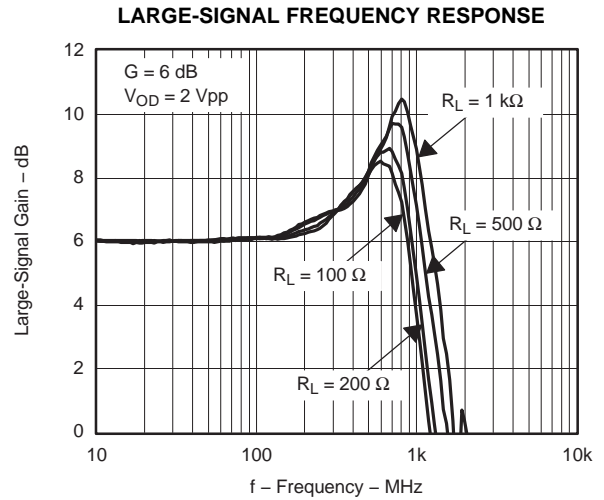


Figure 4.

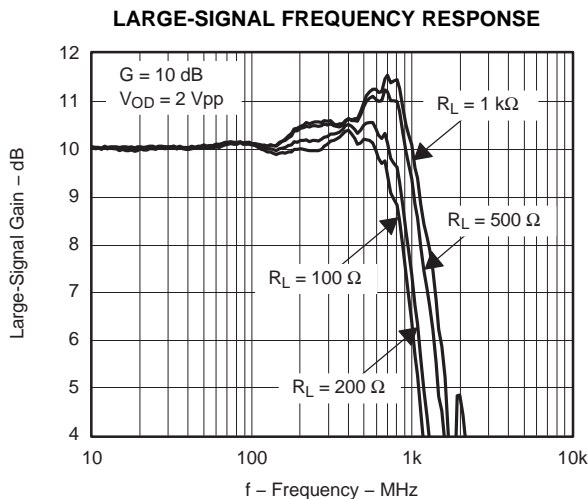


Figure 5.

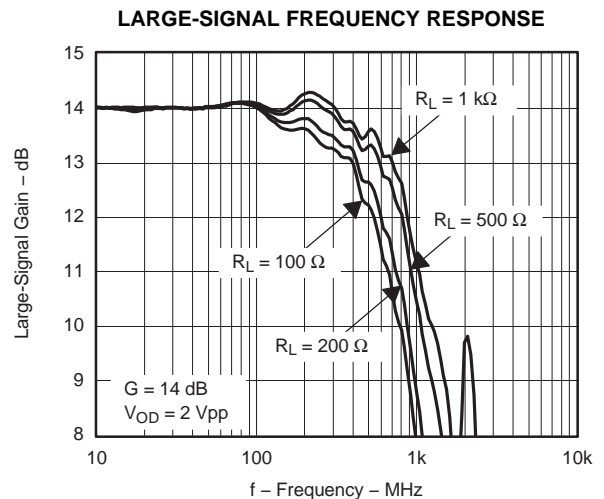


Figure 6.

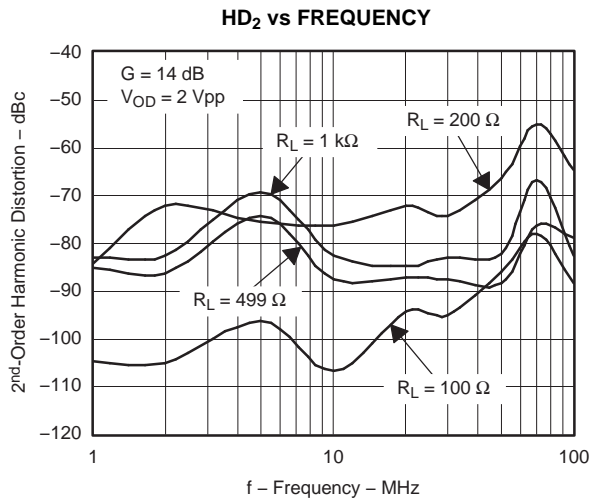


Figure 7.

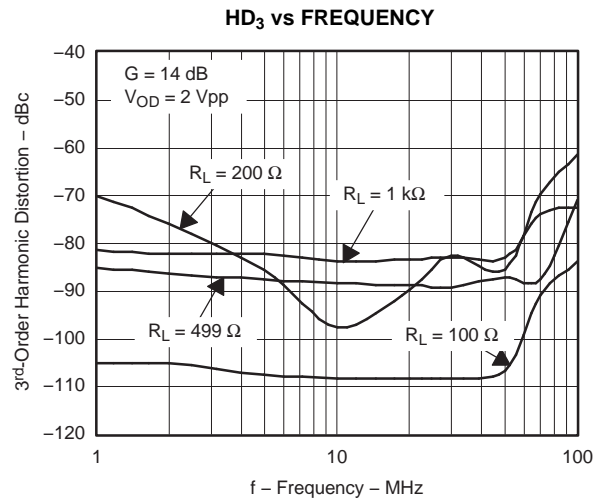


Figure 8.

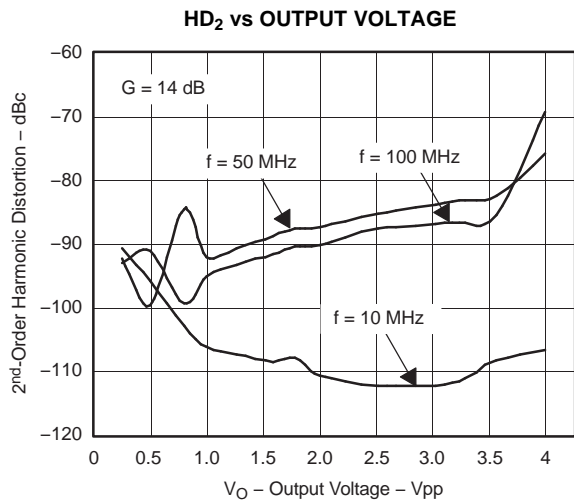


Figure 9.

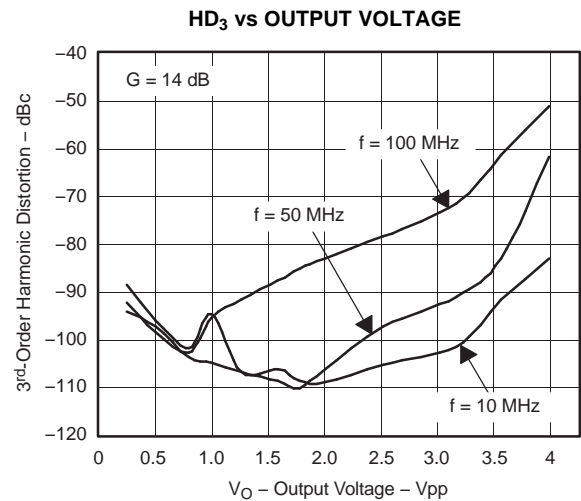


Figure 10.

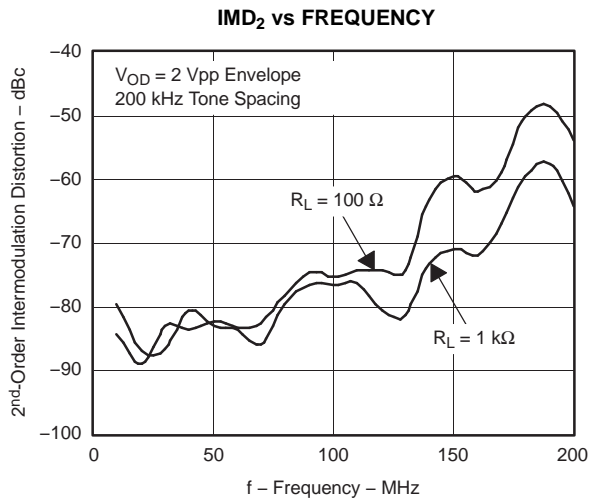


Figure 11.

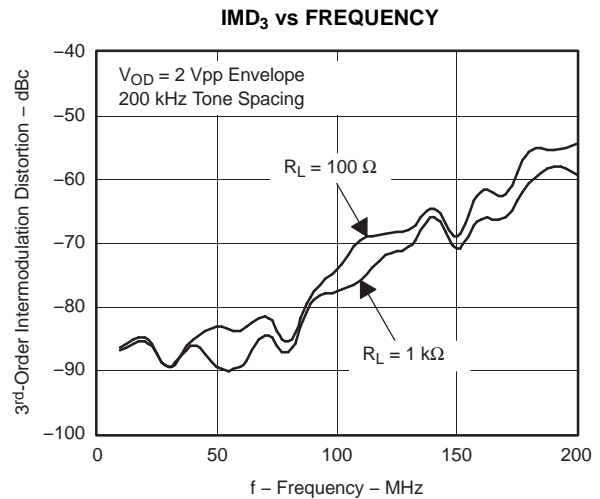
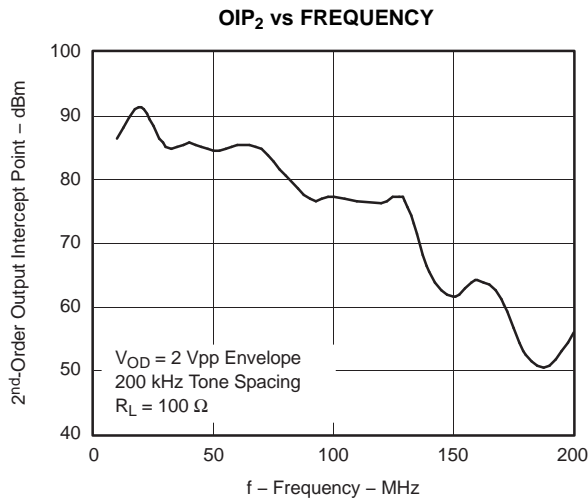
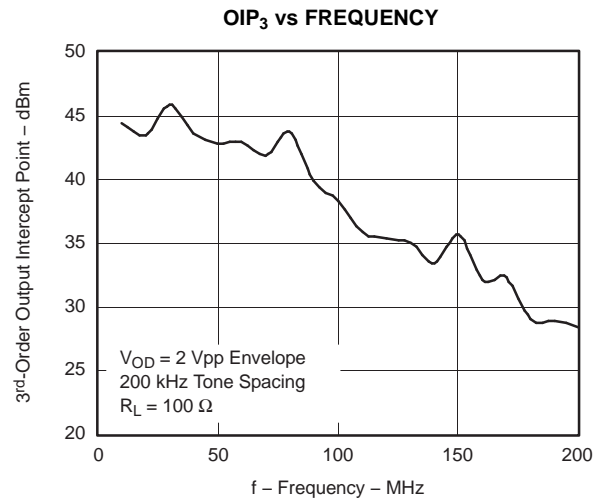


Figure 12.

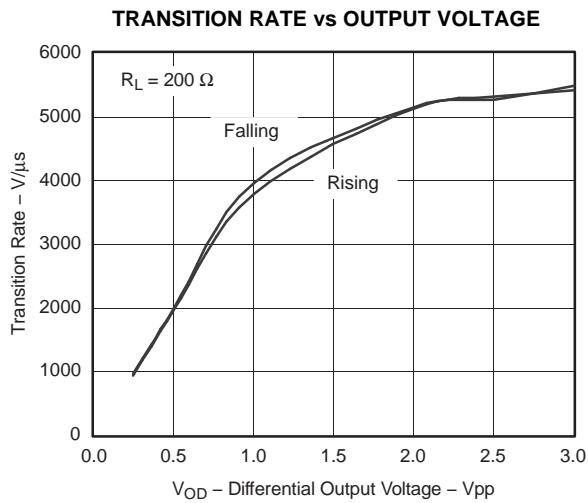




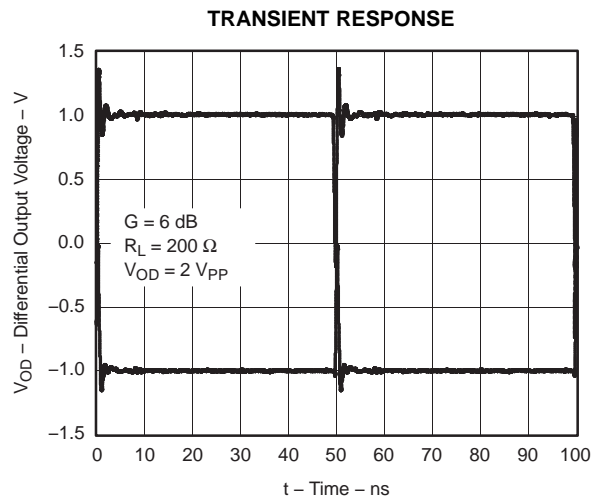
**Figure 13.**



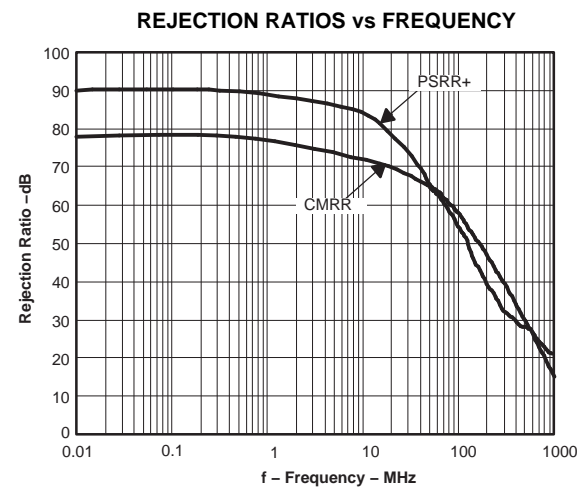
**Figure 14.**



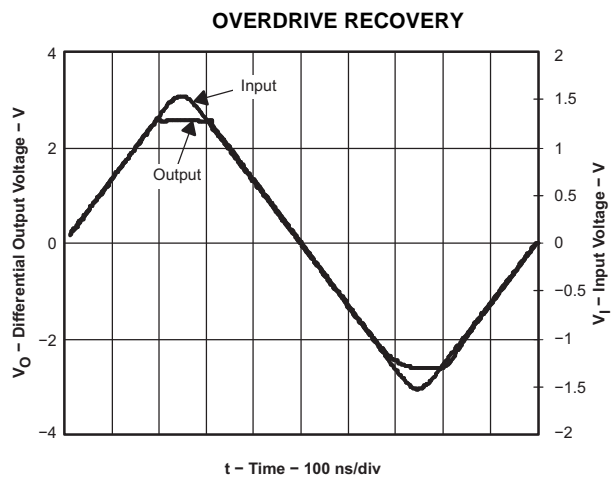
**Figure 15.**



**Figure 16.**



**Figure 17.**



**Figure 18.**

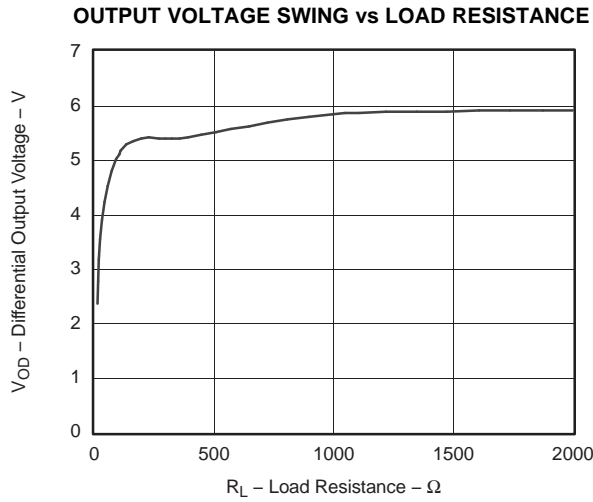


Figure 19.

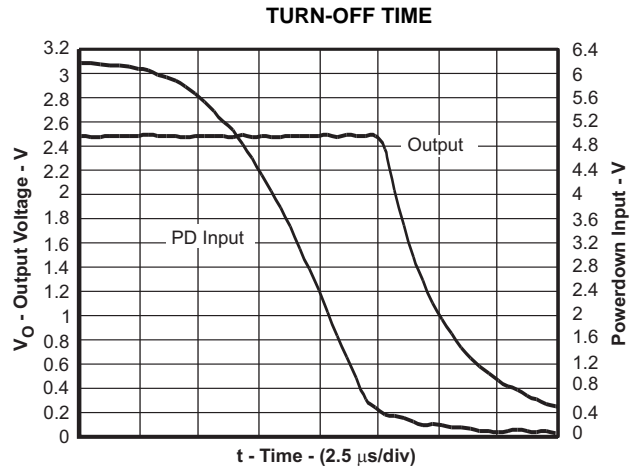


Figure 20.

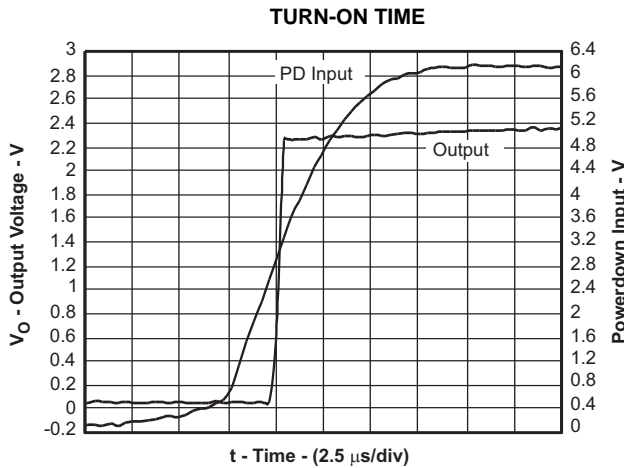


Figure 21.

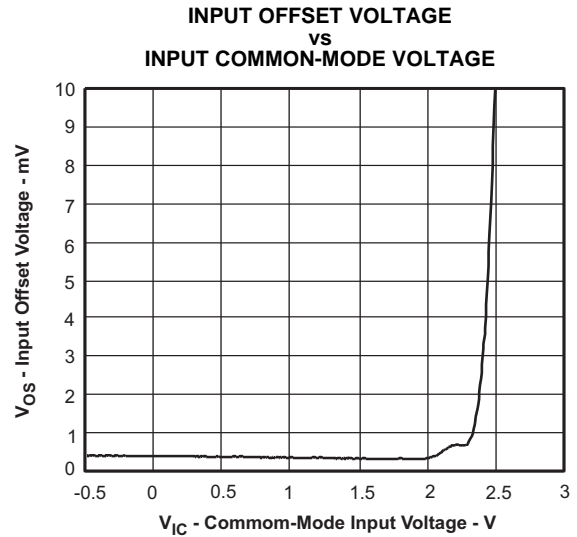


Figure 22.

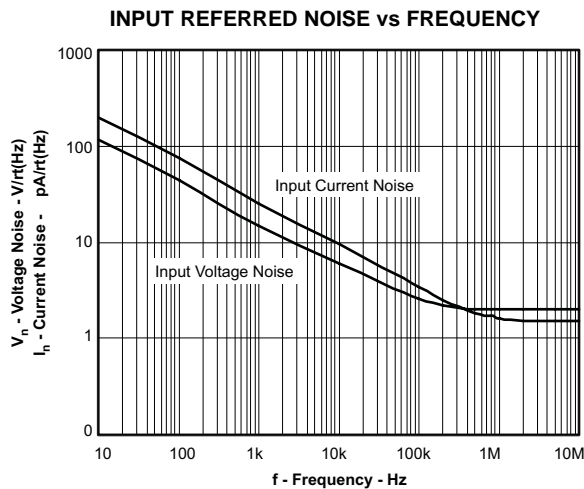


Figure 23.

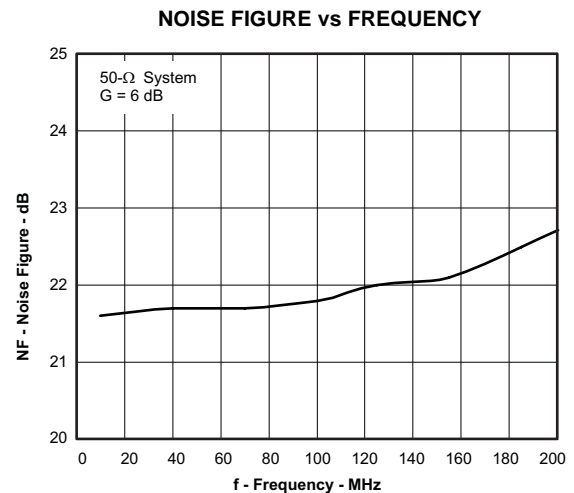


Figure 24.

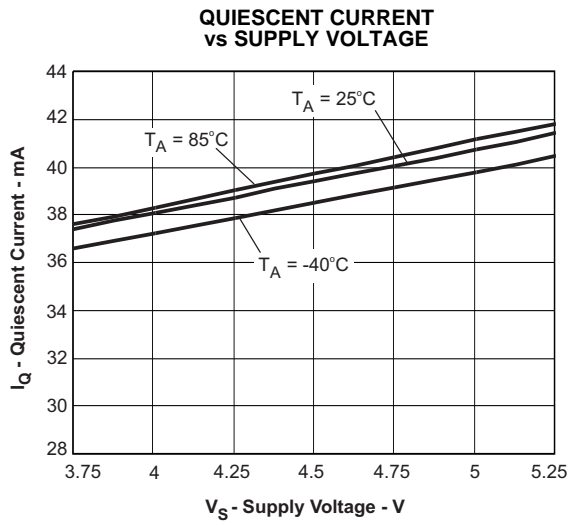


Figure 25.

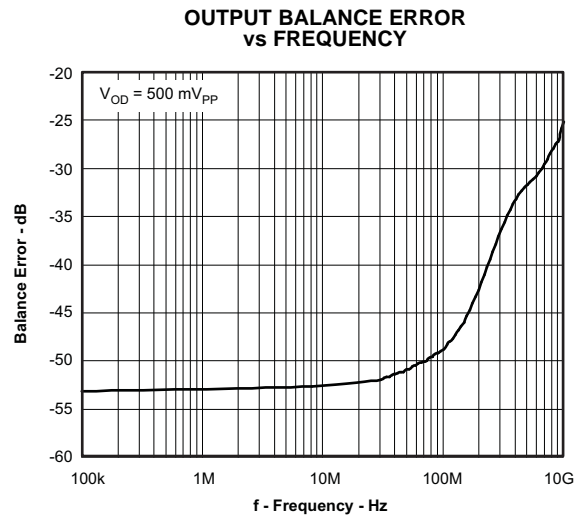


Figure 26.

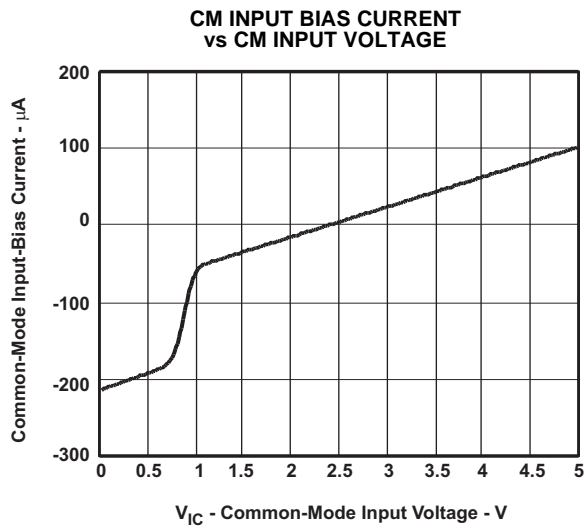


Figure 27.

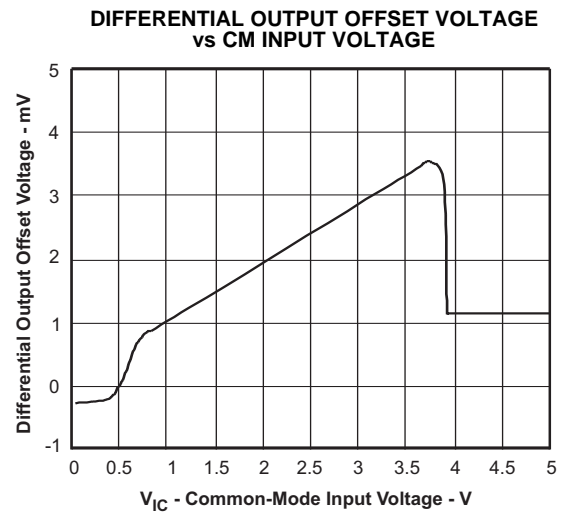


Figure 28.

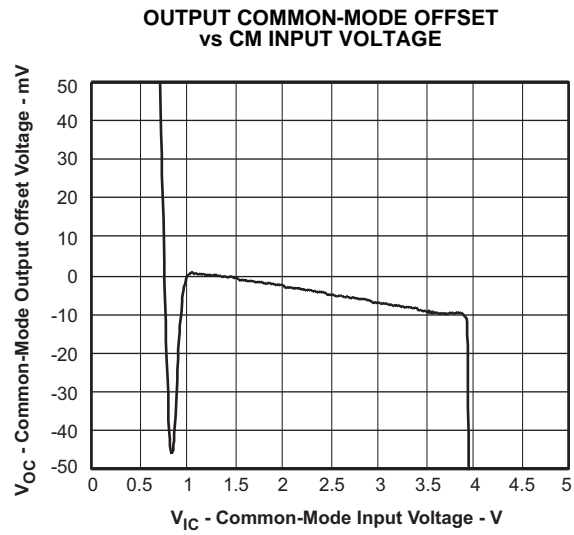


Figure 29.

## TEST CIRCUITS

The THS4511 is tested with the following test circuits. For simplicity, the power supply decoupling is not shown – see the layout in the *application information* section for recommendations. Depending on the test conditions, component values are changed per the following tables, or as otherwise noted. The signal generators used are ac coupled 50 Ω sources, and a 0.22 μF capacitor and a 49.9 Ω resistor to ground are inserted across  $R_{IT}$  on the alternate input to balance the circuit.

**Table 1. Gain Component Values**

GAIN	$R_F$	$R_G$	$R_{IT}$
6 dB	348 Ω	165 Ω	61.9 Ω
10 dB	348 Ω	100 Ω	69.8 Ω
14 dB	348 Ω	56.2 Ω	88.7 Ω
20 dB	348 Ω	16.5 Ω	287 Ω

**Note: The gain setting includes 50 Ω source impedance. Components are chosen to achieve gain and 50 Ω input termination.**

**Table 2. Load Component Values**

$R_L$	$R_O$	$R_{OT}$	Atten
100 Ω	25 Ω	open	6 dB
200 Ω	86.6 Ω	69.8 Ω	16.8 dB
499 Ω	237 Ω	56.2 Ω	25.5 dB
1k Ω	487 Ω	52.3 Ω	31.8 dB

**Note: The total load includes 50 Ω termination by the test equipment. Components are chosen to achieve load and 50 Ω line termination through a 1:1 transformer.**

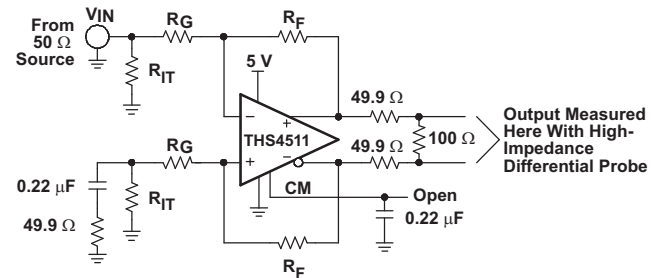
Due to the voltage divider on the output formed by the load component values, the amplifier's output is attenuated. The column *Atten* in Table 2 shows the attenuation expected from the resistor divider. When using a transformer at the output as shown in Figure 31, the signal will see slightly more loss, and these numbers will be approximate.

### Frequency Response

The circuit shown in Figure 30 is used to measure the frequency response of the circuit.

A network analyzer is used as the signal source and as the measurement device. The output impedance of the network analyzer is 50 Ω.  $R_{IT}$  and  $R_G$  are chosen to impedance match to 50 Ω, and to maintain the proper gain. To balance the amplifier, a 0.22 μF capacitor and 49.9 Ω resistor to ground are inserted across  $R_{IT}$  on the alternate input.

The output is probed using a high-impedance differential probe across the 100 Ω resistor. The gain is referred to the amplifier output by adding back the 6 dB loss due to the voltage divider on the output.



**Figure 30. Frequency Response Test Circuit**

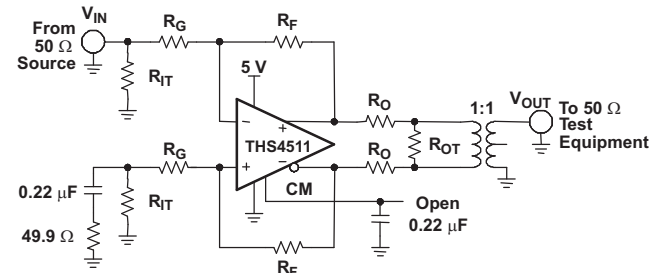
### Distortion

The circuit shown in Figure 31 is used to measure harmonic distortion and intermodulation distortion of the amplifier.

A signal generator is used as the signal source, and the output is measured with a spectrum analyzer. The output impedance of the signal generator is 50 Ω.  $R_{IT}$  and  $R_G$  are chosen to impedance-match to 50 Ω and to maintain the proper gain. To balance the amplifier, a 0.22 μF capacitor and 49.9 Ω resistor to ground are inserted across  $R_{IT}$  on the alternate input.

A low-pass filter is inserted in series with the input to reduce harmonics generated at the signal source. The level of the fundamental is measured, then a high-pass filter is inserted at the output to reduce the fundamental so that it does not generate distortion in the input of the spectrum analyzer.

The transformer used in the output to convert the signal from differential to single ended is an ADT1-1WT. It limits the frequency response of the circuit so that measurements cannot be made below approximately 1 MHz.

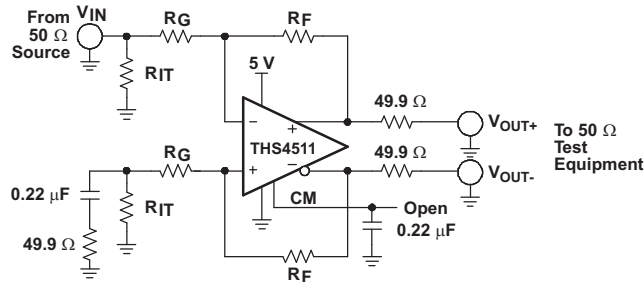


**Figure 31. Distortion Test Circuit**

**Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive, Output Voltage,**

**and Turn-On/Off Time**

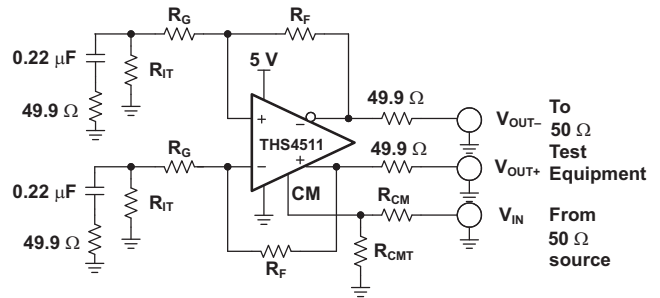
The circuit shown in Figure 32 is used to measure slew rate, transient response, settling time, output impedance, overdrive recovery, output voltage swing, and turn-on/turn-off times of the amplifier. For output impedance, the signal is injected at  $V_{IN}$  with  $V_{IN}$  left open, and the drop across the 49.9  $\Omega$  resistor is used to calculate the impedance seen looking into the amplifier's output.



**Figure 32. SR, Transient Response, Settling Time,  $Z_O$ , Overdrive Recovery,  $V_{OUT}$  Swing, and Turn-on/off Test Circuit**

**CM Input**

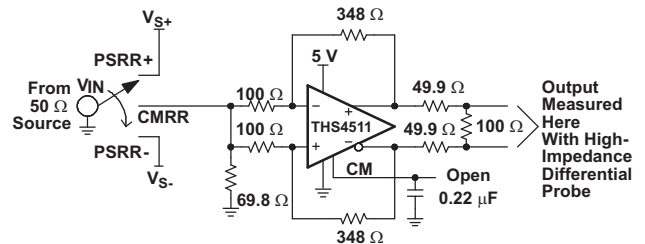
The circuit shown in Figure 33 is used to measure the frequency response and input impedance of the CM input. Frequency response is measured single-ended at  $V_{OUT+}$  or  $V_{OUT-}$  with the input injected at  $V_{IN}$ ,  $R_{CM} = 0 \Omega$  and  $R_{CMT} = 49.9 \Omega$ . The input impedance is measured with  $R_{CM} = 49.9 \Omega$  with  $R_{CMT} = \text{open}$ , and calculated by measuring the voltage drop across  $R_{CM}$  to determine the input current.



**Figure 33. CM Input Test Circuit**

**CMRR and PSRR**

The circuit shown in Figure 34 is used to measure the CMRR and PSRR of  $V_{S+}$  and  $V_{S-}$ . The input is switched appropriately to match the test being performed.



**Figure 34. CMRR and PSRR Test Circuit**

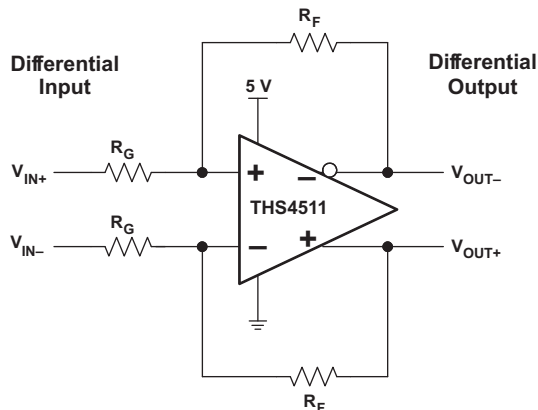
## APPLICATION INFORMATION

### APPLICATIONS

The following circuits show application information for the THS4511. For simplicity, power supply decoupling capacitors are not shown in these diagrams. For more detail on the use and operation of fully differential operational amplifiers, refer to application report *Fully-Differential Amplifiers (SLOA054)*.

#### Differential Input to Differential Output Amplifier

The THS4511 is a fully differential operational amplifier, and can be used to amplify differential input signals to differential output signals. A basic block diagram of the circuit is shown in [Figure 35](#) (CM input not shown). The gain of the circuit is set by  $R_F$  divided by  $R_G$ .

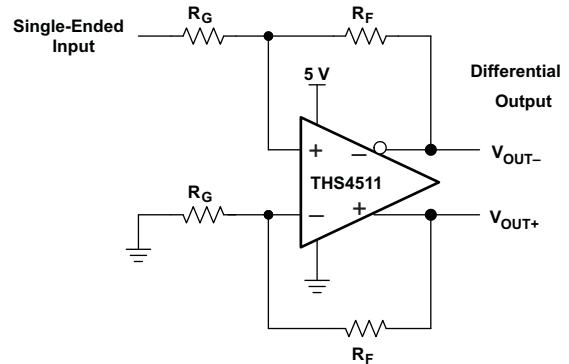


**Figure 35. Differential Input to Differential Output Amplifier**

Depending on the source and load, input and output termination can be accomplished by adding  $R_{IT}$  and  $R_O$ .

#### Single-Ended Input to Differential Output Amplifier

The THS4511 can be used to amplify and convert single-ended input signals to differential output signals. A basic block diagram of the circuit is shown in [Figure 36](#) (CM input not shown). The gain of the circuit is again set by  $R_F$  divided by  $R_G$ .



**Figure 36. Single-Ended Input to Differential Output Amplifier**

#### Input Common-Mode Voltage Range

The input common-mode voltage of a fully differential operational amplifier is the voltage at the (+) and (-) input pins of the operational amplifier.

It is important to not violate the input common-mode voltage range ( $V_{ICR}$ ) of the operational amplifier. Assuming the operational amplifier is in linear operation, the voltage across the input pins is only a few millivolts at most. Finding the voltage at one input pin determines the input common-mode voltage of the operational amplifier.

Treating the negative input as a summing node, the voltage is given by [Equation 1](#):

$$V_{IC} = \left( V_{OUT+} \times \frac{R_G}{R_G + R_F} \right) + \left( V_{IN-} \times \frac{R_F}{R_G + R_F} \right) \quad (1)$$

To determine the  $V_{ICR}$  of the operational amplifier, the voltage at the negative input is evaluated at the extremes of  $V_{OUT+}$ .

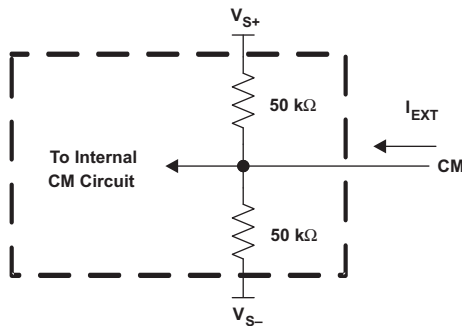
As the gain of the operational amplifier increases, the input common-mode voltage becomes closer and closer to the input common-mode voltage of the source.

**Setting the Output Common-Mode Voltage**

The output common-mode voltage is set by the voltage at the CM pin(s). The internal common-mode control circuit maintains the output common-mode voltage within 5 mV offset (typical) from the set voltage, when set within 0.5 V of mid-supply. If left unconnected, the common-mode set point is set to mid-supply by internal circuitry, which may be over-driven from an external source. Figure 37 is representative of the CM input. The internal CM circuit has about 700 MHz of -3 dB bandwidth, which is required for best performance, but it is intended to be a dc-bias input pin. Bypass capacitors are recommended on this pin to reduce noise at the output. The external current required to overdrive the internal resistor divider is given by Equation 2:

$$I_{EXT} = \frac{2V_{CM} - (V_{S+} - V_{S-})}{50\text{ k}\Omega} \tag{2}$$

where  $V_{CM}$  is the voltage applied to the CM pin, and  $V_{S+}$  ranges from 3.75 V to 5 V, and  $V_{S-}$  is 0 V (ground).

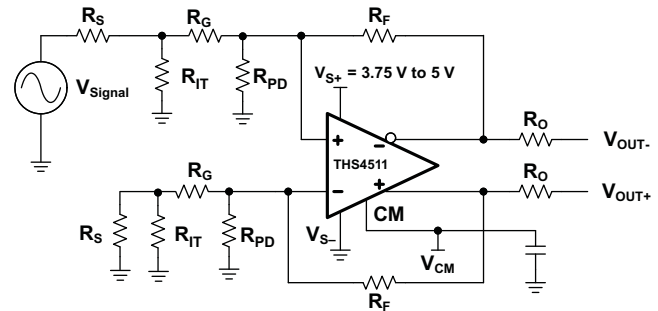


**Figure 37. CM Input Circuit**

**Device Operation with Single Power Supplies Less than 5 V**

The THS4511 is optimized to work in systems using 5 V single supplies, and the characterization data presented in this data sheet was taken with 5 V single-supply inputs. For ac-coupled systems or dc-coupled systems operating with supplies less than 5 V and greater than 3.75 V, the amplifier input common-mode range is maximized by adding pull-down resistors at the device inputs. The pull-down resistors provide additional loading at the input, and lower the common-mode voltage that is fed back into the device input through resistor  $R_F$ . Figure 38 shows the circuit configuration for this mode of operation where  $R_{PD}$  is added to the dc-coupled circuit to avoid violating the  $V_{ICR}$  of the

operational amplifier. Note  $R_S$  and  $R_{IT}$  are added to the alternate input from the signal input to balance the amplifier. One resistor that is equal to the combined value  $R_I = R_G + R_S || R_{IT}$  can be placed at the alternate input.



**Figure 38. THS4511 DC Coupled Single-Source Supply Range From 3.75 V to 5 V With  $R_{PD}$  Used To Set  $V_{IC}$**

Note that in Figure 38, the source is referenced to ground as is the input termination resistor  $R_{IT}$ . The proper value of resistance to add can be calculated from Equation 3:

$$R_{PD} = \frac{1}{\frac{1}{R_F} \left[ \frac{1.6}{\frac{V_{S+}}{2} - 1.6} \right] - \frac{1}{R_I}} \tag{3}$$

where  $R_I = R_G + R_S || R_{IT}$ .

$V_{S+}$  is the power-supply voltage,  $R_F$  is the feedback resistance,  $R_G$  is the gain-setting resistance,  $R_S$  is the signal source resistance, and  $R_{IT}$  is the termination resistance.

Table 3 is a modification of Table 1 to add the proper values with  $R_{PD}$  assuming  $V_{S+} = 3.75$  V, a dc-coupled 50  $\Omega$  source impedance, and setting the output common-mode voltage to mid-supply.

**Table 3.  $R_{PD}$  Values for Various Gains,  $V_{S+} = 3.75$  V, DC-coupled Signal Source**

Gain	$R_F$	$R_G$	$R_{IT}$	$R_{PD}$
6 dB	348 $\Omega$	169 $\Omega$	64.9 $\Omega$	80.6 $\Omega$
10 dB	348 $\Omega$	102 $\Omega$	78.7 $\Omega$	90.9 $\Omega$
14 dB	348 $\Omega$	61.9 $\Omega$	115 $\Omega$	90.9 $\Omega$
20 dB	348 $\Omega$	40.2 $\Omega$	221 $\Omega$	77.6 $\Omega$

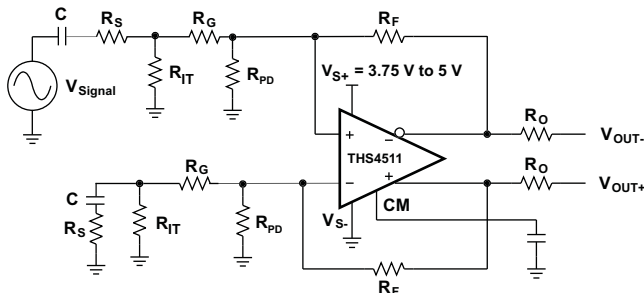
If the signal originates from an ac-coupled 50  $\Omega$  source (see Figure 39), the equivalent dc-source



resistance is an open circuit, and  $R_I = R_G + R_{IT}$ . Table 4 is a modification of Table 1 to add the proper values with  $R_{PD}$  assuming  $V_{S+} = 3.75$  V, an ac-coupled 50  $\Omega$  source impedance, and setting the output common-mode voltage to mid-supply.

**Table 4.  $R_{PD}$  Values for Various Gains,  $V_{S+} = 3.75$  V, AC-Coupled Signal Source**

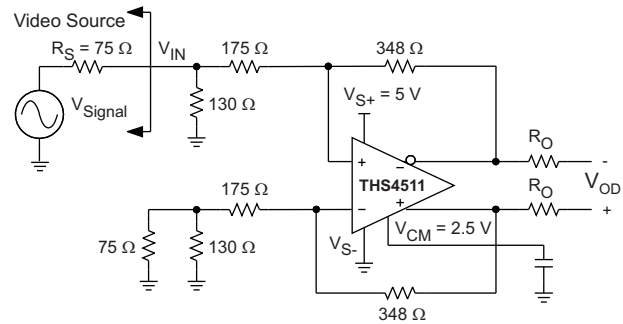
Gain	$R_F$	$R_G$	$R_{IT}$	$R_{PD}$
6 dB	348 $\Omega$	169 $\Omega$	64.9 $\Omega$	86.6 $\Omega$
10 dB	348 $\Omega$	102 $\Omega$	78.7 $\Omega$	110 $\Omega$
14 dB	348 $\Omega$	61.9 $\Omega$	115 $\Omega$	158 $\Omega$
20 dB	348 $\Omega$	40.2 $\Omega$	221 $\Omega$	226 $\Omega$



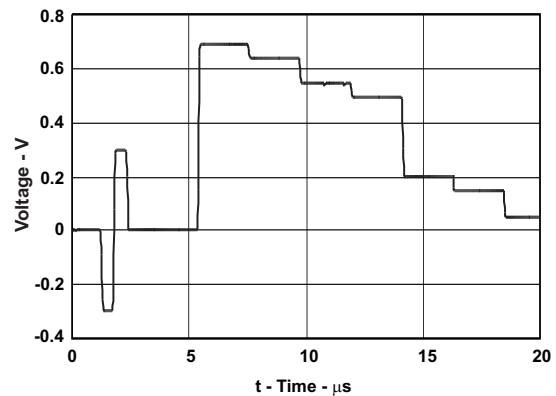
**Figure 39. THS4511 AC Coupled Single-Source Supply Range From 3.75 V to 5 V With  $R_{PD}$  Used to Set  $V_{IC}$**

### Video Buffer

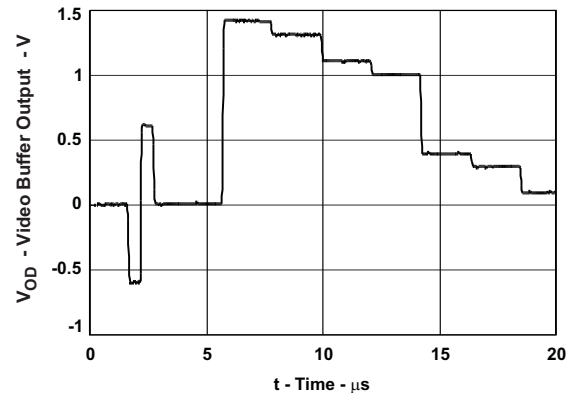
Figure 40 shows a possible application of the THS4511 as a DC-coupled video buffer with a gain of 2. Figure 41 shows a plot of the Y' signal originating from a HDTV 720p video system. The input signal includes a tri-level sync (minimum level at  $-0.3$  V) and the portion of a video signal with maximum amplitude of  $0.7$  V. Although the buffer draws its power from a  $5$  V single-ended power supply, internal level shifters allow the buffer to support input signals, which are as much as  $-0.3$  V below ground. This allows maximum design flexibility while maintaining a minimum parts count. Figure 42 shows the differential output of the buffer. Note that the DC-coupled amplifier can introduce a DC offset on a signal applied at its input.



**Figure 40. Single-Supply Video Buffer, Gain = 2**



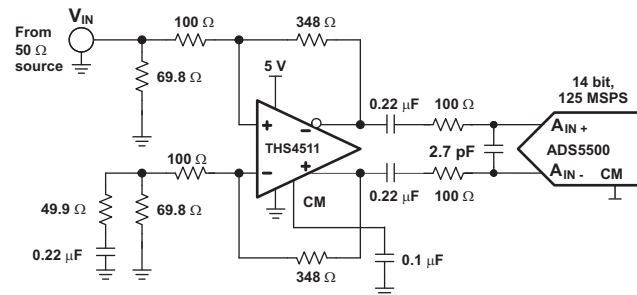
**Figure 41. Y' Signal With 3-Level Sync and Video Signal**



**Figure 42. Video Buffer Differential Output Signal**

**THS4511 + ADS5500 Combined Performance**

The THS4511 is designed to be a high-performance drive amplifier for high-performance data converters like the ADS5500 14 bit 125 MSPS ADC. Figure 43 shows a circuit combining the two devices. The THS4511 amplifier circuit provides 10 dB of gain and converts the single-ended input signal to a differential output signal. The default common-mode output of the THS4511 (2.5 V) is not compatible with the required common-mode input of the ADS5500 (1.55 V), so dc-blocking capacitors are added (0.22  $\mu$ F). Note that a biasing circuit (not shown in Figure 43) is needed to provide the required common-mode, dc-input for the ADS5500. The 100  $\Omega$  resistors and 2.7 pF capacitor between the THS4511 outputs and ADS5500 inputs, along with the input capacitance of the ADS5500, limit the bandwidth of the signal to 115 MHz (-3 dB). For testing, a signal generator is used for the signal source. The generator is an ac-coupled 50  $\Omega$  source. A band-pass filter is inserted in series with the input to reduce harmonics and noise from the signal source. Input termination is accomplished via the 69.8  $\Omega$  resistor and 0.22  $\mu$ F capacitor to ground in conjunction with the input impedance of the amplifier circuit. A 0.22  $\mu$ F capacitor and 49.9  $\Omega$  resistor are inserted to ground across the 69.8  $\Omega$  resistor and 0.22  $\mu$ F capacitor on the alternate input to balance the circuit. Gain is a function of the source impedance, termination, and 348  $\Omega$  feedback resistor. See Table 1 for component values to set proper 50  $\Omega$  termination for other common gains.



**Figure 43. THS4511 + ADS5500 Circuit**

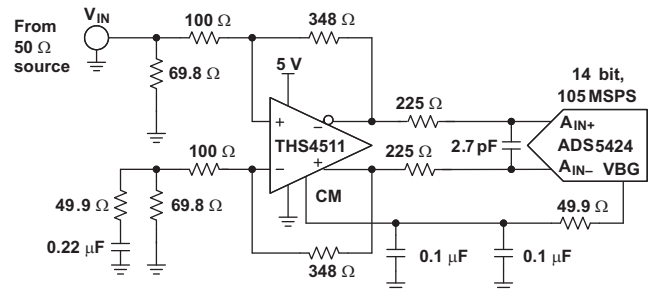
**THS4511 + ADS5424 Combined Performance**

Figure 44 shows the THS4511 driving the ADS5424 ADC.

The THS4511 amplifier provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5424. Input termination and circuit testing is the same as described above for the THS4511 + ADS5500 circuit.

The 225  $\Omega$  resistors and 2.7 pF capacitor between the THS4511 outputs and ADS5424 inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to about 100MHz (-3dB).

When the THS4511 is operated from a single power supply with  $V_{S+} = 5$  V and  $V_{S-} =$  ground, the 2.5 V output common-mode voltage is compatible with the recommended value of the ADS5424 input common-mode voltage (2.4 V).



**Figure 44. THS4511 + ADS5424 Circuit**

### Layout Recommendations

It is recommended to follow the layout of the external components near the amplifier, ground plane construction, and power routing of the EVM as closely as possible. General guidelines are:

1. Signal routing should be direct and as short as possible into and out of the operational amplifier circuit.
2. The feedback path should be short and direct avoiding vias.
3. Ground or power planes should be removed from directly under the amplifier's input and output pins.
4. An output resistor is recommended on each output, as near the output pin as possible.
5. Two 10  $\mu\text{F}$  and two 0.1  $\mu\text{F}$  power-supply decoupling capacitors should be placed as near the power-supply pins as possible.
6. Two 0.1  $\mu\text{F}$  capacitors should be placed between the CM input pins and ground. This limits noise coupled into the pins. One each should be placed to ground near pin 4 and pin 9.
7. It is recommended to split the ground plane on layer 2 (L2) as shown below and to use a solid ground on layer 3 (L3). A single-point connection should be used between each split section on L2 and L3.
8. A single-point connection to ground on L2 is recommended for the input termination resistors R1 and R2. This should be applied to the input gain resistors if termination is not used.

THS4511 EVM

Figure 45 is the THS4511 EVAL1 EVM schematic for the plastic QFN (RGT) package. Layers 1 through 4 of the PCB are shown in Figure 46, and Table 5 is the bill of material for the EVM as supplied from TI. The same layout recommendations should be followed for the THS4511 ceramic flatpack devices. Contact your TI representative for availability of the THS4511 EVM.

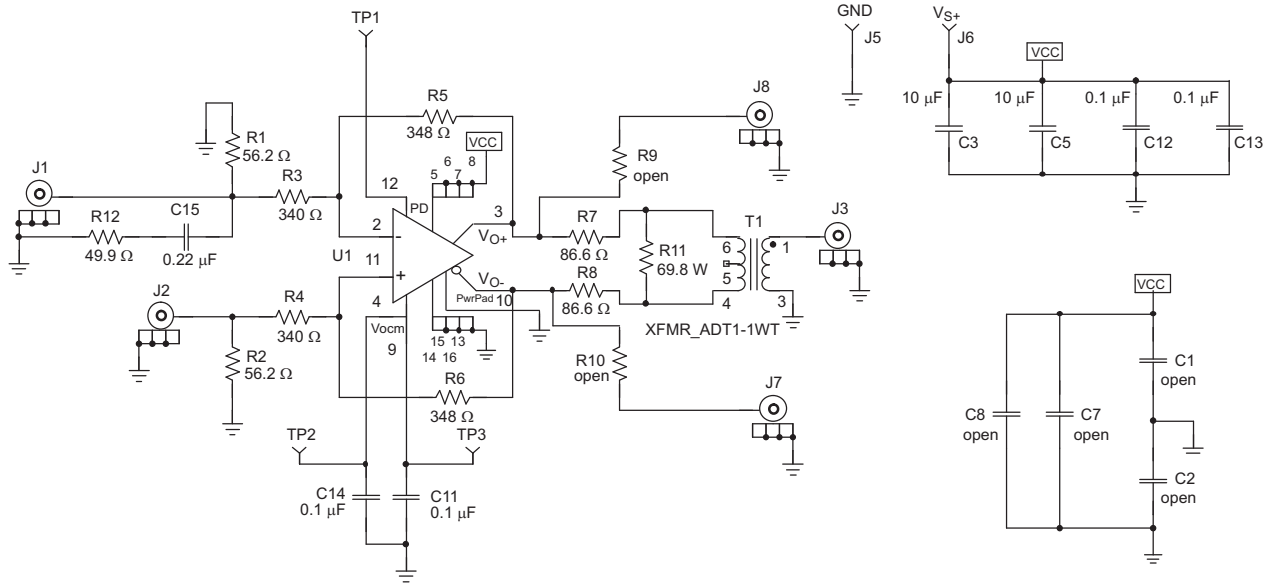


Figure 45. THS4511 EVAL1 EVM Schematic

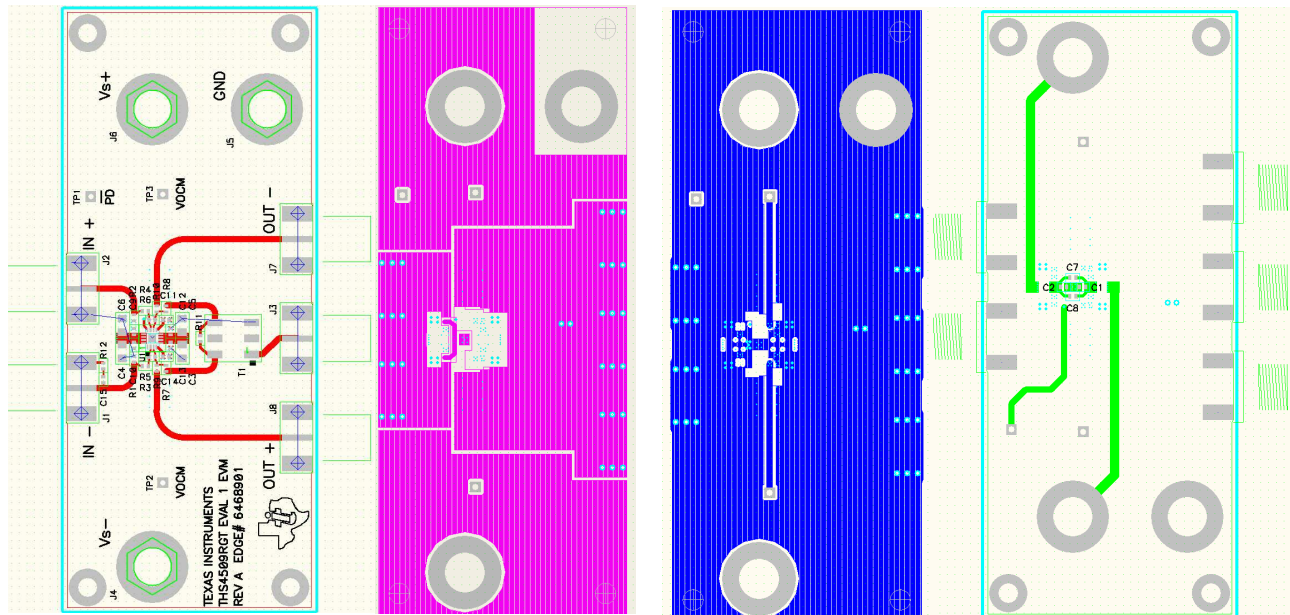


Figure 46. THS4511 EVAL1 EVM Layer 1 Through 4

**Table 5. THS4511RGT EVM Bill of Materials**

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	PCB QTY	MANUFACTURER'S PART NUMBER <sup>(1)</sup>
1	CAP, 10.0 $\mu$ F, Ceramic, X5R, 6.3V	0805	C3, C5	2	(AVX) 08056D106KAT2A
2	CAP, 0.1 $\mu$ F, Ceramic, X5R, 10V	0402	C11, C12, C13, C14	4	(AVX) 0402ZD104KAT2A
3	CAP, 0.22 $\mu$ F, Ceramic, X5R, 6.3V	0402	C15	1	(AVX) 04026D224KAT2A
4	OPEN	0402	C1, C2, C7, C8, C9, C10	6	
5	OPEN	0402	R9, R10	2	
6	Resistor, 49.9 $\Omega$ , 1/16W, 1%	0402	R12	1	(KOA) RK73H1ETTP49R9F
7	Resistor, 56.2 $\Omega$ , 1/16W, 1%	0402	R1, R2		(KOA) RK73H1ETTP56R2F
8	Resistor, 69.8 $\Omega$ , 1/16W, 1%	0402	R11	3	(KOA) RK73H1ETTP69R8F
9	Resistor, 86.6 $\Omega$ , 1/16W, 1%	0402	R7, R8	2	(KOA) RK73H1ETTP86R6F
10	Resistor, 340 $\Omega$ , 1/16W, 1%	0402	R3, R4	2	(KOA) RK73H1ETTP3400F
11	Resistor, 348 $\Omega$ , 1/16W, 1%	0402	R5, R6	2	(KOA) RK73H1ETTP3480F
12	Resistor, 0 $\Omega$ , 5%	0805	C4, C6	2	(KOA) RK73Z2ATTD
13	Transformer, RF		T1	1	(MINI-CIRCUITS) ADT1-1WT
14	Jack, banana receptance, 0.25" diameter hole		J5, J6	2	(HH SMITH) 101
15	OPEN		J1, J7, J8	3	
16	Connector, edge, SMA PCB Jack		J2, J3	2	(JOHNSON) 142-0701-801
17	Test point, Red		TP1, TP2, TP3	3	(KEYSTONE) 5000
18	IC, THS4511		U1	1	(TI) THS4511RGT
19	Standoff, 4-40 HEX, 0.625" length			4	(KEYSTONE) 1808
20	SCREW, PHILLIPS, 4-40, 0.250"			4	SHR-0440-016-SN
21	Printed circuit board			1	(TI) EDGE# 6475513

(1) The manufacturer's part numbers were used for test purposes only.

## EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input and output voltage ranges as specified in the following table.

Input Range, $V_{S+}$ to $V_{S-}$	3.0 V to 6.0 V
Input Range, $V_I$	3.0 V to 6.0 V NOT TO EXCEED $V_{S+}$ or $V_{S-}$
Output Range, $V_O$	3.0 V to 6.0 V NOT TO EXCEED $V_{S+}$ or $V_{S-}$

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the product data sheet or EVM user's guide (if user's guide is available) prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the material provided. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-0722201VFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF THS4511-SP :**

- Catalog: [THS4511](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

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