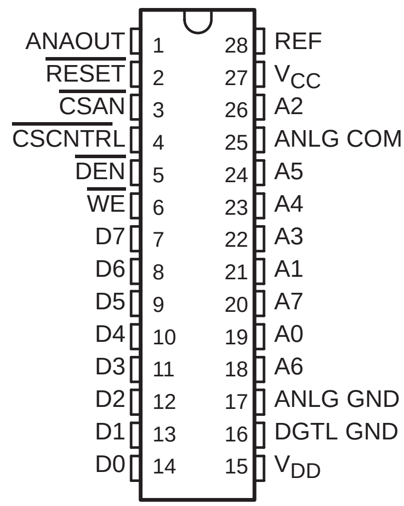
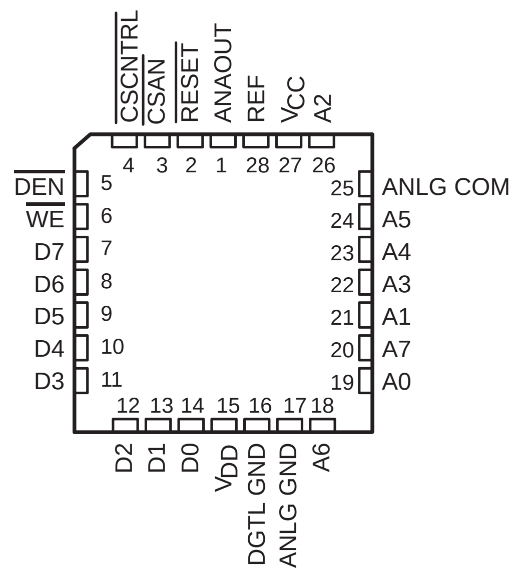
- **Advanced LinCMOS™ Technology**
- **8-Bit Analog-to-Digital Converter**
- **8-Bit Digital-to-Analog Converter**
- **Monotonic Over Entire Analog-to-Digital and Digital-to-Analog Conversion Range**
- **8-Input Analog Multiplexer With Latched Channel Select**
- **Programmable Input Range on Two Input Amplifiers**
- **Interfaces Directly to Many Digital Signal Processors Including the TMS320 Family**
- **Low-Glitch Impulse at DAC Output**
- **Built-In Scaling and Level Shifting on Six of the Analog Inputs**
- **Designed for Servo-Loop Control Systems Including Disk Drives**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TLC32071 is an analog interface integrated circuit that converts between the analog and digital domains. The device includes an 8-bit voltage-output digital-to-analog converter (DAC), an 8-bit analog-to-digital converter (ADC), an analog input multiplexer with eight analog inputs, an output reference MUX, and a high-speed 8-bit bidirectional data bus that interfaces directly to the TMS320 family of digital signal processors. The reset input (RESET) is used to clear the DAC and control registers. The 8-bit DAC converts digital signals to the equivalent analog values. The DAC is followed by a level shifter, which adjusts the center of the DAC output range to the voltage externally applied to the ANLG COM input. One of three output ranges can be selected by an internal register.

The 8-bit ADC converts any one of eight analog inputs selected by a programmable internal register through an input multiplexer. Six of these have inverting inputs with built-in level shifting so that these six output ranges are centered at the ADC input voltage midpoint. Two of the six inputs have register selectable gains. The first conversion result after selection of one of the six inverting inputs should be discarded as invalid. The two remaining inputs are direct inputs to the ADC multiplexer with output ranges centered at the internal 2.5-V reference (V_{ref}). After reset, this reference is available at the REF output. The REF output can also be programmed by an internal control register to provide access to other internal references, any of the analog inputs after scaling and shifting, or the unscaled output of the DAC.

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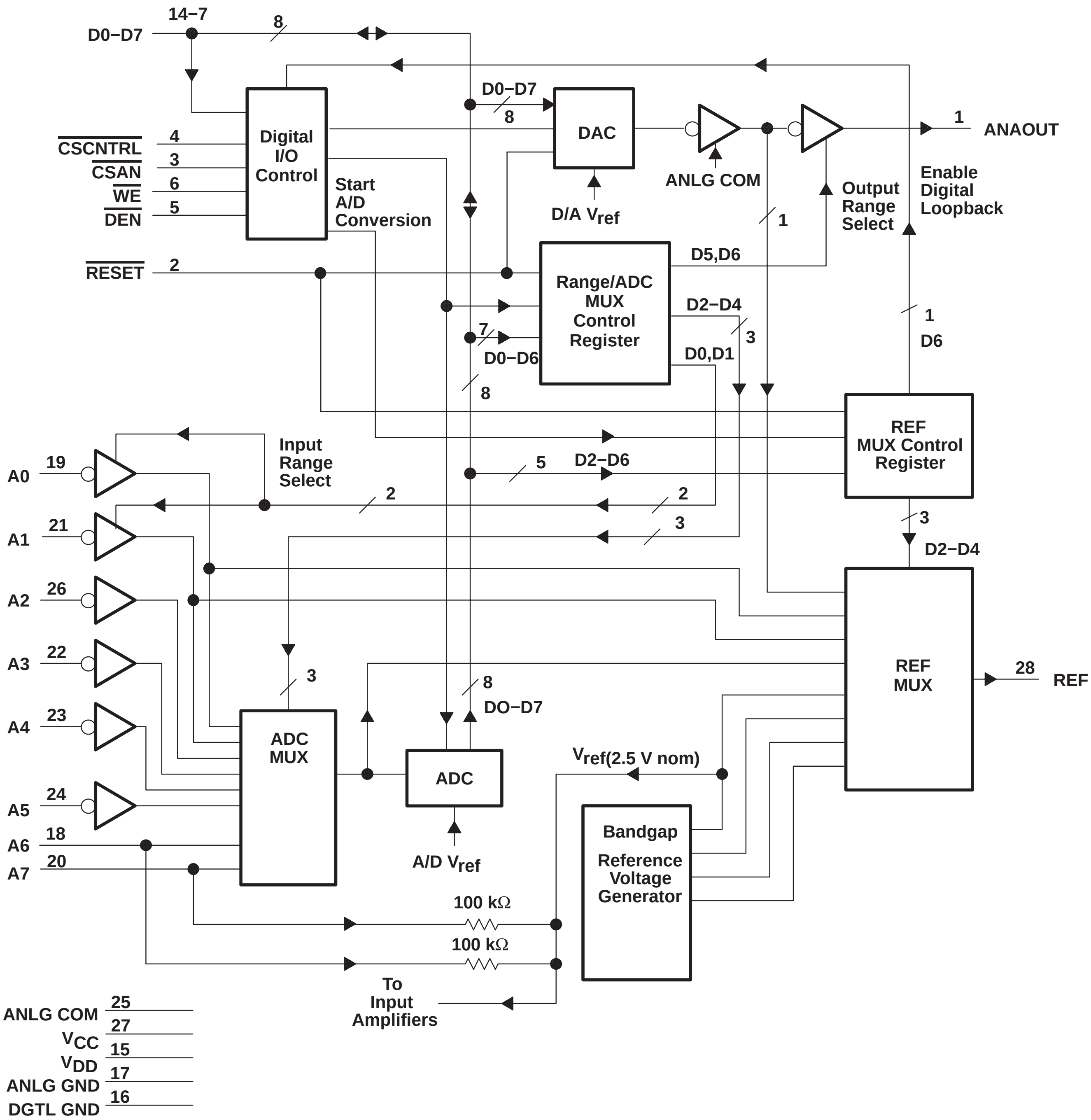
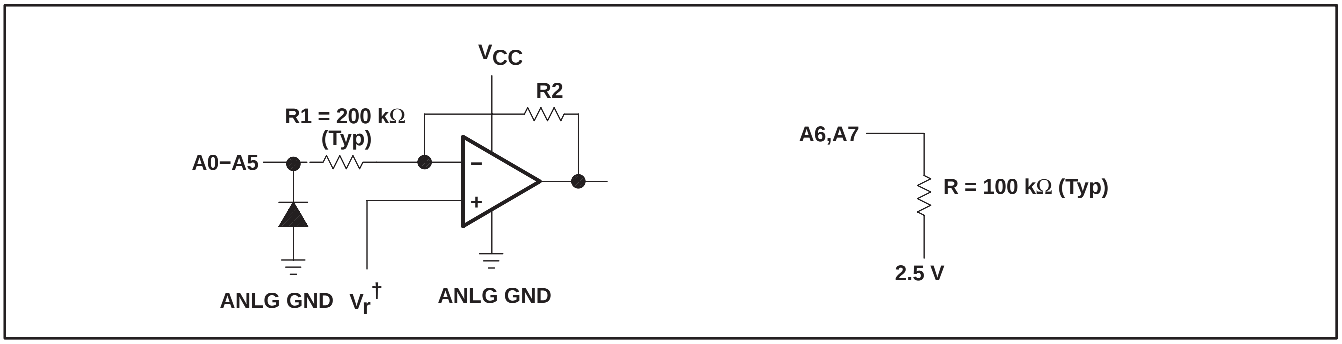
functional block diagram



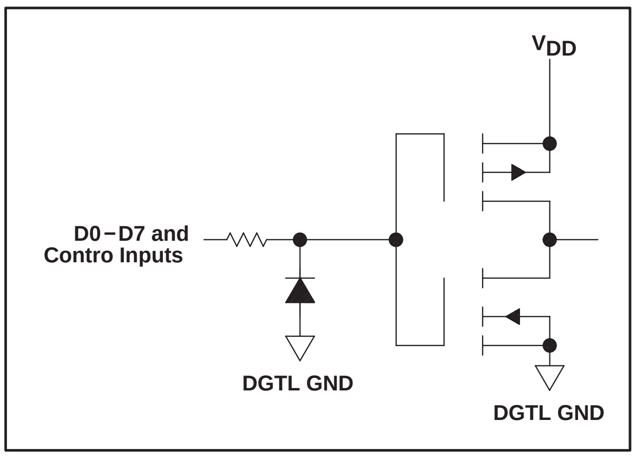
All resistor values shown are nominal.

equivalents of analog input circuit



† V_r is an internally generated voltage with the following typical values: at range = 1, V_r = 3.33 V; at range = 1/2, V_r = 3.75; at range = 1/4, V_r = 4.167 V.

equivalent of digital input circuit



Terminal Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
ANAOUT	1	O	Analog output. The DAC output with selectable ranges.
ANLG COM	25	I	Analog common. Input for reference voltage for inverting analog inputs.
ANLG GND	17		Analog ground. Ground connection associated with ADC, DAC, and other analog circuits.
A0	19	I	Inverting analog input with range programmable to 8, 4, or 2 V. This input uses ANLG COM as a signal ground.
A1	21	I	
A2	26	I	Inverting analog Input. This input uses ANLG COM as a signal ground.
A3	22	I	
A4	23	I	
A5	24	I	
A6	18	I	Auxiliary noninverting analog input with input range of 0.5 to 4.5 V. This input uses the internal reference VR2.5 as a signal ground.
A7	20	I	
$\overline{\text{CSAN}}$	3	I	Chip select for writing to the D/A converter and reading the results of an A/D conversion.
$\overline{\text{CSCNTRL}}$	4	I	Chip select for the control register, which selects DAC and ADC ranges and the analog input channel.
$\overline{\text{DEN}}$	5	I	Read strobe for the A/D converter output. Output buffers are enabled when this signal is held low.
DGTL GND	16		Digital ground. Ground connection associated with digital data-bus signals and other digital circuits.
D7−D0	7−1 4	I/O	Bidirectional data bus. This bus is used for writing conversion data to the DAC, writing data to the range/ADC MUX control register or to the REF MUX control register, and for reading the ADC conversion result.
$\overline{\text{RESET}}$	2	I	Reset. This strobe, when low, clears the range/ADC MUX control register, the REF MUX control register, and the DAC input register. $\overline{\text{CSCNTRL}}$ and $\overline{\text{CSAN}}$ should be held high during a reset operation.
REF	28	O	2.5-V reference output. The signal routed to this pin is determined by the contents of an internal register (see $\overline{\text{CSCNTRL}}$ data word description). The internally generated 2.5-V reference may be selected for use in biasing inputs A6 and A7.
V_{DD}	15		5-V (digital) supply
V_{CC}	27		10-V (analog) supply
$\overline{\text{WE}}$	6	I	Write enable. This input is a write strobe for the control registers and the DAC input register. Data is latched on the rising edge of this signal.

PRINCIPLES OF OPERATION

writing control words to the TLC32071

With the CSCNTRL input low, a control word is written to the TLC32071 by placing data on the D7−D0 inputs and applying a low-going pulse to the write enable input (WE). Data is latched on the rising edge of the WE pulse. The values of D0 and D1 of the control word determine whether the data is latched in the range/ADC MUX control register or the REF MUX register. See Tables 1, 2, 3, and 4 for data-bit formats.

operation of the ADC channel

Analog-to-digital conversion begins when gain-select and channel-select data word is latched in the range/ADC MUX control register by the rising edge of the WE pulse. This data word controls the state of the range/ADC input multiplexer. After the conversion time, the conversion result may be read by taking the DEN input low while the CSAN input is low. Writing of data to the REF MUX control register (using CSCNTRL and WE with D0 and D1 both 0) does not start a conversion. Each time one of the A0 through A5 signal channels is selected, the first conversion result after selection should be ignored due to internal input amplifier settling time. If this channel remains selected, subsequent conversions are valid.

operation of the DAC channel

When the CSAN input is low, digital-to-analog conversion is performed by placing input data on data bus DB7−DB0 and applying a low-going pulse to WE. The data word is latched on the rising edge of the WE pulse and is decoded to an equivalent analog voltage. The conversion occurs internally in approximately 100 ns with the D/A conversion result available at the ANAOUT output after a specified settling time.

digital loopback mode

Digital loopback enables the simultaneous testing of the A/D and D/A channels. When digital loopback is enabled, the A/D conversion result is transferred to the D/A input latches on the next rising edge of DEN. The analog signal from the input pin at the A/D converter is transferred through the D/A converter to the analog output ANAOUT. To enable digital loopback, write to the REF MUX control register (see data word format in Table 3) to set bit D6. Then, perform A/D conversion (as in normal operation) by writing channel select and range select information to the range/ADC MUX control register. This is done by strobing WE while CSCTRL is low. Read the conversion result by strobing DEN while holding CSAN low when digital loopback is enabled. The A/D conversion result is transferred to the DAC on the rising edge of DEN (See Tables 1, 2, 3, and 4).

reset operation

CSAN and CSCNTRL should be held high during a reset operation. When the RESET input is taken low, the internal reset signal clears the range/ADC MUX control register, the REF MUX control register, and the DAC input register. The following conditions exist after reset:

1. The DAC output is set to the voltage at the ANLG COM input.
2. The DAC range is set to ANLG COM ±4 V.
3. The A0 analog channel is selected and the A0 and A1 amplifier ranges are set to ANLG COM ±4 V.
4. The 2.5 V reference is selected at the REF output.
5. Digital loopback is disabled.

analog inputs

The ANLG COM voltage establishes the operating midpoint of the input amplifiers, A0 through A5. When the input signal voltage equals this voltage, the ADC output is ideally digital count zero. These amplifiers level shift to the ADC midpoint of 2.5 V and scale the input voltage range to the ADC range of 0.5 to 4.5 V. The A6 and A7 noninverting inputs are centered at the 2.5 V internally generated voltage reference and are connected directly to the input MUX. Table 5 gives the full scale input range and the midpoint voltages applicable for the individual analog inputs.

Table 1. Data Word Formats (Channel Range Selection)

D1	D0	A0/A1 CHANNEL PROGRAMMABLE GAIN	DATA DESTINATION	INPUT FULL SCALE RANGE (ANLG COM=5)	MIN	MAX
L	L	No range selection	Higher-order bits are sent to REF-MUX register			
L	H	Range is set to 1	Higher-order bits are sent to ADC channel-select register	ANLG COM ±4 V	1 V	9 V
H	L	Range is set to 1/2		ANLG COM ±2 V	3 V	7 V
H	H	Range is set to 1/4		ANLG COM ±1 V	4 V	6 V

Table 2. Data Word Formats (RANGE/ADC-Multiplexer Channel Selection)
(Data chosen from this table is only valid when data bits D1 and D0 are not both low)

SELECTED CHANNEL	D7	D6	D5	D4	D3	D2
A0	X	X	X	L	L	L
A1	X	X	X	L	L	H
A2	X	X	X	L	H	L
A3	X	X	X	L	H	H
A4	X	X	X	H	L	L
A5	X	X	X	H	L	H
A6	X	X	X	H	H	L
A7	X	X	X	H	H	H

Table 3. Data Word Formats (DAC Output Range Selection)
(Data chosen from this table is only valid when data bits D1 and D0 are not both low)

D6	D5	DAC OUTPUT RANGE	OUTPUT FULL SCALE RANGE (ANLG COM=5)	MIN	MAX
L	X	Range is set to 1	ANLG COM ±4 V	1 V	9 V
H	L	Range is set to 1/2	ANLG COM ±2 V	3 V	7 V
H	H	Range is set to 1/4	ANLG COM ±1 V	4 V	6 V

Table 4. Data Word Formats (REF-Multiplexer Channel Selection)
(Data chosen from this table is valid only when data bits D1 and D0 are both low)

SELECTED CHANNEL	D6	D5	D4	D3	D2
V_{ref} (2.5 V nom)	X	X	L	L	L
Bandgap (ACOM + 1.25 V)	X	X	L	L	H
A/D reference (approximately 4.6 V)	X	X	L	H	L
D/A reference (ANLG COM −3 V)	X	X	L	H	H
A0 amp output†	X	X	H	L	L
A1 amp output†	X	X	H	L	H
ADC MUX output†	X	X	H	H	L
DAC level shift output‡	X	X	H	H	H
Enable digital loopback	H	X	X	X	X

† These signals are outputs of scaling/level-shifting amplifiers. The range of these signals is V_{ref} ±2 V.
‡ The unscaled output of the DAC. This analog output is proportional to the DAC value with a fixed range of ANLG COM ±1 V, but inverted relative to the twos-complement code written to the DAC.

Table 5. Analog Input Characteristics

INPUT	V_{mid}†	NOMINAL FSR‡	INPUT VOLTAGE RANGE (ANLG COM=5)	
			MIN	MAX
A0, A1§ (1)	ANLG COM	±4 V	1 V	9 V
(1/2)	ANLG COM	±4 V	3 V	7 V
(1/4)	ANLG COM	±4 V	4 V	6 V
A2 thru A5§	ANLG COM	±4 V	1 V	9 V
A6, A7	V_{ref}¶	±2 V	0.5 V	4.5 V

† V_{mid} is (VP127-VM127)•127.5/254+VM127 where VP127 is the minimum input voltage to produce an output code of +127, and VM127 is the minimum input voltage to produce an output code of −127.
‡ Full-scale range is (VP127−VM127)•256/254 where VP127 is the minimum input voltage to produce an output code of +127, and VM127 is the minimum input voltage to produce an output code of −127.
§ Inverting inputs
¶ V_{ref} is an internally generated reference voltage that can be available at the REF output. The inputs A6 and A7 are connected to V_{ref} through an on-chip resistor.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (analog supply) (see Note 1) . . . . −0.5 V to 14 V
Supply voltage range, V_{DD} (digital supply) (see Note 2) . . . . −0.5 V to 7 V
Digital ground voltage range, DGTL GND . . . . −0.5 V to 0.5 V
Analog output voltage range (see Note 1) . . . . −0.5 V to V10 + 0.5 V
Analog input voltage range (see Note 1) . . . . −0.5 V to 14 V
Digital output voltage range (see Note 2) . . . . −0.5 V to V5 + 0.5 V
Digital input voltage range (see Note 2) . . . . −0.5 V to V5 + 0.5 V
Operating free-air temperature range, T_A . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C
Case temperature for 10 seconds: FN package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . 260°C

NOTES: 1. All voltage values are given with respect to ANLG GND unless otherwise noted.
2. All voltage values are with respect to DGTL GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	9	10	12	V
Supply voltage, V_{DD}	4.5	5	5.5	V
High-level input voltage, V_{IH} (digital inputs)	2.4			V
Low-level input voltage, V_{IL} (digital inputs)			0.5	V
Reference voltage input at ANLG COM† input, V_{ref}	3.5	5	6	V
Setup time, $\overline{CSCNTRL}$ low before $\overline{WE}$ low, $t_{su(CS)}$	0			ns
Hold time, $\overline{CSCNTRL}$ high after $\overline{WE}$ high, $t_{h(CS)}$	0			ns
Setup time, data bus before $\overline{CSCNTRL}$ high, $t_{su(D)}$	15			ns
Hold time, data bus after $\overline{CSCNTRL}$ high, $t_{h(D)}$	15			ns
Pulse duration, $\overline{DEN}$, $t_{w(DEN)}$	t_a‡			ns
Setup time, $\overline{CSAN}$ low before $\overline{DEN}$ low, $t_{su(CS)}$	0			ns
Hold time, $\overline{CSAN}$ high after $\overline{DEN}$ high, $t_{h(CS)}$	0			ns
Setup time, $\overline{CSAN}$ low before $\overline{WE}$ low, $t_{su(CS)}$	0			ns
Hold time, $\overline{CSAN}$ high after $\overline{WE}$ high, $t_{h(CS)}$	0			ns
Pulse duration, $\overline{RESET}$, $t_{w(RE)}$	25			ns
Pulse duration, $\overline{WE}$, $t_{w(WE)}$	30			ns
Operating free-air temperature, T_A	0		70	°C

† For a DAC range of R = (1, 1/2, 1/4), ANLG COM should be chosen so that ANLG COM ±4R is greater than 0.5 V and less then V_{CC} −0.5 V or the DAC output may not be able to deliver the specified maximum current without voltage limiting occurring.
‡ Access time

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} at 4.5 V, I_{OH} = −360 µA	2.4			V
V_{OL}	Low-level output voltage	V_{DD} at 4.5 V, I_{OL} = 1.6 mA			0.4	V
V_{ref}	Reference voltage output (see Note 3)	ANLG COM = 5 V	2.42	2.5	2.58	V
$R_{O(ref)}$	Reference output resistance	ANLG COM = 5 V		0.8	1.2	kΩ
I_{IH}	High-level input current	V_{IH} = 5 V			10	µA
I_{IL}	Low-level input current	V_{IL} = 0			− 10	µA
I_{DD}	Supply current, digital	D0−D7 at V_{IH} or V_{IL}			20	mA
I_{CC}	Supply current, analog				22	mA
I_{OZ}	Off-state output current (high-impedance state)	V_O = 5 V			3	µA
		V_O = 0			−3	
I_{OS}	Short-circuit output current	V_O = 5 V	25	40		mA
		V_O = 0	−45	−60		
C_o	Output capacitance (digital outputs)				5	pF

§ All typical values are at T_A = 25°C.
NOTE 3: This voltage is an internal reference voltage (2.5 V) that is available at the output-multiplexer output.

ADC operating characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
	Linearity error				±1	LSB
$V_{I(FS)}$ †	Input voltage for full-scale output code (Input channel = A6 or A7)			3.92	4.08	V
V_{mid} ‡	ADC input offset voltage (Input channel = A6 or A7)			V_{ref} − 0.06	V_{ref} + 0.06	V
t_{conv}	Conversion time	See Figure 2			2.5	μs
t_a	Access time (delay from falling edge of $\overline{DEN}$ to data output)	See Figure 3	C_L = 100 pF§		50	ns
			C_L = 50 pF§		41	
			C_L = 25 pF§		37	
t_{dis}	Disable time (delay from rising edge of $\overline{DEN}$ to high-impedance state of data output)	See Figure 3	C_L = 100 pF		35	ns

† Full-scale range is (VP127−VM127) • 256/254 where VP127 is the minimum input voltage to produce an output code of +127, and VM127 is the minimum input voltage to produce an output code of − 127.
‡ V_{mid} is (VP127−VM127) • 127.5/254 + VM127 where VP127 is the minimum input voltage to produce an output code of +127, and VM127 is the minimum input voltage to produce an output code of − 127.
§ C_L is in addition to the internal capacitance of the digital output.

DAC operating characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP¶	MAX	UNIT
t_s	Settling time (to 1 LSB)	Load on ANAOUT = 20 pF + 5 kΩ (to ANLG COM)			8	15	μs
E_L	Linearity error					±1	LSB
	Code width			0.25		1.75	LSB
$V_{O(FS)}$	Output voltage swing#, full scale (VP127−VM128)•256/255	DAC input = − 128 to +127	Range = 1	7.84	8	8.16	V
			Range = 1/2	3.92	4	4.08	
			Range = 1/4	1.96	2	2.04	
	Output bias level#, full scale (VP127−VM128)•128/255+VM128	DAC input = 0	Range = 1	ANLG COM − 0.08		ANLG COM+0.08	V
			Range = 1/2	ANLG COM − 0.06		ANLG COM+0.06	
			Range = 1/4	ANLG COM − 0.05		ANLG COM+0.05	
	Glitch energy	Sample rate = 30 kHz				1.2	mV
I_{OM}	Maximum output current, ANAOUT	Source from V_{CC} − 0.5 V or sink from 0.5 V		1.2			mA

¶ Typical values are at T_A = 25°C.
# VP127 is the voltage output for an input code of +127. VM128 is the voltage output for an input code of − 128.

ADC electrical characteristics for inputs A0 and A1 over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
A_V1	Voltage amplification	Range = 1		0.99	1	1.01	V/V
A_V2	Voltage amplification	Range = 1/2		1.98	2	2.02	V/V
A_V4	Voltage amplification	Range = 1/4		3.96	4	4.04	V/V
$V_{OB}1$	Output bias voltage at input of ADC with respect to V_{ref}	$V_I = V_{(ANLG\ COM)}$,	Range = 1		0	±0.02	V
$V_{OB}2$	Output bias voltage at input of ADC with respect to V_{ref}	$V_I = V_{(ANLG\ COM)}$,	Range = 1/2		0	±0.03	V
$V_{OB}4$	Output bias voltage at input of ADC with respect to V_{ref}	$V_I = V_{(ANLG\ COM)}$,	Range = 1/4		0	±0.05	V
r_i	Input resistance			140	200	260	kΩ

ADC electrical characteristics for inputs A2, A3, A4 and A5 over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_V	Voltage amplification to ADC		−0.495	−0.5	−0.505	V/V
V_{OB}	Output bias voltage at the input of the ADC with respect to V_{ref}	$V_I = V_{(ANLG\ COM)}$	−0.02	0	+0.02	V
r_i	Input resistance		140	200	260	kΩ

ADC electrical characteristics for inputs A6 and A7 (direct inputs) over recommended free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_V	Voltage amplification to ADC			1		V/V
r_i	Input resistance (to REF)		70	100	130	kΩ

PARAMETER MEASUREMENT INFORMATION

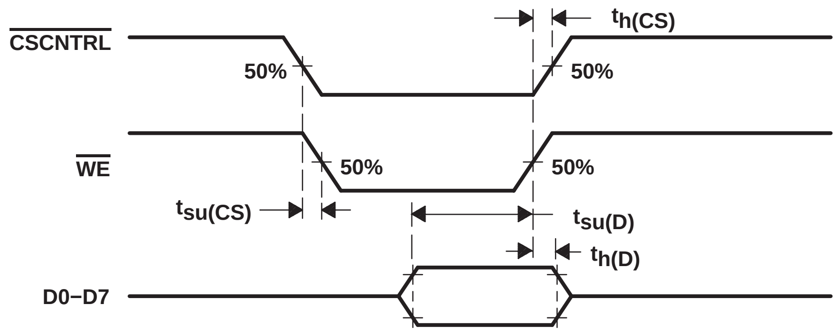


Figure 1. Write Operation

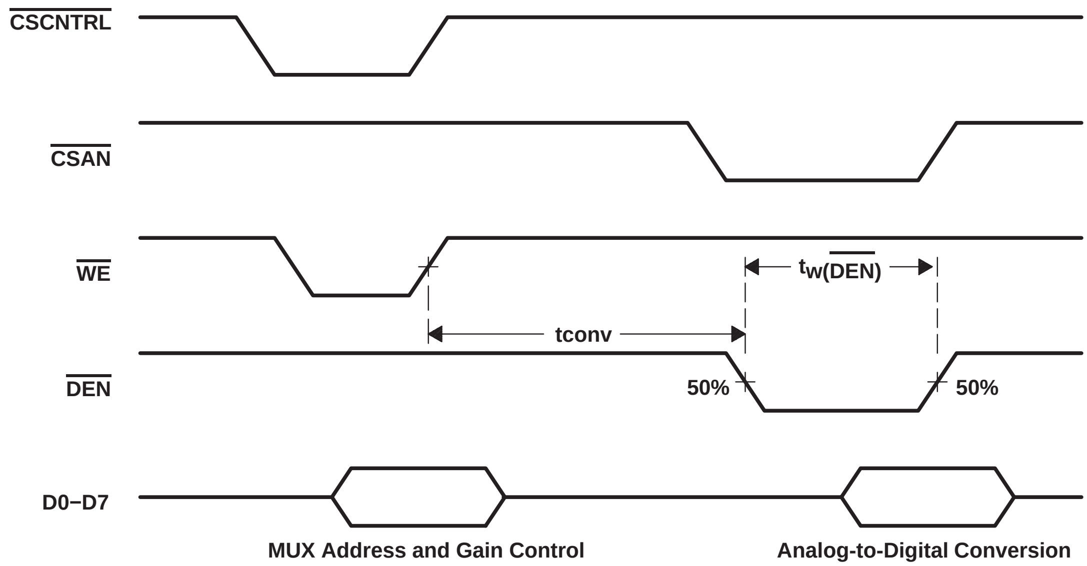


Figure 2. A/D Conversion Cycle

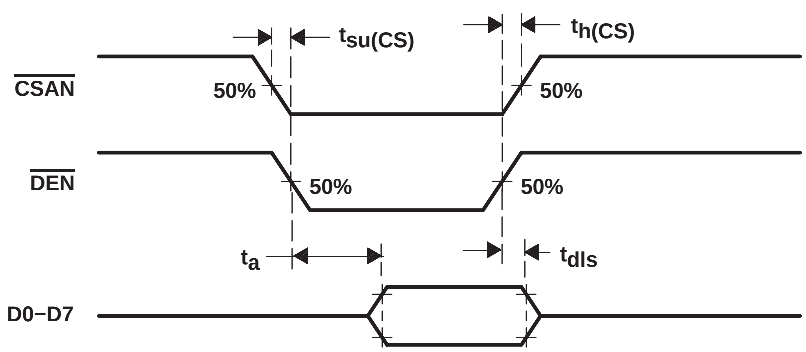


Figure 3. A/D Read Operation

PARAMETER MEASUREMENT INFORMATION

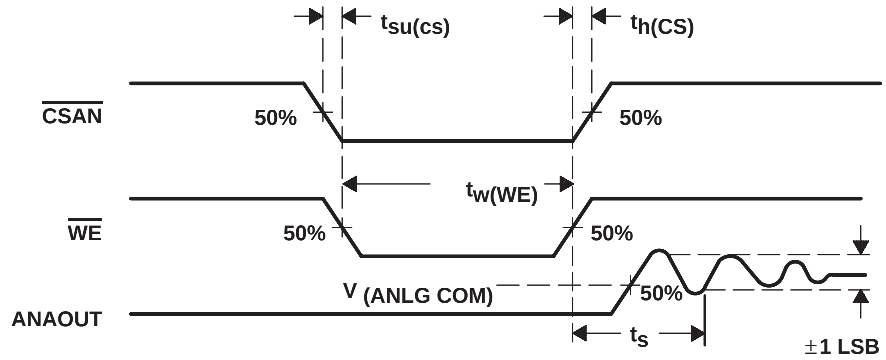


Figure 4. D/A Conversion Operation

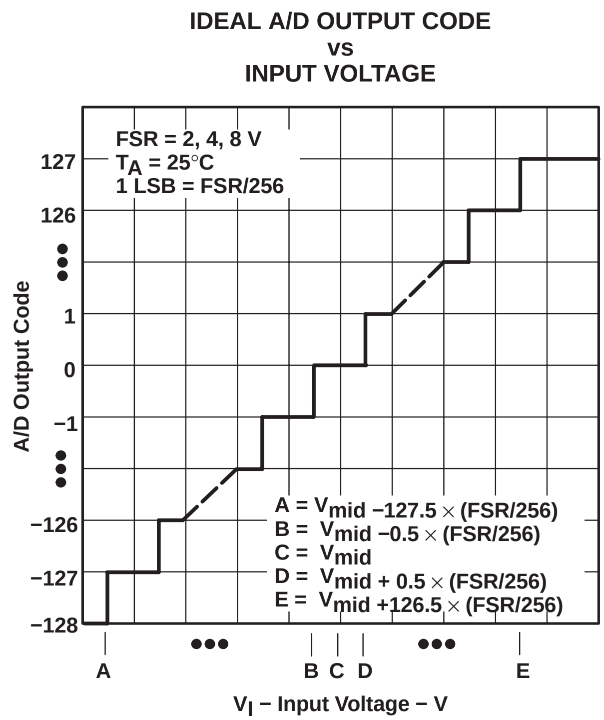


Figure 5

PARAMETER MEASUREMENT INFORMATION

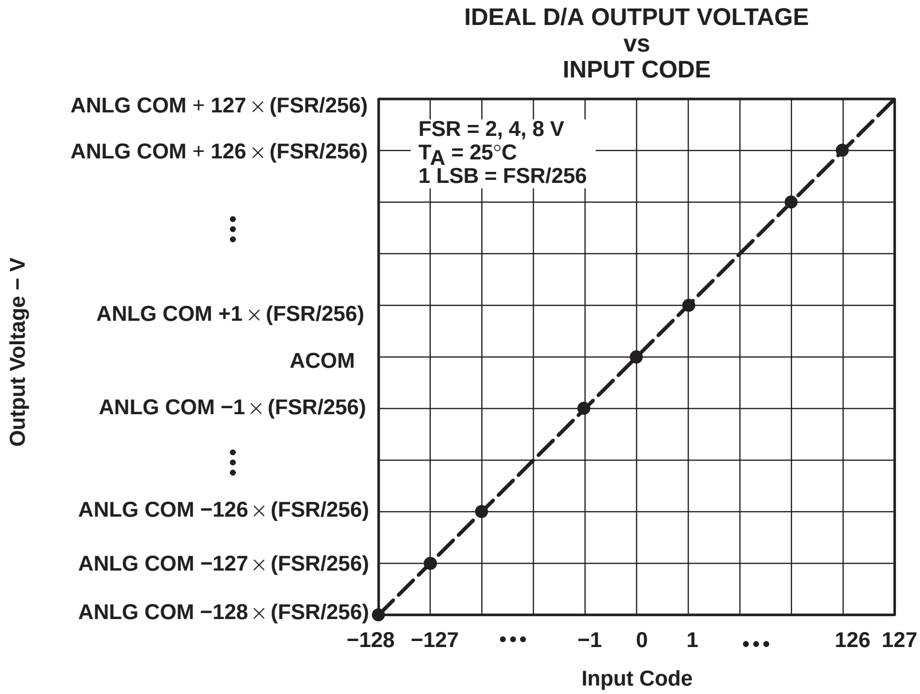


Figure 6

APPLICATION INFORMATION

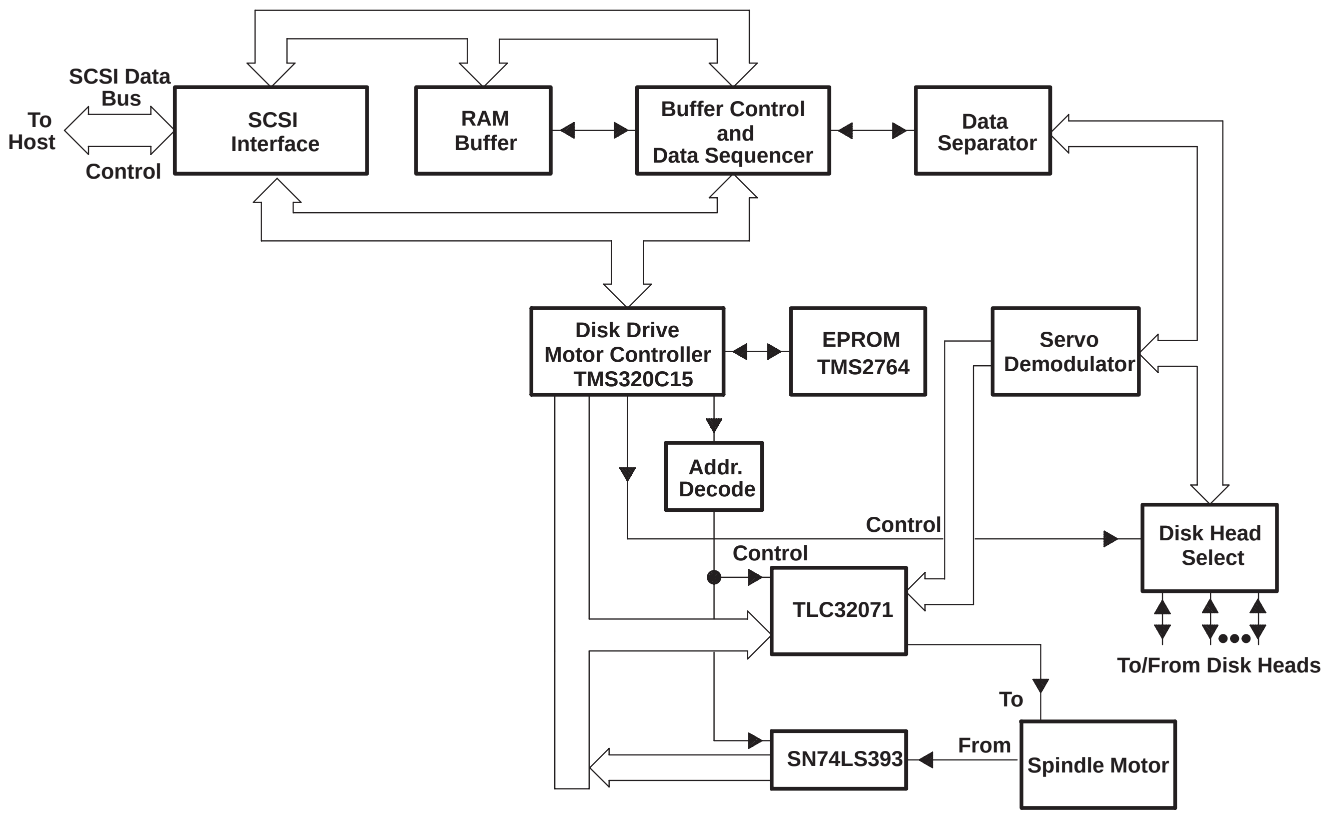


Figure 7. Simplified Disk-Drive Controller