CMOS 8-Bit Microcontroller

TMP86C845U

The TMP86C845 is the high-speed, high-performance and low-power consumption 8-bit microcomputer, including ROM, RAM, multi-function timer/counter, serial interface and 10-bit AD converter on chip.

Product No.	ROM	RAM	Package	OTP MCU
TMP86C845U	8K×8bits	256 × 8 bits	P-LQFP44-1010-0.80A	TMP86PM47U

Features

♦ 8-bit single chip microcomputer TLCS-870/C series

 Instruction execution time: 0.5 μs (at 8 MHz) $122 \mu s (at 32.768 kHz)$

◆ 132 types and 731 basic instructions

◆ 15 interrupt sources (External: 6, Internal: 9)

Input/Output ports (35 pins)

8-bit timer counter: 2 ch

• Timer, PWM, PPG, PDO, Event counter modes

Time base timer

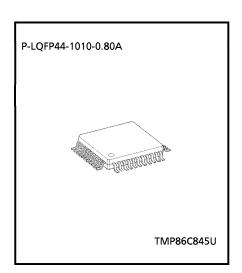
Watchdog timer

Serial interface

• 8-bit SIO: 1 ch

10-bit successive approximation type AD converter

• Analog input: 8 ch



Note: There are some difference between TMP86C845U and TMP86PM47U. Please refer to these data sheet about them.

For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.

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- ◆ Dual clock operation
 - Single/Dual-clock mode
- ♦ Nine power saving operating modes

• STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/High-impedance.

• SLOW 1, 2 mode: Low power consumption operation using low-frequency clock. (32.768 kHz)

• IDLE 0 mode: CPU stops, and peripherals operate using high-frequency clock of Time-Base-

Timer. Release by INTTBT interruput.

• IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock. Release by

interruputs.

• IDLE 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release

by interruputs.

• SLEEP 0 mode: CPU stops, and peripherals operate using low-frequency clock of Time-Base-

Timer. Release by INTTBT interruput.

• SLEEP 1 mode: CPU stops, and peripherals operate using low-frequency clock. Release by

interruputs.

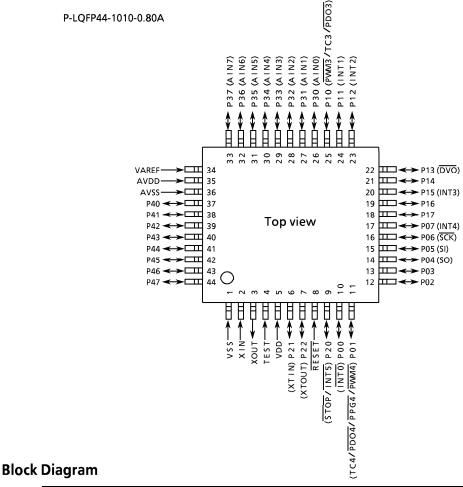
• SLEEP 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release

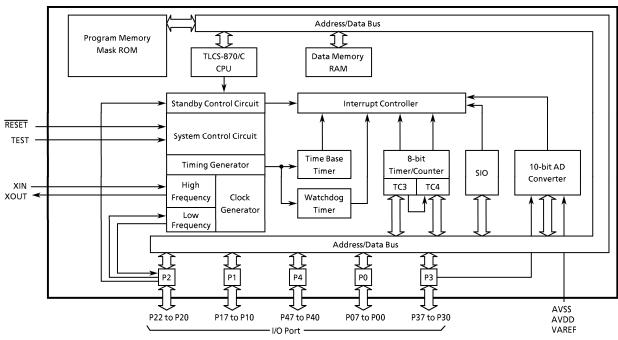
by interruputs.

♦ Wide operating voltage: 2.7 to 5.5 V at 8 MHz/32.768 kHz

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Pin Assignments (Top View)





Pin Functions

Pin Name	I/O	Functions						
P07 (INT4)	I/O (Input)		External interrupt input					
P06 (SCK)	I/O (Input/Output)							
P05 (SI)	I/O (Input)	8-bit I/O port.	SIO input/output					
P04 (SO)	I/O (Output)	When used as input port, external interrupt						
P03	I/O	input, serial clock input/output, serial data input/output and timer/counter 4						
P02	I/O	input/output, the latch must be set to "1".						
P01 (PWM4/TC4/ PDO4/PPG4)	I/O (Input/Output)		Timer/Counter input PPG output, PWM output, PDO output					
P00 (INTO)	I/O (Input)		External interrupt input					
P17	1/0							
P16	I/O		_					
P15 (INT3)	I/O (Input)	 8-bit I/O port with latch.	External interrupt input					
P14 (PPG)	I/O (Output)	Each bit of these ports can be individually	PPG output					
P13 (DVO)	I/O (Output)	configured as an input or an output under software control.	Divider output					
P12 (INT2/TC1)	I/O (Input)	An output latch is set to "1" when using it as a functional terminal.	External interrupt input					
P11 (INT1)	I/O (Input)	as a functional terminal.	External interrupt input.					
P10 (PWM3/TC3/PDO3)	I/O (Input/Output)		Timer/Counter input PWM output, PDO output					
P20 (ĪNT5/STOP1)	I/O (Input)	3-bit I/O port with latch.	External interrupt input STOP mode release signal input					
P21 (XTIN)	I/O (Input)	When used as input port, external interrupt input, and STOP mode release signal input,	Resonator connecting pins for low- frequency clock. For inputting external					
P22 (XTOUT)	I/O (Output)	the latch must be set to "1".	clock, XTIN is used and XTOUT is opened.					
P37 (AIN7)								
P36 (AIN6)								
P35 (AIN5)		 8-bit I/O port.						
P34 (AIN4)		Each bit of these ports can be individually						
P33 (AIN3)	I/O (Input)	configured as an input or output under software control.	AD converter analog inputs					
P32 (AIN2)		When used as analog input, then must be set to "1".						
P31 (AIN1)		set to 1.						
P30 (AIN0)								
P47								
P46								
P45								
P44		8-bit I/O port with latch. Each bit of these ports can be individually						
P43	1/0	configured as an input or an output under	_					
P42		software control.						
P41								
P40								
TEST	Input	Test pin for out-going test. Be fixed to Low.						
RESET	Input	Reset signal input						
XIN	Input	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN						
XOUT	Output	is used and XOUT is opened.						
VSS	•	0.0 [V] (GND)						
VDD		+5V						
AVSS	Power Supply	0.0 [V] (GND)						
AVDD	1.1.7	AD circuit power supply						
VAREF		Analog reference voltage inputs (High, Low)						
		Analog reference voltage inputs (High, Low)						

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

1.1 Memory Address Map

The TMP86C845 memory consist of 3 blocks: ROM, RAM and SFR (Special Function Register). They are all mapped in 64-Kbyte address space. Figure 1-1 shows the TMP86C845 memory address map. The general-purpose registers are not assigned to the RAM address space.

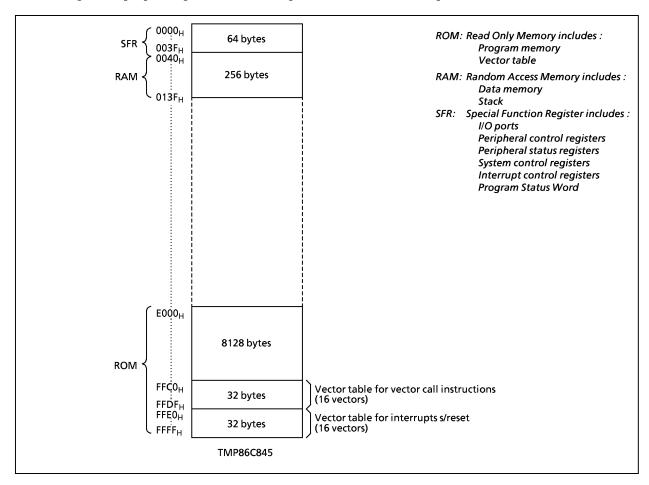


Figure 1-1. Memory Address Maps

1.2 Program Memory (ROM)

The TMP86C845 has a 8 K \times 8 bits (Address E000_H to FFFF_H), of program memory (mask programmed ROM). However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See 2.4.5 Address trap).

Input/Output Circuitry

(1) Control Pins

The input/output circuitries of the TMP86C847/H47/M47 control pins are shown below.

Control Pin	1/0	Input/Output Circuitry	Remarks
XIN XOUT	Input Output	Osc. enable fc VDD VDD Rf XIN XOUT	Resonator connecting pins (high-frequency) $R_f = 1.2 \ M\Omega \ (typ.)$ $R_O = 1.5 \ k\Omega \ (typ.)$
XTIN XTOUT	Input Output	NM1 NM2 Refer to port P2 VDD o R XTEN OVDD OVDD R R R R R R O VDD OVDD R XTIN XTOUT	Resonator connecting pins (Low-frequency) $R_f = 6 \ M\Omega \ (typ.)$ $R_O = 220 \ k\Omega \ (typ.)$
RESET	Input Output	R RIN RIN RIN RIN RIN RIN RIN RIN RIN RI	Hysteresis input Pull-up resistor $R_{\text{IN}} = 220 \text{ k}\Omega \text{ (typ.)}$ $R = 100 \Omega \text{ (typ.)}$
TEST	Input	R D1 D1	Pull-down resistor $R_{\text{IN}} = 70 \text{k}\Omega (\text{typ.})$ $R = 100 \Omega (\text{typ.})$

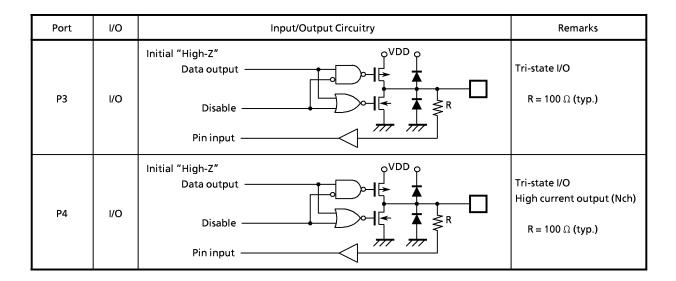
Note 1: The TEST pin of the TMP86PM47 does not have a pull-down resistor and protect diode (D1). Fix the TEST pin at low-level.

Note 2: The input circuitry of RESET pin of TMP86C845 is diffeernt from TMP86PM47's one.

(2) Input/Output Ports

Port	I/O	Input/Output Circuitry	Remarks
P07 to P05 P00	I/O	Initial "High-Z" Data output Input from output latch Pin input	Sink open drain output High current output Hysteresis input $R=100~\Omega~(typ.)$
P04 to P01	I/O	Initial "High-Z" Data output Input from output latch Pin input	Sink open drain output High current output R = 100Ω (typ.)
P15 P12 to P10	1/0	Initial "High-Z" Data output Disable Pin input	Tri-state I/O Hysteresis input $R=100~\Omega~(typ.)$
P17, P16 P14, P13	l/O	Initial "High-Z" Data output Disable Pin input	Tri-state I/O $R = 100 \Omega \text{ (typ.)}$
P2	I/O	Initial "High-Z" Data output Input from output latch Pin input	Sink open drain output High current output Hysteresis input $R=100~\Omega~(typ.)$

Note: In TMP87PM47, P04 to P01, P17, 16, P14 and P13 are hysteresis input.



Electrical Characteristics

Absolute Maximum Ratings $(V_{SS} = 0 V)$

Parameter	Symbol	Pins	Rating	Unit
Supply Voltage	V _{DD}		- 0.3 to 6.5	
Input Voltage	V _{IN}		- 0.3 to V _{DD} + 0.3] ,
Output Voltage	V _{OUT}		- 0.3 to V _{DD} + 0.3] '
	I _{OUT1} I _{OH}	P1, P3, P4 port	- 1.8	
Output Current (Per 1 pin)	I _{OUT2} I _{OL}	P1, P3 port	3.2	
	I _{OUT3} I _{OL}	P0, P2, P4 port	30	
Output Current (Total)	Σl _{OUT1}	P1, P3 port	60	mA
Output Current (Total)	ΣI _{OUT2}	P0, P2, P4 port	80	
Power Dissipation [T _{opr} = 85℃]	PD		250	mW
Soldering Temperature (Time)	Tsld		260 (10 sec)	
Storage Temperature	Tstg		– 55 to 125] ℃
Operating Temperature	Topr		- 40 to 85	

Note: The absolute maximum ratings are rated values, which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition $(V_{SS} = 0 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Pins	c	ondition	Min	Max	Unit
				NORMAL1, 2 mode	2.7		
			fc = 8 MHz	IDLE1, 2 mode	2.7		
Supply Voltage	V _{DD}		fs =	SLOW mode	2.7	5.5	
			32.768 kHz	SLEEP mode	2.7		
				STOP mode	2.0		
	V _{IH1}	Except Hysteresis input	$V_{DD} \ge 4.5 \text{ V}$ $V_{DD} < 4.5 \text{ V}$		$V_{DD} \times 0.70$		V
Input high Level	V _{IH2}	Hysteresis input			$V_{DD} \times 0.75$	V_{DD}	
	V _{IH3}				$V_{DD} \times 0.90$		
	V _{IL1}	Except Hysteresis input	V > 4.5.V			$V_{DD} \times 0.30$	
Input low Level	V _{IL2}	Hysteresis input	$V_{DD} \ge 4.5 V$		0	$V_{DD} \times 0.25$	
	V _{IL3}		V _{DD} < 4.5 V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V _{DD} =	= 2.7 to 5.5 V	1.0	8.0	MHz
Clock Frequency	fs	XTIN, XTOUT			30.0	34.0	kHz

The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics

 $(V_{SS} = 0 \text{ V, Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Pins	Condition	Min	Тур.	Max	Unit
Hysteresis Voltage	V _{HS}	Hysteresis input		-	0.9	-	V
	I _{IN1}	TEST					
Input Current	I _{IN2}	Sink Open Drain, Tri-state	$V_{DD} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}/0 \text{ V}$	_	_	± 2	μΑ
	I _{IN3}	RESET, STOP					
Lauret Basistana	R _{IN1}	TEST Pull-Down		_	70	_	I.O
Input Resistance	R _{IN2}	RESET Pull-Up		100	200	450	kΩ
Output Leakage	I _{LO1}	Sink Open Drain	V _{DD} = 5.5 V, V _{OUT} = 5.5 V	-	-	2	
Current	I _{LO2}	Tri-state	$V_{DD} = 5.5 \text{ V}, V_{OUT} = 5.5 \text{ V}/0 \text{ V}$	-	-	± 2	μΑ
Output High Voltage	V _{OH}	Tri-state Port	$V_{DD} = 4.5 \text{ V}, V_{OH} = -0.7 \text{ mA}$	4.1	_	_	V
Output Low Current	V _{OL}	Except XOUT, XTOUT, P0, P4, P2 Port	V _{DD} = 4.5 V, V _{OL} = 1.6 mA	-	-	0.4	
	l _{OL}	High Current Port (P0, P2, P4 Port)	V _{DD} = 4.5 V, V _{OL} = 1.0 V	_	20	_	
Supply Current in NORMAL1, 2 mode			V _{DD} = 5.5 V V _{IN} = 5.3/0.2 V	-	4.0	6.2	mA
Supply Current in IDLE0, 1, 2 mode			fc = 8 MHz fs = 32.768 kHz	ı	2.8	4.5	
Supply Current in SLOW1 mode			204	_	6	18	
Supply Current in SLEEP1 mode Supply Current in SLEEP0 mode			$V_{DD} = 3.0 \text{ V}$ $V_{IN} = 2.8/0.2 \text{ V}$ fs = 32.768 kHz	-	4	15	μ A
			32.700 11.12	-	4	13	
Supply Current in STOP mode			V _{DD} = 5.5 V V _{IN} = 5.3/0.2 V	-	0.5	10	

Note 1: Typical values show those at Topr = 25° C, $V_{DD} = 5 \text{ V}$

Note 2: Input current (I_{IN1}, I_{IN3}); The current through pull-up or pull-down resistor is not included.

Note 3: IDD does not include IREF current.

AD Conversion Characteristics

$(V_{SS} = 0.0 \text{ V}, 4.5 \text{ V to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog Reference Voltage	V _{AREF}		A _{VDD} - 1.0	-	A _{VDD}	
Power Supply Voltage of Analog Control Circuit	A _{VDD}			V _{DD}		v
Analog Reference Voltage Range	$\triangle V_{AREF}$		3.5	-	_	
Analog Input Voltage	V _{AIN}		V _{SS}	-	V _{AREF}	
Power Supply Current of Analog Reference Voltage	I _{REF}	$V_{DD} = A_{VDD} = V_{AREF} = 5.5 V$ $V_{SS} = AVSS = 0.0 V$	-	0.6	1.0	mA
Non linearity Error			_	_	± 2	
Zero Point Error		$V_{DD} = A_{VDD} = 5.0 \text{ V},$	-	_	± 2] , , ,
Full Scale Error		$V_{SS} = AVSS = 0.0 V$ $V_{\Delta REF} = 5.0 V$	-	-	± 2	LSB
Total Error		- AILL	-	-	± 2	

$(V_{SS} = 0.0 \text{ V}, 2.7 \text{ V to } 4.5 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog Reference Voltage	V _{AREF}		A _{VDD} – 1.0	-	A _{VDD}	
Power Supply Voltage of Analog Control Circuit	A _{VDD}			V _{DD}		v
Analog Reference Voltage Range	$\triangle V_{AREF}$		2.5	-	_	
Analog Input Voltage	V _{AIN}		V _{SS}	-	V _{AREF}	
Power Supply Current of Analog Reference Voltage	I _{REF}	$V_{DD} = A_{VDD} = V_{AREF} = 4.5 V$ $V_{SS} = AVSS = 0.0 V$	-	0.5	0.8	mA
Non linearity Error			-	-	± 2	
Zero Point Error		$V_{DD} = A_{VDD} = 2.7 \text{ V},$	-	-	± 2	LSB
Full Scale Error		$V_{SS} = AVSS = 0.0 V$ $V_{AREF} = 2.7 V$	-	-	± 2	LOB
Total Error		1 AILL	-	-	± 2	1

- Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.
- Note 2: Conversion time is different in recommended value by power supply voltage.
 - About conversion time, please refer to "2.8.2 Register Configuration".
- Note 3: Please use input voltage to AIN input Pin in limit of V_{AREF}- V_{SS}.

 When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.
- Note 4: Analog Reference Voltage Range: $\triangle V_{AREF} = V_{AREF} V_{SS}$

AC Characteristics

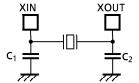
 $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

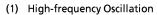
Parameter	Symbol	Condition	Min	Тур.	Max	Unit
		NORMAL1, 2 mode	_	-	4	
Machina Cuda Tima	+0.4	IDLE0, 1, 2 mode	0.5			μ\$
Machine Cycle Time	tcy	SLOW1, 2 mode		-	133.3	
		SLEEP0, 1, 2 mode	117.6			
High Level Clock Pulse Width	twcH	For external clock operation (XIN input)				ns
Low Level Clock Pulse Width	twcL	fc = 8 MHz	_	62.5	_	115
High Level Clock Pulse Width	twsH	For external clock operation (XTIN input)				
Low Level Clock Pulse Width	twsL	fs = 32.768 kHz	_	15.26	_	μS

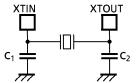
Recommended Oscillating Conditions

 $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 5.5 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Danamatan	0 111 1	Oscillation				Recommended Constant		
Parameter	Oscillator	Frequency	Recommended Oscillator		C ₁	C ₂		
		8 MHz	MURATA	CSA8.00MTZ	30 pF	30 pF		
High-frequency	Ceramic Resonator	6 IVITZ		CST8.00MTW	30 pF (built-in)	30 pF (built-in)		
Oscillation		4.40.8411-	MURATA	CSA4.19MG	30 pF	30 pF		
		4.19 MHz		CST4.19MGW	30 pF (built-in)	30 pF (built-in)		
Low-frequency	Crystal Oscillator	32.768 kHz	SII	VT-200	6 pF	6 pF		
Oscillation	Crystal Oscillator	32.700 KHZ	311	V1-200	брг	брг		







(2) Low-frequency Oscillation

- Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.
- Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL; http://www.murata.co.jp/search/index.html