CMOS 8-Bit Microcontroller

TMP86C847, TMP86CH47, TMP86CM47

The TMP86C847/H47/M47 are the high-speed, high-performance and low-power consumption 8-bit microcomputer, including ROM, RAM, multi-function timer/counter, serial interface a 10-bit AD converter on chip.

| Product No. | ROM | RAM | Package | OTP MCU |
|-------------|---------------|--------------|---------------------|------------|
| TMP86C847U | 8 K × 8 bits | F12 9 hite | | |
| TMP86CH47U | 16 K × 8 bits | 512 × 8 bits | P-LQFP44-1010-0.80A | TMP86PM47U |
| TMP86CM47U | 32 K × 8 bits | 1 K × 8 bits | | |

Features

◆ 8-bit single chip microcomputer TLCS-870/C series

• Instruction execution time: $0.25 \mu s$ (at 16 MHz) $122 \mu s (at 32.768 \text{ kHz})$

◆ 132 types and 731 basic instructions

18 interrupt sources (External: 6, Internal: 12)

◆ Input/Output ports (35 pins)

8-bit timer counter: 2 ch

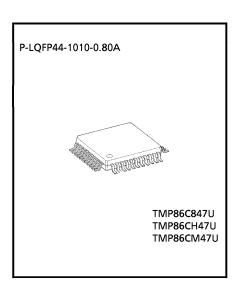
• Timer, PWM, PPG, PDO, Event counter modes

Time Base Timer

Watchdog Timer

• Interrupt source/reset output (programmable)

Serial interface • 8-bit SIO: 1 ch • 8-bit UART: 1 ch



For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.

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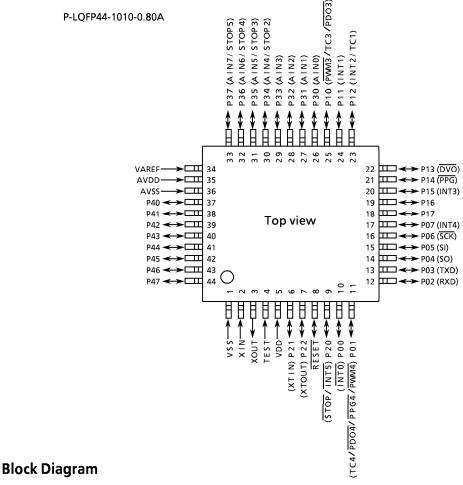
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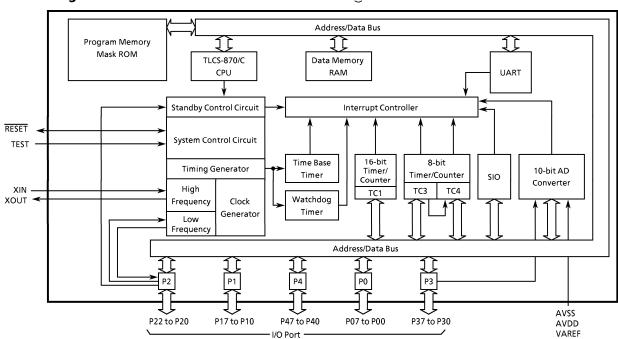
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86CM47-1 2002-09-11

- ♦ 10-bit successive approximation type AD converter
 - Analog input: 8 ch
- ◆ 16-bit timer counter: 1 ch
 - Timer, Event counter, Pulse width measurement, Programmable Pulse Generator (PPG), External-triggered Window modes
- ♦ Key On Wake Up: 4 ch
- ◆ Dual clock operation
 - Single/Dual-clock mode
- ◆ Nine power saving operating modes
 - $\bullet \quad STOP \ mode: \qquad Oscillation \ stops. \ Battery/Capacitor \ back-up. \ Port \ output \ hold/High-impedance.$
 - SLOW 1, 2 mode: Low power consumption operation using low-frequency clock. (32.768 kHz)
 - IDLE 0 mode: CPU stops, and peripherals operate using high-frequency clock of Time-Base-
 - Timer. Release by INTTBT interruput.
 - IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock. Release by
 - interruputs.
 - IDLE 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release
 - by interruputs.
 - SLEEP 0 mode: CPU stops, and peripherals operate using low-frequency clock of Time-Base-
 - Timer. Release by INTTBT interruput.
 - SLEEP 1 mode: CPU stops, and peripherals operate using low-frequency clock. Release by
 - interruputs.
 - SLEEP 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release
 - by interruputs.
- ♦ Wide operating voltage: 4.5 to 5.5 V at 16 MHz/32.768 kHz
 - 2.7 to 5.5 V at 8 MHz/32.768 kHz 1.8 to 5.5 V at 4.2 MHz/32.768 kHz

Pin Assignments (Top View)





Pin Functions

| Pin Name | I/O | Functi | ons | | | | |
|------------------------------|-----------------------|---|---|--|--|--|--|
| P07 (INT4) | I/O (Input) | | External interrupt input | | | | |
| P06 (SCK) | I/O (Input/Output) | | | | | | |
| P05 (SI) | I/O (Input) | 8-bit I/O port. | SIO input/output | | | | |
| P04 (SO) | I/O (Output) | When used as input port, external interrupt | | | | | |
| P03 (TXD) | I/O (Output) | input, serial clock input/output, serial data input/output and timer/counter 4 | UART Data output | | | | |
| P02 (RXD) | I/O (Input) | input/output, the latch must be set to "1". | UART Data input | | | | |
| P01 (PWM4/TC4/ PDO4/PPG4) | I/O (Input/Output) | | Timer/Counter input PPG output, PWM output, PDO output | | | | |
| P00 (INTO) | I/O (Input) | | External interrupt input | | | | |
| P17 | 1/0 | | _ | | | | |
| P16 | 1/0 | | | | | | |
| P15 (INT3) | I/O (Input) | 8-bit I/O port with latch. | External interrupt input | | | | |
| P14 (PPG) | I/O (Output) | Each bit of these ports can be individually configured as an input or an output under | PPG output | | | | |
| P13 (DVO) | I/O (Output) | software control. | Divider output | | | | |
| P12 (INT2/TC1) | I/O (Input) | An output latch is set to "1" when using it as a functional terminal. | External interrupt input. Timer/Counter input | | | | |
| P11 (INT1) | I/O (Input) | | External interrupt input. | | | | |
| P10 (PWM3/TC3/PDO3) | I/O (Input/Output) | | Timer/Counter input PWM output, PDO output | | | | |
| P20 (ĪNT5/STOP1) | I/O (Input) | 3-bit I/O port with latch. When used as input port, external interrupt | External interrupt input STOP mode release signal input | | | | |
| P21 (XTIN) | I/O (Input) | linput, and STOP mode release signal input, | Resonator connecting pins for low- frequency clock. For inputting external | | | | |
| P22 (XTOUT) | I/O (Output) | the latch must be set to "1". | clock, XTIN is used and XTOUT is opened. | | | | |
| P37 (AIN7/STOP5) | | | 5 T O B | | | | |
| P36 (AIN6/STOP4) | | | S T O P m o d e | | | | |
| P35 (AIN5/STOP3) | | 8-bit I/O port. | release signal | | | | |
| P34 (AIN4/STOP2) | I/O (Input) | Each bit of these ports can be individually configured as an input or output under | input | | | | |
| P33 (AIN3) | i/O (iliput) | software control. | AD converter analog inputs | | | | |
| P32 (AIN2) | | When used as analog input, then must be set to "1". | _ | | | | |
| P31 (AIN1) | | | | | | | |
| P30 (AIN0) | | | | | | | |
| P47 | | | | | | | |
| P46 | | | | | | | |
| P45 | | S hit I/O mant with latah | | | | | |
| P44 | I/O | 8-bit I/O port with latch. Each bit of these ports can be individually | | | | | |
| P43 | ",0 | configured as an input or an output under software control. | _ | | | | |
| P42 | | Software control. | | | | | |
| P41 | | | | | | | |
| P40 | | | | | | | |
| TEST | Input | Test pin for out-going test. Be fixed to Low. | | | | | |
| RESET | I/O | Reset signal input or watchdog timer output/a | address-trap-reset output | | | | |
| XIN | Input | Resonator connecting pins for high-frequency | clock. For inputting external clock, XIN | | | | |
| XOUT | Output | is used and XOUT is opened. | | | | | |
| VSS | | 0.0 [V] (GND) | | | | | |
| VDD | | +5V | | | | | |
| AVSS | Power Supply | 0.0 [V] (GND) | | | | | |
| AVDD | | AD circuit power supply | | | | | |
| VAREF | | Analog reference voltage inputs (High, Low) | | | | | |

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

1.1 Memory Address Map

The TMP86C847/H47/M47 memory consist of 4 blocks: ROM, RAM, DBR (Data Buffer Register) and SFR (Special Function Register). They are all mapped in 64-Kbyte address space. Figure 1-1 shows the TMP86C847/H47/M47 memory address map. The general-purpose registers are not assigned to the RAM address space.

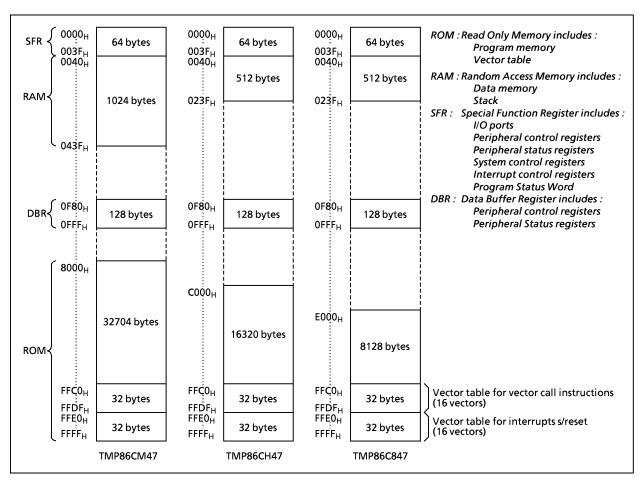


Figure 1-1. Memory Address Maps

1.2 Program Memory (ROM)

The TMP86C847 has a 8 K×8 bits (Address $E000_H$ to FFFF_H), TMP86CH47 has a 16 K×8 bits (Address $C000_H$ to FFFF_H), and the TMP86CM47 has a 32 K×8 bits (address 8000_H to FFFF_H) of program memory (mask programmed ROM). However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See 2.4.5 Address trap).

4. Electrical Characteristics

Absolute Maximum Ratings $(V_{SS} = 0 V)$

| Parameter | Symbol | Pins | Rating | Unit |
|--|-----------------------------------|-----------------|--------------------------------|------|
| Supply Voltage | V _{DD} | | – 0.3 to 5.5 | |
| Input Voltage | V _{IN} | | - 0.3 to V _{DD} + 0.3 |] , |
| Output Voltage | V _{OUT} | | - 0.3 to V _{DD} + 0.3 |] |
| | I _{OUT1} I _{OH} | P1, P3, P4 port | - 1.8 | |
| Output Current (Per 1 pin) | I _{OUT2} I _{OL} | P1, P3 port | 3.2 | |
| | I _{OUT3} I _{OL} | P0, P2, P4 port | 30 | |
| Output Current (Total) | Σl _{OUT1} | P1, P3 port | 60 | mA |
| Output Current (Total) | Σl _{OUT2} | P0, P2, P4 port | 80 |] |
| Power Dissipation [T _{opr} = 85℃] | PD | | 250 |] |
| Soldering Temperature (Time) | Tsld | | 260 (10 sec) | |
| Storage Temperature | Tstg | | – 55 to 125 | °c |
| Operating Temperature | Topr | | - 40 to 85 | |

Note: The absolute maximum ratings are rated values, which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition

 $(V_{SS} = 0 \text{ V, Topr} = -40 \text{ to } 85^{\circ}\text{C})$

| Parameter | Symbol | Pins | С | ondition | Min | Max | Unit | |
|------------------|------------------|-------------------------|--|-----------------------|----------------------|----------------------|------|--|
| | | | | NORMAL1, 2 mode | 4.5 | | | |
| | | | fc = 16 MHz | IDLE1, 2 mode | 4.5 | | | |
| | | | C. OBALL | NORMAL1, 2 mode | 2.7 | | | |
| | | | fc = 8 MHz | IDLE1, 2 mode | 2.7 | | | |
| Supply Voltage | V_{DD} | | fc = 4.2 MHz fs = 32.768 kHz | NORMAL1, 2 mode | | 5.5 | | |
| | | | | IDLE1, 2 mode | | | | |
| | | | | SLOW mode | 1.8 | | | |
| | | | | SLEEP mode | | | V | |
| | | | | STOP mode | | | | |
| | V _{IH1} | Except Hysteresis input | $V_{DD} \ge 4.5 V$ | | $V_{DD} \times 0.70$ | | | |
| Input high Level | V _{IH2} | Hysteresis input | | | $V_{DD} \times 0.75$ | V_{DD} | | |
| | V _{IH3} | | V _D | _{DD} < 4.5 V | $V_{DD} \times 0.90$ | | | |
| | V _{IL1} | Except Hysteresis input | | > 4 5 1/ | | $V_{DD} \times 0.30$ | | |
| Input low Level | V _{IL2} | Hysteresis input | V _C | _{DD} ≥ 4.5 V | 0 | $V_{DD} \times 0.25$ | | |
| | V _{IL3} | | V _D | _{DD} < 4.5 V | | $V_{DD} \times 0.10$ | | |
| | | | V _{DD} = 4.5 to 5.5 V | | | 16.0 | | |
| Clock Frequency | fc | XIN, XOUT | V _{DD} = 2.7 to 5.5 V | | 1.0 | 8.0 | MHz | |
| Clock Frequency | | | $V_{DD} = 1.8 \text{ to } 5.5 \text{ V}$ | | | 4.2 | | |
| | fs | XTIN, XTOUT | | | 30.0 | 34.0 | kHz | |

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics

 $(V_{SS} = 0 \text{ V, Topr} = -40 \text{ to } 85^{\circ}\text{C})$

| Parameter | Symbol | Pins | Condition | Min | Тур. | Max | Unit |
|------------------------------------|------------------|---|--|-----|------|-----|------|
| Hysteresis Voltage | V _{HS} | Hysteresis input | | - | 0.9 | - | V |
| | I _{IN1} | TEST | | | | | |
| Input Current | I _{IN2} | Sink Open Drain, Tri-state | $V_{DD} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}/0 \text{ V}$ | _ | _ | ± 2 | μΑ |
| | I _{IN3} | RESET, STOP | | | | | |
| Lauret Baristana | R _{IN1} | TEST Pull-Down | | _ | 70 | _ | 1.0 |
| Input Resistance | R _{IN2} | RESET Pull-Up | | 100 | 200 | 450 | kΩ |
| Output Leakage | I _{LO1} | Sink Open Drain | V _{DD} = 5.5 V, V _{OUT} = 5.5 V | - | - | 2 | |
| Current | I _{LO2} | Tri-state | V _{DD} = 5.5 V, V _{OUT} = 5.5 V/0 V | - | _ | ± 2 | μA |
| Output High Voltage | V _{OH} | Tri-state Port | $V_{DD} = 4.5 \text{ V}, V_{OH} = -0.7 \text{ mA}$ | 4.1 | _ | - | V |
| | V _{OL} | Except X _{OUT} , P0, P4, P2 Port | $V_{DD} = 4.5 V, V_{OL} = 1.6 \text{mA}$ | - | _ | 0.4 | |
| Output Low Current | I _{OL} | High Current Port (P0, P2, P4 Port) | V _{DD} = 4.5 V, V _{OL} = 1.0 V | _ | 20 | _ | |
| Supply Current in | | | V _{DD} = 5.5 V | _ | 7.5 | 9 | mA |
| NORMAL1, 2 mode | 4 | | $V_{IN} = 5.3/0.2 \text{ V}$ | | | | |
| Supply Current in IDLE0, 1, 2 mode | | | fc = 16 MHz fs = 32.768 kHz | _ | 5.5 | 6.5 | |
| Supply Current in | 1 | | 13 - 32.700 KHZ | | | | |
| SLOW1 mode | | | | _ | 8 | 20 | |
| Supply Current in | l _{DD} | | $V_{DD} = 3.0 \text{ V}$ $V_{IN} = 2.8/0.2 \text{ V}$ | | _ | 45 | |
| SLEEP1 mode | | | fs = 32.768 kHz | _ | 5 | 15 | μA |
| Supply Current in | 1 | | 15 = 52.765 KHZ | | 4 | 13 | 1 |
| SLEEP0 mode | | | | _ | 4 | 13 | |
| Supply Current in | | | $V_{DD} = 5.5 V$ $V_{IN} = 5.3/0.2 V$ | _ | 0.5 | 10 | |
| STOP mode | | | VIN - 3.3/0.2 V | | | | |

Note 1: Typical values show those at Topr = 25° C, $V_{DD} = 5 \text{ V}$

Note 2: Input current (I_{IN1} , I_{IN3}); The current through pull-up or pull-down resistor is not included.

Note 3: IDD does not include IREF current.

AD Conversion Characteristics

$(V_{SS} = 0.0 \text{ V}, 4.5 \text{ V to } 5.5 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$

| Parameter | Symbol | Condition | Min | Тур. | Max | Unit |
|---|----------------------|--|------------------------|-----------------|-------------------|---------|
| Analog Reference Voltage | V _{AREF} | | A _{VDD} - 1.0 | - | A _{VDD} | |
| Power Supply Voltage of Analog Control Circuit | A _{VDD} | | | V _{DD} | | v |
| Analog Reference Voltage Range | $\triangle V_{AREF}$ | | 3.5 | - | _ | |
| Analog Input Voltage | V _{AIN} | | V _{SS} | - | V _{AREF} | |
| Power Supply Current of Analog Reference Voltage | I _{REF} | $V_{DD} = A_{VDD} = V_{AREF} = 5.5 V$ $V_{SS} = AVSS = 0.0 V$ | - | 0.6 | 1.0 | mA |
| Non linearity Error | | | _ | _ | ± 2 | |
| Zero Point Error | | $V_{DD} = A_{VDD} = 5.0 \text{ V},$ | - | _ | ± 2 |] , , , |
| Full Scale Error | | $V_{SS} = AVSS = 0.0 V$ $V_{\Delta REF} = 5.0 V$ | - | - | ± 2 | LSB |
| Total Error | | - AILL | - | - | ± 2 | |

$(V_{SS} = 0.0 \text{ V}, 2.7 \text{ V to } 4.5 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$

| Parameter | Symbol | Condition | Min | Тур. | Max | Unit |
|---|----------------------|--|------------------------|-----------------|-------------------|------|
| Analog Reference Voltage | V_{AREF} | | A _{VDD} - 1.0 | - | A _{VDD} | |
| Power Supply Voltage of Analog Control Circuit | A _{VDD} | | | V _{DD} | | v |
| Analog Reference Voltage Range | $\triangle V_{AREF}$ | | 2.5 | - | _ | |
| Analog Input Voltage | V _{AIN} | | V _{SS} | - | V _{AREF} | |
| Power Supply Current of Analog Reference Voltage | I _{REF} | $V_{DD} = A_{VDD} = V_{AREF} = 4.5 V$ $V_{SS} = AVSS = 0.0 V$ | - | 0.5 | 0.8 | mA |
| Non linearity Error | | | - | - | ± 2 | |
| Zero Point Error | | $V_{DD} = A_{VDD} = 2.7 \text{ V},$ | - | - | ± 2 | LSB |
| Full Scale Error | | $V_{SS} = AVSS = 0.0 V$ $V_{\Delta REF} = 2.7 V$ | - | - | ± 2 | LOB |
| Total Error | | ANLI | - | - | ± 2 | |

(V_{SS} = 0.0 V, 2.0 V to 2.7 V, Topr = -40 to 85°C) (V_{SS} = 0.0 V, 1.8 V to 2.0 V, Topr = -10 to 85°C)

| Parameter | Symbol | Condition | Min | Тур. | Max | Unit |
|---|----------------------|--|------------------------|-----------------|-------------------|------|
| Analog Reference Voltage | V _{AREF} | | A _{VDD} - 0.9 | - | A _{VDD} | |
| Power Supply Voltage of Analog Control Circuit | A _{VDD} | | | V _{DD} | |] |
| Analog Reference Voltage Range | Δv | $1.8 \text{ V} \le \text{V}_{DD} < 2.0 \text{ V}$ | 1.8 | - | _ | V |
| | $\triangle V_{AREF}$ | $2.0 \text{ V} \le \text{V}_{DD} < 2.7 \text{ V}$ | 2.0 | - | _ | 1 |
| Analog Input Voltage | V _{AIN} | | V _{SS} | - | V _{AREF} | 1 |
| Power Supply Current of Analog Reference Voltage | I _{REF} | $V_{DD} = A_{VDD} = V_{AREF} = 2.7 \text{ V}$ $V_{SS} = AVSS = 0.0 \text{ V}$ | - | 0.3 | 0.5 | mA |
| Non linearity Error | | | - | _ | ± 4 | |
| Zero Point Error | | $V_{DD} = A_{VDD} = 1.8 \text{ V},$ | _ | _ | ± 4 |] |
| Full Scale Error | | $V_{SS} = AVSS = 0.0 V$ $V_{AREF} = 1.8 V$ | _ | _ | ± 4 | LSB |
| Total Error | | ANLI | - | - | ± 4 | |

- Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.

Note 2: Conversion time is different in recommended value by power supply voltage.

About conversion time, please refer to "2.8.2 Register Framing".

Note 3: Please use input voltage to AIN input Pin in limit of V_{AREF} - V_{SS}.

When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.

Note 4: Analog Reference Voltage Range: $\triangle V_{AREF} = V_{AREF} - V_{SS}$ Note 5: When AD is used with VDD < 2.7 V, the guaranteed temperature range varies with the operating voltage.

AC Characteristics

 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

| Parameter | Symbol | Condition | Min | Тур. | Max | Unit |
|------------------------------|--------|---|-------|-------|-------|------|
| | | NORMAL1, 2 mode | | | _ | |
| Machine Cycle Time | +0.4 | IDLE0, 1, 2 mode | 0.25 | _ | 4 | |
| | tcy | SLOW1, 2 mode | 447.6 | 447.6 | 422.2 | μS |
| | | SLEEP0, 1, 2 mode | _ | 133.3 | | |
| High Level Clock Pulse Width | twcH | For external clock operation (XIN input) | | 31.25 | | ns |
| Low Level Clock Pulse Width | twcL | fc = 16 MHz | _ | | - | 113 |
| High Level Clock Pulse Width | twsH | For external clock operation (XTIN input) | | 15.26 | - | |
| Low Level Clock Pulse Width | twsL | fs = 32.768 kHz | - | | | μ\$ |

$(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 4.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

| Parameter | Symbol | Condition | Min | Тур. | Max | Unit |
|------------------------------|--------|---|-------|-------|-------|------|
| | | NORMAL1, 2 mode | | | | |
| Machine Cycle Time | +01 | IDLE0, 1, 2 mode | 0.5 | _ | 4 | |
| | tcy | SLOW1, 2 mode | 117.5 | 422.2 | 422.2 | μS |
| | | SLEEP0, 1, 2 mode | _ | 133.3 | | |
| High Level Clock Pulse Width | twcH | For external clock operation (XIN input) | | 62.5 | | ns |
| Low Level Clock Pulse Width | twcL | fc = 8 MHz | _ | | - | 115 |
| High Level Clock Pulse Width | twsH | For external clock operation (XTIN input) | | 45.26 | | |
| Low Level Clock Pulse Width | twsL | fs = 32.768 kHz | _ | 15.26 | - | μS |

$(V_{SS} = 0 \text{ V}, V_{DD} = 1.8 \text{ to } 2.7 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

| Parameter | Symbol | Condition | Min | Тур. | Max | Unit |
|------------------------------|--------|---|-------|--------|-------|------|
| | | NORMAL1, 2 mode | | | _ | |
| Machine Cycle Time | +41.4 | IDLE0, 1, 2 mode | 0.95 | | 4 | |
| | tcy | SLOW1, 2 mode | 447.6 | | 122.2 | μS |
| | | SLEEP0, 1, 2 mode | 117.6 | _ | 133.3 | |
| High Level Clock Pulse Width | twcH | For external clock operation (XIN input) | | 119.05 | _ | ns |
| Low Level Clock Pulse Width | twcL | fc = 4.2 MHz | _ | | | 113 |
| High Level Clock Pulse Width | twsH | For external clock operation (XTIN input) | | 1F 2C | | ,,c |
| Low Level Clock Pulse Width | twsL | fs = 32.768 kHz | _ | 15.26 | - | μ |

Recommended Oscillating Conditions - 1

$$(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$$

| Danamatan | 0 771 4 | Oscillation | | Recommended Constant | | |
|---|--------------------|-------------|------------|------------------------|------------------|------------------|
| Parameter Oscillator | | Frequency | Recom | Recommended Oscillator | | C ₂ |
| | | 16 MHz | MURATA | CSA16.00MXZ040 | 10 pF | 10 pF |
| Lieb francis | High-frequency | 8 MHz | MURATA | CSA8.00MTZ | 30 pF | 30 pF |
| High-frequency Oscillation Ceramic Resonator | 8 IVITIZ | | CST8.00MTW | 30 pF (built-in) | 30 pF (built-in) | |
| Oscillation | | 4.19 MHz | MURATA | CSA4.19MG | 30 pF | 30 pF |
| | | 4. 19 IVID2 | | CST4.19MGW | 30 pF (built-in) | 30 pF (built-in) |
| Low-frequency | Crystal Oscillator | 32.768 kHz | SII | VT-200 | 6 pF | 6 pF |
| Oscillation | Crystal Oscillator | 32.700 KHZ | 311 | V 1-200 | σρι | o pi |

Recommended Oscillating Conditions - 2

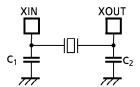
$$(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 5.5 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$$

| Parameter | Oscillator | Oscillation | Recommended Oscillator | | Recommended Constant | |
|-------------------------------|-------------------|-------------|------------------------|------------|----------------------|------------------|
| | | Frequency | | | C ₁ | C ₂ |
| High-frequency Oscillation | Ceramic Resonator | 8 MHz | MURATA | CSA8.00MTZ | 30 pF | 30 pF |
| | | | | CST8.00MTW | 30 pF (built-in) | 30 pF (built-in) |
| | | 4.19 MHz | MURATA | CSA4.19MG | 30 pF | 30 pF |
| | | | | CST4.19MGW | 30 pF (built-in) | 30 pF (built-in) |

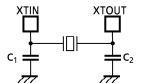
Recommended Oscillating Conditions - 3

$$(V_{SS} = 0 \text{ V}, V_{DD} = 1.8 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$$

| Do no ma et an | Oscillator | Oscillation | Recommended Oscillator | | Recommended Constant | |
|----------------|-------------------|-------------|------------------------|------------|----------------------|------------------|
| Parameter | | Frequency | | | C ₁ | C ₂ |
| High-frequency | Ceramic Resonator | 4.19 MHz | MURATA | CSA4.19MG | 30 pF | 30 pF |
| Oscillation | | | | CST4.19MGW | 30 pF (built-in) | 30 pF (built-in) |



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

- Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.
- Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL; http://www.murata.co.jp/search/index.html