#### CMOS 8-Bit Microcontroller

## TMP86CS44U

The TMP86CS44 are the high-speed, high-performance and low-power consumption 8-bit microcomputer, including ROM, RAM, multi-function timer/counter, serial interface a 10-bit AD converter on chip.

	Product No.	ROM	RAM	Package	OTP MCU
Γ	TMP86CS44U	60 K × 8 bits	1 K × 8 bits	P-LQFP44-1010-0.80A	TMP86PS44U

#### **Features**

◆ 8-bit single chip microcomputer TLCS-870/C series

• Instruction execution time:  $0.25 \mu s$  (at 16 MHz)  $122 \mu s (at 32.768 kHz)$ 

◆ 132 types and 731 basic instructions

19 interrupt sources (External: 6, Internal: 13)

◆ Input/Output ports (35 pins)

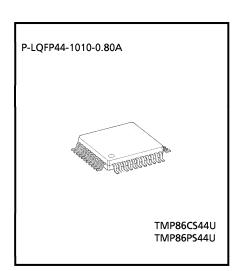
◆ 16-bit timer counter: 2 ch

• Timer, Event counter, Pulse width measurement, Programmable Pulse Generator (PPG), External-trigger Window modes

◆ 8-bit timer counter: 2 ch

• Timer, PWM, PPG, PDO, Event counter modes

- Time Base Timer
- Divider output
- Watchdog Timer
  - Interrupt source/reset output (programmable)



For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled

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Serial interface

8-bit SIO: 1 ch8-bit UART: 1 ch

◆ 10-bit successive approximation type AD converter

• Analog input: 8 ch

♦ 8-bit DA converter

• Analog output: 1 ch

♦ Key On Wake Up: 4 ch

◆ Dual clock operation

• Single/Dual-clock mode

◆ Nine power saving operating modes

• STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/High-impedance.

• SLOW1 mode: Low power consumption operation using low-frequency clock.

SLOW2 mode: Low power consumption operation using high and low frequency clock.

• IDLE 0 mode: CPU stops, and peripherals operate using high-frequency clock of Time-Base-

Timer. Release by falling edge of the clock which is set by TBTCR (TBTCK).

• IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock. Release by

interruputs.

• IDLE 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release

by interruputs.

• SLEEP 0 mode: CPU stops, and peripherals operate using low-frequency clock of Time-Base-

Timer. Release by falling edge of the clock which is set by TBTCR (TBTCK).

• SLEEP 1 mode: CPU stops, and peripherals operate using low-frequency clock. Release by

interruputs.

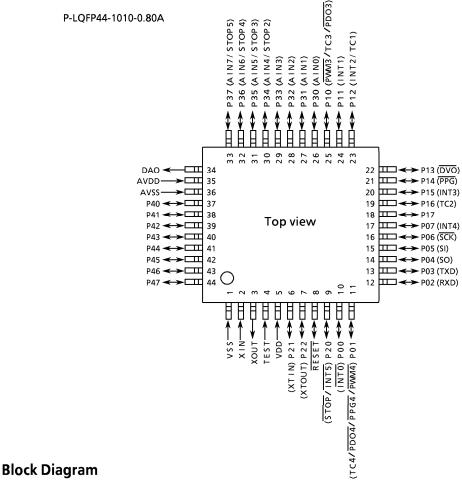
• SLEEP 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release

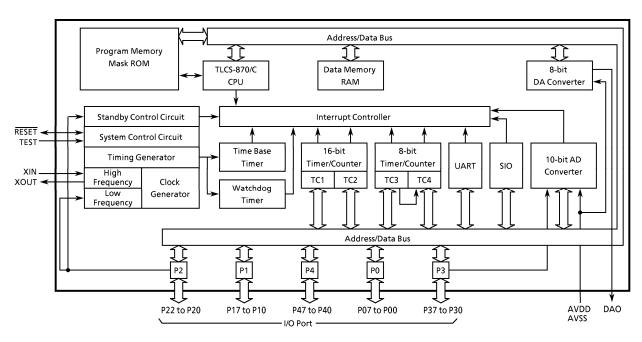
by interruputs.

♦ Wide operating voltage: 4.5 to 5.5 V at 16 MHz/32.768 kHz

2.7 to 5.5 V at 8 MHz/32.768 kHz

# Pin Assignments (Top View)





# **Pin Functions**

Pin Name	I/O	Functi	ons					
P07 (INT4)	I/O (Input)		External interrupt input					
P06 (SCK)	I/O (Input/Output)							
P05 (SI)	I/O (Input)	8-bit I/O port.	SIO input/output					
P04 (SO)	I/O (Output)	When used as input port, external interrupt						
P03 (TXD)	I/O (Output)	input, serial clock input/output, serial data input/output and timer/counter 4	UART Data output					
P02 (RXD)	I/O (Input)	input/output, the latch must be set to "1".	UART Data input					
P01 (PWM4/TC4/ PDO4/PPG4)	I/O (Input/Output)		Timer/Counter input PPG output, PWM output, PDO output					
P00 ( <del>INT0</del> )	I/O (Input)		External interrupt input					
P17	I/O		_					
P16(TC2)	I/O(Input)		Timer/Counter input					
P15 (INT3)	I/O (Input)	   8-bit I/O port with latch.	External interrupt input					
P14 (PPG)	I/O (Output)	Each bit of these ports can be individually	PPG output					
P13 (DVO)	I/O (Output)	configured as an input or an output under software control.	Divider output					
P12 (INT2/TC1)	I/O (Input)	An output latch is set to "1" when using it	External interrupt input, Timer/Counter					
P11 (INT1)	I/O (Input)	as a functional terminal.	External interrupt input					
P10 (PWM3/TC3/PDO3)	I/O (Input/Output)		Timer/Counter input PWM output, PDO output					
P20 (INT5/STOP1)	I/O (Input)	3-bit I/O port with latch. When used as input port, external interrupt	External interrupt input STOP mode release signal input					
P21 (XTIN)	I/O (Input)	input, and STOP mode release signal input,	Resonator connecting pins for low-					
P22 (XTOUT)	I/O (Output)	the latch must be set to "1".	frequency clock. For inputting external clock, XTIN is used and XTOUT is opened.					
P37 (AIN7/STOP5)			,					
P36 (AIN6/STOP4)			STOP mode   r e l e a s e					
P35 (AIN5/STOP3)		   8-bit I/O port.	signal					
P34 (AIN4/STOP2)		Each bit of these ports can be individually	input					
P33 (AIN3)	I/O (Input)	configured as an input or output under software control.	AD converter analog inputs					
P32 (AIN2)		When used as analog input, then must be						
P31 (AIN1)		set to "1"	-					
P30 (AIN0)								
P47								
P46								
P45								
P44		8-bit I/O port with latch.						
P43	I/O	Each bit of these ports can be individually configured as an input or an output under	_					
P42		software control.						
P41								
P40								
TEST	Input	Test pin for out-going test. Be fixed to Low.						
RESET	I/O	Reset signal input or watchdog timer output/a	address-tran-reset output					
XIN	Input							
XOUT	Output	Resonator connecting pins for high-frequency clock. For inputting external clock is used and XOUT is opened.						
VSS	Gutput	·						
VDD		0.0 [V] (GND)						
AVSS	Power Supply	+5 V						
AVDD		+ 5 V AD, DA circuit GND  + 5 V AD, DA circuit power supply						
DAO	Output	, , , , , , , , , , , , , , , , , , , ,						
DAU	Output	DA converter analog output						

## **Operational Description**

#### 1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

### 1.1 Memory Address Map

The TMP86CS44 memory consist of 4 blocks: ROM, RAM and SFR (Special Function Register). They are all mapped in 64-Kbyte address space. Figure 1-1 shows the TMP86CS44 memory address map. The general-purpose registers are not assigned to the RAM address space.

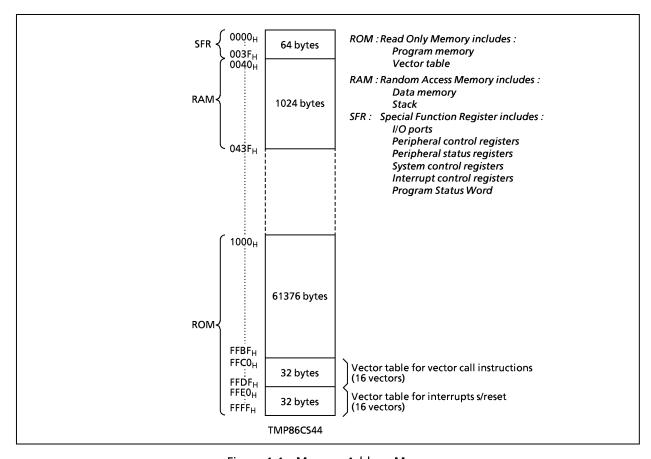


Figure 1-1. Memory Address Maps

### 1.2 Program Memory (ROM)

The TMP86CS44 has a  $60 \text{ K} \times 8$  bits (Address  $1000_H$  to FFFF<sub>H</sub>) of program memory (mask programmed ROM). However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See 2.4.5 Address trap).

#### 4. Electrical Characteristics

Absolute Maximum Ratings  $(V_{SS} = 0 V)$ 

Parameter	Symbol	Pins	Rating	Unit
Supply Voltage	V <sub>DD</sub>		- 0.3 to 6.5	
Input Voltage	V <sub>IN</sub>		- 0.3 to V <sub>DD</sub> + 0.3	] ,
Output Voltage	V <sub>OUT</sub>		- 0.3 to V <sub>DD</sub> + 0.3	] '
	I <sub>OUT1</sub> I <sub>OH</sub>	P1, P3, P4 port	- 1.8	
Output Current (Per 1 pin)	I <sub>OUT2</sub> I <sub>OL</sub>	P1, P3 port	3.2	
	I <sub>OUT3</sub> I <sub>OL</sub>	P0, P2, P4 port	30	
Output Compat (Total)	ΣI <sub>OUT1</sub>	P1, P3 port	60	mA
Output Current (Total)	ΣI <sub>OUT2</sub>	P0, P2, P4 port	80	
Power Dissipation $[T_{opr} = 85^{\circ}C]$	PD		250	
Soldering Temperature (Time)	Tsld		260 (10 sec)	
Storage Temperature	Tstg		– 55 to 125	°c
Operating Temperature	Topr		- 40 to 85	

Note: The absolute maximum ratings are rated values, which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition

 $(V_{SS} = 0 \text{ V, Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

Parameter	Symbol	Pins	С	ondition	Min	Max	Unit	
				NORMAL1, 2 mode	4.5			
			fc = 16 MHz	IDLE0,1, 2 mode	4.5	_		
				NORMAL1, 2 mode				
			fc = 8 MHz	IDLE0,1, 2 mode				
Supply Voltage	V <sub>DD</sub>			NORMAL1, 2 mode	•	5.5		
			fs = 32.768 kHz	IDLE0,1, 2 mode	2.7			
				SLOW1,2 mode				
				SLEEP0,1,2 mode				
				STOP mode	2.0		V	
	V <sub>IH1</sub>	Except Hysteresis input	V	$V_{DD} \ge 4.5 V$				
Input high Level	V <sub>IH2</sub>	Hysteresis input	v <sub>D</sub>			$V_{DD}$		
	V <sub>IH3</sub>		VD	<sub>DD</sub> < 4.5 V	$V_{DD} \times 0.90$			
	V <sub>IL1</sub>	Except Hysteresis input	\/_	<sub>oD</sub> ≧ 4.5 V		$V_{DD} \times 0.30$		
Input low Level	V <sub>IL2</sub>	Hysteresis input	<b>V</b> D	5D = 4.5 V	0	$V_{DD} \times 0.25$		
	V <sub>IL3</sub>		V <sub>D</sub>	<sub>D</sub> < 4.5 V		$V_{DD} \times 0.10$		
		VIII VOUT	$V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$			16.0	MHz	
Clock Frequency	fc	XIN, XOUT	$V_{DD} = 2.7 \text{ to } 5.5 \text{ V}$		1.0	8.0	IVIIIZ	
	fs	XTIN, XTOUT			30.0	34.0	kHz	

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

**DC** Characteristics

 $(V_{SS} = 0 \text{ V, Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

Parameter	Symbol	Pins	Condition	Min	Тур.	Max	Unit
Hysteresis Voltage	V <sub>HS</sub>	Hysteresis input		-	0.9	-	V
	I <sub>IN1</sub>	TEST					
Input Current	I <sub>IN2</sub>	Sink Open Drain, Tri-state	$V_{DD} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}/0 \text{ V}$	_	_	± 2	μΑ
	I <sub>IN3</sub>	RESET, STOP					
Lauret Bardatana	R <sub>IN1</sub>	TEST Pull-Down		_	70	_	1.0
Input Resistance	R <sub>IN2</sub>	RESET Pull-Up		100	200	450	kΩ
Output Leakage	I <sub>LO1</sub>	Sink Open Drain	V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub> = 5.5 V	-	-	2	
Current	I <sub>LO2</sub>	Tri-state	V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub> = 5.5 V/0 V	-	-	± 2	μΑ
Output High Voltage	V <sub>OH</sub>	Tri-state Port	$V_{DD} = 4.5  V, V_{OH} = -0.7  \text{mA}$	4.1	-	-	.,
Output Low Voltage	V <sub>OL</sub>	Except XOUT, P0, P2, P4 Port	V <sub>DD</sub> = 4.5 V, I <sub>OL</sub> = 1.6 mA	_	-	0.4	V
Output Low Current	I <sub>OL</sub>	High Current Port (P0, P2, P4 Port)	V <sub>DD</sub> = 4.5 V, V <sub>OL</sub> = 1.0 V	_	20	-	
Supply Current in			V <sub>DD</sub> = 5.5 V	_	10.5	12	
NORMAL1, 2 mode	1		V <sub>IN</sub> = 5.3/0.2 V				mA
Supply Current in			fc = 16 MHz	_	5.5	6.5	
IDLE0,1, 2 mode	1		fs = 32.768 kHz		0.0		
Supply Current in				_	8	20	
SLOW1 mode			V <sub>DD</sub> = 3.0 V			20	
Supply Current in	I <sub>DD</sub>		$V_{IN} = 2.8/0.2 \text{ V}$		5	15	
SLEEP1 mode			fs = 32.768 kHz	_	٥	2	μΑ
Supply Current in	]					13	
SLEEP0 mode				-	4	13	
Supply Current in			$V_{DD} = 5.5 V$	_	0.5	10	
STOP mode			$V_{IN} = 5.3/0.2 V$		0.5	'0	

Note 1: Typical values show those at Topr =  $25^{\circ}$ C,  $V_{DD} = 5 \text{ V}$ 

Note 2: Input current ( $I_{IN1}$ ,  $I_{IN3}$ ); The current through pull-up or pull-down resistor is not included.

Note 3: IDD does not include IREF current.

Note 4: The supply currents of SLOW2 and SLEEP2 modes are equivalent to IDLE 0,1,2.

## **AD Conversion Characteristics**

## $(V_{SS} = 0.0 \text{ V}, V_{DD} = 4.5 \text{ V} \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Symbol Condition		Тур.	Max	Unit
Analog Reference Voltage	$V_{AREF}$	V <sub>AREF</sub> = A <sub>VDD</sub> - A <sub>VSS</sub>	A <sub>VDD</sub>	-	A <sub>VDD</sub>	
Power Supply Voltage of Analog Control Circuit	A <sub>VDD</sub>	$A_{VSS} = V_{SS}$ $V_{DD}$			V	
Analog Input Voltage	V <sub>AIN</sub>	$A_{VSS} = V_{SS}, A_{VDD} = V_{DD}$	V <sub>SS</sub>	-	V <sub>DD</sub>	
Power Supply Current of Analog Reference Voltage	I <sub>REF</sub>	$V_{DD} = A_{VDD} = 5.5 V$ $V_{SS} = A_{VSS} = 0.0 V$	-	0.6	1.0	mA
Non linearity Error			-	-	± 2	
Zero Point Error		$V_{DD} = A_{VDD} = 5.0 \text{ V},$	-	-	± 2	LSB
Full Scale Error		$V_{SS} = A_{VSS} = 0.0 \text{ V}$ $V_{AREF} = A_{VDD} - A_{VSS}$	-	-	± 2	135
Total Error		700 000	_	-	± 2	

### $(V_{SS} = 0.0 \text{ V}, V_{DD} = 2.7 \text{ V to } 4.5 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog Reference Voltage	V <sub>AREF</sub>	V <sub>AREF</sub> = A <sub>VDD</sub> - A <sub>VSS</sub>	A <sub>VDD</sub>	_	A <sub>VDD</sub>	
Power Supply Voltage of Analog Control Circuit	A <sub>VDD</sub>	$A_{VSS} = V_{SS}$		V <sub>DD</sub>		V
Analog Input Voltage	V <sub>AIN</sub>	$A_{VSS} = V_{SS}, A_{VDD} = V_{DD}$	V <sub>SS</sub>	_	V <sub>DD</sub>	
Power Supply Current of Analog Reference Voltage	I <sub>REF</sub>	$V_{DD} = A_{VDD} = 4.5 \text{ V}$ $V_{SS} = A_{VSS} = 0.0 \text{ V}$	-	0.5	0.8	mA
Non linearity Error			-	_	± 2	
Zero Point Error		$ V_{DD} = A_{VDD} = 2.7 V, $	-	_	± 2	LSB
Full Scale Error		$ \begin{array}{c} V_{SS} = A_{VSS} = 0.0 \text{ V} \\ V_{AREF} = A_{VDD} - A_{VSS} \end{array} $	-	_	± 2	135
Total Error		AILL VOD V33	-	_	± 2	

## $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 4.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

- Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.
- Note 2: Conversion time is different in recommended value by power supply voltage.

About conversion time, please refer to Figure 2-64.

Note 3: Please use input voltage to AIN input Pin in limit of V<sub>AREF</sub> - V<sub>SS</sub>.

When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.

Note 4: Analog Reference Voltage Range:  $\triangle V_{AREF} = A_{VDD} - A_{VSS}$ 

**DA Conversion Characteristics** 

 $(V_{SS} = 0.0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog Reference	A <sub>VDD</sub>	$A_{VDD} = V_{DD}$		_	5.5	V
voltage A <sub>VSS</sub>		$A_{VSS} = V_{SS}$		-	V <sub>SS</sub>	]
Resolution			_	-	8	Bits
Linearity Error (Note 1)		$A_{VDD} = V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$ $A_{VSS} = V_{SS} = 0 \text{ V}$ Load conditions 5 pF, 10 M $\Omega$	-	-	± 5	LSB
Settling Time					4	ms
Reference Current (DA Power Dissipation) (Note 2)	I <sub>DREF</sub>	No load, V <sub>DD</sub> = 5.5 V, fc = 16 MHz	-	350	500	
DAO Output Current (Note 3)	I <sub>DAO</sub>	$A_{VDD} = V_{DD} = 4.5 \text{ V}$ $A_{VSS} = V_{SS} = 0 \text{ V}$ No load 0.5 V bias when inputting 7FH	14	19	-	μΑ

**DA Conversion Characteristics** 

 $(V_{SS} = 0.0 \text{ V}, V_{DD} = 2.7 \text{ to } 4.5 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$ 

Parameter	Symbol	Conditio	n	Min	Тур.	Max	Unit
Analog Reference	$A_{VDD}$	$A_{VDD} = V_{DD}$	$A_{VDD} = V_{DD}$			4.5	V
voltage	A <sub>VSS</sub>	$A_{VSS} = V_{SS}$	V <sub>SS</sub>	_	V <sub>SS</sub>	]	
Resolution				1	_	8	Bits
		$A_{VSS} = V_{SS} = 0 V$	– 10°C≦Ta≦85°C			+ 5	- LSB
Linaanitu Funan (Nata 1)			- 10 C= 1a=65 C	_	_	-8	
Linearity Error (Note 1)			– 40°C≦Ta< – 10°C			+ 5	
			-40 C= 10 C		_	- 26	
Settling Time						6	ms
Reference Current							
(DA Power Dissipation)	I <sub>DREF</sub>	No load, $V_{DD} = 2.7 \text{ V, fc} = 8 \text{ MH}$	Ηz	-	200	300	
(Note 2)							,
DAG Contract Comment		$A_{VDD} = V_{DD} = 2.7 \text{ V}$	0.4	5.3		μA	
DAO Output Current	I <sub>DAO</sub>	$A_{VSS} = V_{SS} = 0 V$			_		
(Note 3)		No load 0.5 V bias when inputting 7FH					

Note 1: In linearity error measurements, the first code  $(00_H, 01_H)$  and the last code  $(FE_H, FF_H)$  are excluded. Note 2: DA converter power dissipation Note 3: DAO current drive capability

## **AC Characteristics**

 $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$ 

Parameter	Symbol	mbol Condition		Тур.	Max	Unit
		NORMAL1, 2 mode			4	- μ <b>s</b>
Machine Cycle Time	4	IDLE0,1, 2 mode	0.25	_		
Machine Cycle Time	tcy	SLOW1, 2 mode	447.6	_	133.3	
		SLEEP0, 1, 2 mode	117.6			
High Level Clock Pulse Width	t <sub>WCH</sub>	For external clock operation (XIN input)				ns
Low Level Clock Pulse Width	t <sub>WCL</sub>	fc = 16 MHz	_	31.25	_	115
High Level Clock Pulse Width	t <sub>WSH</sub>	For external clock operation (XTIN input)		45.00		
Low Level Clock Pulse Width	t <sub>WSL</sub>	fs = 32.768 kHz	_	15.26	_	μS

# $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 4.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
		NORMAL1, 2 mode			4	
Machine Cycle Time	4	IDLE0,1, 2 mode	0.5	_		
Machine Cycle Time	tcy	SLOW1, 2 mode	117.6	_	133.3	μS
		SLEEP0, 1, 2 mode	117.6			<u> </u>
High Level Clock Pulse Width	t <sub>WCH</sub>	For external clock operation (XIN input)		62.5		ns
Low Level Clock Pulse Width	t <sub>WCL</sub>	fc = 8 MHz	_		_	''3
High Level Clock Pulse Width	t <sub>WSH</sub>	For external clock operation (XTIN input)		45.00		μS
Low Level Clock Pulse Width	t <sub>WSL</sub>	fs = 32.768 kHz	-	15.26	-	$\mu$ 5

## **Recommended Oscillating Conditions - 1**

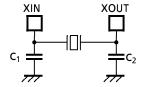
$$(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$$

Davamatas	0.28.4	Oscillation			Recommended Constant		
Parameter	Oscillator	Frequency	Recom	mended Oscillator	C <sub>1</sub>	C <sub>2</sub>	
		16 MHz	MURATA	CSA16.00MXZ040	10 pF	10 pF	
High francisco	Ceramic Resonator	0.0411-	MURATA	CSA8.00MTZ	30 pF	30 pF	
High-frequency Oscillation		8 MHz		CST8.00MTW	30 pF (built-in)	30 pF (built-in)	
Oscillation		4.40.0411-	MURATA	CSA4.19MG	30 pF	30 pF	
		4.19 MHz		CST4.19MGW	30 pF (built-in)	30 pF (built-in)	
Low-frequency	Country Contillation	32.768 kHz	SII	VT-200	6 pF	6 pF	
Oscillation	Crystal Oscillator	32.700 KHZ	311	V1-200	о рг	брг	

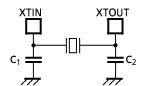
## Recommended Oscillating Conditions - 2

$$(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$$

Parameter	Oscillator	Oscillation	Recommended Oscillator		Recommended Constant	
		Frequency			C <sub>1</sub>	C <sub>2</sub>
High-frequency Oscillation	Ceramic Resonator	8 MHz	MURATA	CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
		4.19 MHz	MURATA	CSA4.19MG	30 pF	30 pF
				CST4.19MGW	30 pF (built-in)	30 pF (built-in)



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

- Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.
- Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL; http://www.murata.co.jp/search/index.html

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